VISVESVARAYA TECHNOLOGICAL UNIVERSITY

"Jnana Sangama" Belagavi – 590 010

PROJECT REPORT ON

"DESIGN OF MULTIPLIER USING LOW POWER HIGH SPEED HYBRID FULL ADDER"

Submitted in partial fulfillment of the requirements for the award of degree

BACHELOR OF ENGINEERING
IN
ELECTRONICS & COMMUNICATION ENGINEERING

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ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

CERTIFICATE

Certified that the project work entitled "**DESIGN OF MULTIPLIER USING LOW POWER HIGH SPEED HYBRID FULL ADDER**" *is a bona fide work carried out by*

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in partial fulfillment for the award of BACHELOR OF ENGINEERING in **ELECTRONICS & COMMUNICATION ENGINEERING** of the **VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI** during the year 2016–2017. It is certified that all corrections/suggestions indicated for Internal Assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the Bachelor of Engineering Degree.

15/05/17	15/05/17	
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ABSTRACT

Arithmetic operations are widely used in most micro electronic systems. Addition is a fundamental arithmetic operation and is the base of many other commonly used arithmetic operation. Also, the other operations such as the subtraction, multiplication and division can be derived from addition and hence adders often seen as the most significant parts of the arithmetic unit.

Design of high performance adders has been difficult task for from long time and is an important goal because of the fast growing technology in mobile computation. High performance indicates smaller area, high throughput circuitry, low power consumption and high speed.

The proposed design defines the novel architecture of adder using pass transistor and transmission gate logic which efficiently reduces the power, area and delay as compared to the existing adder system. The proposed method is developed using cadence tool of 180nm technology. The pass transistor and transmission gate logic makes the computation faster. The proposed adder system is implemented on Braun Multiplier and ALU. The designed adder system significantly reduces the power consumption, area and delay compared with existing adder system.

The proposed adders are constructed in two different ways using 14 transistors and 16 transistors separately. A comparison is made between the average power consumption and average delay of the different proposed circuits. The power and delay of 14T and 16T are calculated for 1-Bit adder circuit and are then calculated for the implementation system i.e., 2x2 Braun Multiplier and 1-Bit ALU. The proposed adder 1 offered 86.57% and 96.51% improvement in average power and delay respectively. The proposed adder 2 offered 87.09% and 95.94% improvement in average power and delay respectively. This makes the proposed system highly advantageous.