	SORS AND M	IICROCONTROLLER	S
As per Choice	Based Credit Syste	em (CBCS) schemel	S.
(Effective fr	om the academic y	ear 2016 -2017)	
	SEMESTER -	-IV	
Subject Code	15CS44	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	C34445
Total Number of Lecture Hours	50	Exam Hours	80
	CREDITS		03
Course objectives: This course will e	enable students to	04	7 1 1 1 1
<ul> <li>Make familiar with important</li> </ul>	ce and applications	of microprocessors and microco	
• Expose architecture of 8086 r	nicroprocessor and	of interoprocessors and microco	ontrollers
Familiarize instruction set of	ARM processor and	ARM processor	
Module 1	Aidvi processor	A STATE OF THE STA	all f
			Teaching
The x86 microprocessor: Brief h	nistory of the vo	S family I it	Hours
assembly blog allilling	IU Introduction to	D	
I Built I I I I I I I I I I I I I I I I I I I	KIIII 2 htooreass A	1 0 1	
Transfer Instructions, Data Types Flowcharts and Pseudo code	and Data Dofiniti	whore Sample programs, Contro	1
Flowcharts and Pseudo code.	and Data Definiti	ion, Full Segment Definition	,
Text book 1: Ch 1: 1.1 to 1.7, Ch 2:	2.1 to 2.7		100
Module 2	2.1 to 2.7		Line Sub- all
x86: Instructions sets description, Ar	ithmotic and last	•	1371.4
Unsigned Addition and Subtraction Instructions BCD and ASCII converse	Unsigned Make	c instructions and programs	10 Hours
Instructions, BCD and ASCII convers	ion Poteta Instant	olication and Division, Logic	
Programming: Bios INT 10H Progra x86 PC and Interrupt Assignment	amming DOS Inte	ions. INT 21H and INT 10H	
x86 PC and Interrupt Assignment.	mining, DOS Inte	errupt 21H. 8088/86 Interrupts	
Text book 1: Ch 3: 3.1 to 3.5, Ch 4: 4	1 42 Chapter 14	.141	
viouule 5	.1, 4.2 Chapter 14	: 14.1 and 14.2	
Signed Numbers and Strings: Signed			
Memory and Memory interfacing: N	number Arithmetic	0	
	number Arithmetic	c Operations, String operations.	10 Hours
nd ROM, 16-bit memory interfacing		c Operations, String operations.	
me really interfacing.	8255 I/O program		
.86 PC's, programming and interfacing	8255 I/O program	coding, data integrity in RAM nming: I/O addresses MAP of	
86 PC's, programming and interfacing ext book 1: Ch 6: 6.1, 6.2. Ch 10: 10	8255 I/O program	coding, data integrity in RAM nming: I/O addresses MAP of	
286 PC's, programming and interfacing Cext book 1: Ch 6: 6.1, 6.2. Ch 10: 10 Module 4	8255 I/O program the 8255. .2, 10.4, 10.5. Ch 1	coding, data integrity in RAM nming: I/O addresses MAP of 1: 11.1 to 11.4	
186 PC's, programming and interfacing fext book 1: Ch 6: 6.1, 6.2. Ch 10: 10  Module 4  Microprocessors versus Microcontrolle	8255 I/O program the 8255. .2, 10.4, 10.5. Ch 1	nming: I/O addresses MAP of  1: 11.1 to 11.4	
1.86 PC's, programming and interfacing. 1.86 P	8255 I/O program the 8255. .2, 10.4, 10.5. Ch 1	nming: I/O addresses MAP of  1: 11.1 to 11.4  ed Systems: The RISC design	
186 PC's, programming and interfacing Text book 1: Ch 6: 6.1, 6.2. Ch 10: 10  Module 4  Microprocessors versus Microcontrolle hilosophy, The ARM Design Philos ystem Software, ARM Processor Fun	8255 I/O program the 8255. .2, 10.4, 10.5. Ch 1 rs, ARM Embedded ophy, Embedded the	and the coding, data integrity in RAM naming: I/O addresses MAP of 1: 11.1 to 11.4  ed Systems: The RISC design System Hardware, Embedded store.	
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Research, Forth memory interfacing, 186 PC's, programming and interfacing fext book 1: Ch 6: 6.1, 6.2. Ch 10: 10  Module 4  Microprocessors versus Microcontrolle hilosophy, The ARM Design Philosystem Software, ARM Processor Functions, Interruptext book 2:Ch 1:1.1 to 1.4, Ch 2:2.1 to 1.4, Ch 2:2.1 to 1.4 to 1.5	8255 I/O program the 8255. .2, 10.4, 10.5. Ch 1 rs, ARM Embedde ophy, Embedded S indamentals: Regists, and the Vector T	coding, data integrity in RAM nming: I/O addresses MAP of  1: 11.1 to 11.4  ed Systems: The RISC design System Hardware, Embedded sters, Current Program Status Table, Core Extensions	
186 PC's, programming and interfacing. 186 PC's, programm	8255 I/O program the 8255. .2, 10.4, 10.5. Ch 1 rs, ARM Embedded ophy, Embedded indamentals: Regists, and the Vector T	coding, data integrity in RAM nming: I/O addresses MAP of  1: 11.1 to 11.4  ed Systems: The RISC design System Hardware, Embedded sters, Current Program Status Table, Core Extensions	10 Hours
As PC's, programming and interfacing fext book 1: Ch 6: 6.1, 6.2. Ch 10: 10  Module 4  Microprocessors versus Microcontrolle hilosophy, The ARM Design Philosystem Software, ARM Processor Fundamental	8255 I/O program the 8255. 2, 10.4, 10.5. Ch 1 rs, ARM Embedde ophy, Embedded indamentals: Regions, and the Vector Toto 2.5 on Set: Data Program	coding, data integrity in RAM nming: I/O addresses MAP of  1: 11.1 to 11.4  ed Systems: The RISC design System Hardware, Embedded sters, Current Program Status Table, Core Extensions  cessing Instructions, Branch	
186 PC's, programming and interfacing. 186 PC's, programm	8255 I/O program the 8255. 2, 10.4, 10.5. Ch 1  rs, ARM Embedde ophy, Embedded indamentals: Regi ts, and the Vector T to 2.5  on Set: Data Productions, Program tants. Simple program	coding, data integrity in RAM nming: I/O addresses MAP of  1: 11.1 to 11.4  ed Systems: The RISC design System Hardware, Embedded sters, Current Program Status Table, Core Extensions  cessing Instructions, Branch	10 Hours
As PC's, programming and interfacing fext book 1: Ch 6: 6.1, 6.2. Ch 10: 10  Module 4  Microprocessors versus Microcontrolle hilosophy, The ARM Design Philosystem Software, ARM Processor Fundamental	8255 I/O program the 8255. 2, 10.4, 10.5. Ch 1  rs, ARM Embedde ophy, Embedded indamentals: Regints, and the Vector T to 2.5  on Set: Data Productions, Program tants, Simple program tants, Simple program tants, Simple program tants, Simple program	coding, data integrity in RAM nming: I/O addresses MAP of  1: 11.1 to 11.4  ed Systems: The RISC design System Hardware, Embedded sters, Current Program Status Table, Core Extensions  cessing Instructions, Branch Status Register Instructions, amming exercises.	10 Hours

- Differentiate between microprocessors and microcontrollers
- Design and develop assembly language code to solve problems
- Gain the knowledge for interfacing various devices to x86 family and ARM processor
- Demonstrate design of interrupt routines for interfacing devices

## **Graduate Attributes**

- Engineering Knowledge
- Problem Analysis
- Design/Development of Solutions

## Question paper pattern:

The question paper will have ten questions.

There will be 2 questions from each module.

Each question will have questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

## Text Books:

- Muhammad Ali Mazidi, Janice Gillispie Mazidi, Danny Causey, The x86 PC Assembly Language Design and Interfacing, 5<sup>th</sup> Edition, Pearson, 2013.
- ARM system developers guide, Andrew N Sloss, Dominic Symes and Chris Wright, Elsevier, Morgan Kaufman publishers, 2008.

## Reference Books:

- Douglas V. Hall: Microprocessors and Interfacing, Revised 2<sup>nd</sup> Edition, TMH, 2006.
- K. Udaya Kumar & B.S. Umashankar: Advanced Microprocessors & IBM-PC Assembly Language Programming, TMH 2003.
- 3. Ayala: The 8086 Microprocessor: programming and interfacing 1st edition, Cengage Learning
- 4. The Definitive Guide to the ARM Cortex-M3, by Joseph Yiu, 2nd Edition, Newnes, 2009
- 5. The Insider's Guide to the ARM7 based microcontrollers, Hitex Ltd., 1st edition, 2005
- 6. ARM System-on-Chip Architecture, Steve Furber, Second Edition, Pearson, 2015
- Architecture, Programming and Interfacing of Low power Processors- ARM7, Cortex-M and MSP430, Lyla B Das Cengage Learning, 1<sup>st</sup> Edition

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