Analysis, Origin of PERT and CPM, Network, Network Techniques, Need for Network Techniques, Steps in PERT, CPM, Advantages, Limitations and Differences.

(Selected topics from Chapters 20, Text 3). **L1,L2,L3**

Course Outcomes: After studying this course, students will be able to:

1. Understand the fundamental concepts of Management and Entrepreneurship and opportunities in order to setup a business
2. Identify the various organizations' architecture
3. Describe the functions of Managers, Entrepreneurs and their social responsibilities
4. Understand the components in developing a business plan
5. Recognize the various sources of funding and institutions supporting entrepreneurs

Text Books:

1. Principles of Management – P.C Tripathi, P.N Reddy, McGraw Hill Education, 6th Edition, 2017. ISBN-13:978-93-5260-535-4.
2. Entrepreneurship Development Small Business Enterprises- Poornima M Charantimath, Pearson Education 2008, ISBN 978-81-7758-260-4.
3. Dynamics of Entrepreneurial Development and Management by Vasant Desai. HPH 2007, ISBN: 978-81-8488-801-2.
4. Robert D. Hisrich, Mathew J. Manimala, Michael P Peters and Dean A. Shepherd, "Entrepreneurship", 8th Edition, Tata Mc-Graw Hill Publishing Co.Ltd.- New Delhi, 2012

Reference Book:

1. Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93-392-2286-4.

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DIGITAL SIGNAL PROCESSING

Course Code : **18EC52**	CIE Marks : 40
Lecture Hours/Week : 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)	Exam Hours : 03
CREDITS : 04	

Course Learning Objectives: This course will enable students to

- Understand the frequency domain sampling and reconstruction of discrete time signals.
- Study the properties and the development of efficient algorithms for the computation of DFT.
- Realization of FIR and IIR filters in different structural forms.
- Learn the procedures to design of IIR filters from the analog filters using impulse invariance and bilinear transformation.
- Study the different windows used in the design of FIR filters and design appropriate filters based on the specifications.
- Understand the architecture and working of DSP processor

Module-1

Discrete Fourier Transforms (DFT): Frequency domain sampling and Reconstruction of Discrete Time Signals, The Discrete Fourier Transform, DFT as a linear transformation, Properties of the DFT: Periodicity, Linearity and Symmetry properties, Multiplication of two DFTs and Circular Convolution, Additional DFT properties.

[Text 1], **L1,L2,L3**

Module-2

Linear filtering methods based on the DFT: Use of DFT in Linear Filtering, Filtering of Long data Sequences.

Fast-Fourier-Transform (FFT) algorithms: Efficient Computation of the DFT: Radix-2 FFT algorithms for the computation of DFT and IDFT–decimation-in-time and decimation-in-frequency algorithms.

[Text 1], **L1,L2, L3**

Module-3

Design of FIR Filters: Characteristics of practical frequency–selective filters, Symmetric and Antisymmetric FIR filters, Design of Linear-phase FIR filters using windows - Rectangular, Hamming, Hanning, Bartlett windows. Design of FIR filters using frequency sampling method. Structure for FIR Systems: Direct form, Cascade form and Lattice structures.

[Text1], **L1, L2, L3**

Module-4

IIR Filter Design: Infinite Impulse response Filter Format, Bilinear Transformation Design Method, Analog Filters using Lowpass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth Filter Design using BLT. Realization of IIR Filters in Direct form I and II.

[Text 2], L1,L2,L3

Module-5

Digital Signal Processors: DSP Architecture, DSP Hardware Units, Fixed point format, Floating point Format, IEEE Floating point formats, Fixed point digital signal processors, Floating point processors, FIR and IIR filter implementations in Fixed point systems.

[Text 2], L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

1. Determine response of LTI systems using time domain and DFT techniques.
2. Compute DFT of real and complex discrete time signals.
3. Compute DFT using FFT algorithms and linear filtering approach.
4. Design and realize FIR and IIR digital filters.
5. Understand the DSP processor architecture.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60

Text Book:

1. Proakis & Manolakis, "Digital Signal Processing – Principles Algorithms & Applications", 4th Edition, Pearson education, New Delhi, 2007. ISBN: 81-317-1000-9.
2. Li Tan, Jean Jiang, "Digital Signal processing – Fundamentals and Applications", Academic Press, 2013, ISBN: 978-0-12-415893.

Reference Books:

1. Sanjit K Mitra, "Digital Signal Processing, A Computer Based Approach", 4th Edition, McGraw Hill Education, 2013,
2. Oppenheim & Schaffer, "Discrete Time Signal Processing" , PHI, 2003.
3. D.Ganesh Rao and Vineeth P Gejji, "Digital Signal Processing" Cengage India Private Limited, 2017, ISBN: 9386858231

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PRINCIPLES OF COMMUNICATION SYSTEMS

Course Code : **18EC53**	CIE Marks : 40
Lecture Hours/Week : 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)	Exam Hours : 03
CREDITS : 04	

Course Learning Objectives: This course will enable students to

- Understand and analyse concepts of Analog Modulation schemes viz; AM, FM, Low pass sampling and Quantization as a random process.
- Understand and analyse concepts digitization of signals viz; sampling, quantizing and encoding.
- Evolve the concept of SNR in the presence of channel induced noise and study Demodulation of analog modulated signals.
- Evolve the concept of quantization noise for sampled and encoded signals and study the concepts of reconstruction from these samples at a receiver.

Module-1

AMPLITUDE MODULATION: Introduction, Amplitude Modulation: Time & Frequency Domain description, Switching modulator, Envelop detector. **(3.1 – 3.2 in Text)**

DOUBLE SIDE BAND-SUPPRESSED CARRIER MODULATION: Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing. **(3.3 – 3.4 in Text)**

SINGLE SIDE–BAND AND VESTIGIAL SIDEBAND METHODS OF MODULATION: SSB Modulation, VSB Modulation, Frequency Translation, Frequency- Division Multiplexing,Theme Example: VSB Transmission of Analog and Digital Television. **(3.5 – 3.8 in Text)**

L1, L2, L3

Module-2

ANGLE MODULATION: Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM, Transmission bandwidth of FM Signals, Generation of FM Signals, Demodulation of FM Signals, FM Stereo Multiplexing, Phase–Locked Loop: Nonlinear model of PLL, Linear model of PLL, Nonlinear Effects in FM Systems. The Superheterodyne Receiver **(4.1 – 4.6 of Text)**

L1, L2, L3

Module-3

[Review of Mean, Correlation and Covariance functions of Random Processes. ***(No questions to be set on these topics)]***

NOISE - Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth **(5.10 in Text)**

NOISE IN ANALOG MODULATION: Introduction, Receiver Model, Noise in DSB-SC receivers. Noise in AM receivers, Threshold effect, Noise in FM receivers, Capture effect, FM threshold effect, FM threshold reduction, Pre-emphasis and De-emphasis in FM **(6.1 – 6.6 in Text)**

L1,L2,L3

Module-4

SAMPLING AND QUANTIZATION: Introduction, Why Digitize Analog Sources?, The Low pass Sampling process Pulse Amplitude Modulation. Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves.**(7.1 – 7.7 in Text)**

L1,L2,L3

Module-5

SAMPLING AND QUANTIZATION (Contd): The Quantization Random Process, Quantization Noise, Pulse–Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding, Filtering, Multiplexing; Delta Modulation **(7.8 – 7.10 in Text)**,

Application examples - (a) Video + MPEG **(7.11 in Text)** and (b) Vocoders **(refer Section 6.8 of Reference Book 1)**.

L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Analyze and compute performance of AM and FM modulation in the presence of noise at the receiver.
2. Analyze and compute performance of digital formatting processes with quantization noise.
3. Multiplex digitally formatted signals at Transmitter.
4. Demultiplex the signals and reconstruct digitally formatted signals at the receiver.
5. Design /Demonstrate the use of digital formatting in Multiplexers, Vocoders and Video transmission.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.

- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. "Communication Systems", Simon Haykin & Moher, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.

Reference Books:

1. Modern Digital and Analog Communication Systems, B. P. Lathi, Oxford University Press, 4th edition.
2. An Introduction to Analog and Digital Communication, Simon Haykin, John Wiley India Pvt. Ltd., 2008, ISBN 978–81–265–3653–5.
3. Principles of Communication Systems, H.Taub & D.L.Schilling, TMH, 2011.
4. Communication Systems, Harold P.E, Samy A. Mahmoud, Lee Elliott Stern, Pearson Edition, 2004.

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INFORMATION THEORY and CODING

Course Code	: **18EC54**	CIE Marks	:40
Lecture Hours/Week	: 3	SEE Marks	:60
Total Number of Lecture Hours : 40 (8 Hrs / Module)		Exam Hours	:03
CREDITS – 03			

Course Learning Objectives: This course will enable students to

- Understand the concept of Entropy, Rate of information and order of the source with reference to dependent and independent source.
- Study various source encoding algorithms.
- Model discrete & continuous communication channels.
- Study various error control coding algorithms.

Module-1

Information Theory: Introduction, Measure of information, Information content of message, Average Information content of symbols in Long Independent sequences, Average Information content of symbols in Long dependent seqùences, Markov Statistical Model for Information Sources, Entropy and Information rate of Markoff Sources

(Section 4.1, 4.2 of Text 1) **L1, L2,L3**

Module-2

Source Coding: Encoding of the Source Output, Shannon's Encoding Algorithm**(Sections 4.3, 4.3.1 of Text 1),** Shannon Fano Encoding Algorithm **(Section 2.15 of Reference Book 4)**

Source coding theorem, Prefix Codes, Kraft McMillan Inequality property – KMI, Huffman codes **(Section 2.2 of Text 2)**

L1, L2, L3

Module-3

Information Channels: Communication Channels, Discrete Communication channels Channel Matrix, Joint probabilty Matrix, Binary Symmetric Channel, System Entropies. **(Section 4.4, 4.5, 4.51,4.5.2 of Text 1)**

Mutual Information, Channel Capacity, Channel Capacity of Binary Symmetric Channel, **(Section 2.5, 2.6 of Text 2)**

Binary Erasure Channel, Muroga's Theorem **(Section 2.27, 2.28 of Reference Book 4)**

L1, L2, L3

Module-4

Error Control Coding:
Introduction, Examples of Error control coding, methods of Controlling Errors, Types of Errors, types of Codes, Linear Block Codes: matrix description of Linear Block Codes, Error detection & Correction capabilities of Linear Block Codes, Single error correction Hamming code, Table lookup Decoding using Standard Array.

Binary Cyclic Codes: Algebraic Structure of Cyclic Codes, Encoding using an (n-k) Bit Shift register, Syndrome Calculation, Error Detection and Correction **(Sections 9.1, 9.2,9.3,9.3.1,9.3.2,9.3.3 of Text 1)** ,

L1, L2, L3

Module-5

Convolution Codes: Convolution Encoder, Time domain approach, Transform domain approach, Code Tree, Trellis and State Diagram, The Viterbi Algorithm) **(Section 8.5 – Articles 1, 2 and 3, 8.6- Article 1 of Text 2),**

L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

1. Explain concept of Dependent & Independent Source, measure of information, Entropy, Rate of Information and Order of a source
2. Represent the information using Shannon Encoding, Shannon Fano, Prefix and Huffman Encoding Algorithms
3. Model the continuous and discrete communication channels using input, output and joint probabilities
4. Determine a codeword comprising of the check bits computed using Linear Block codes, cyclic codes & convolutional codes
5. Design the encoding and decoding circuits for Linear Block codes, cyclic codes, convolutional codes, BCH and Golay codes.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Digital and Analog Communication Systems, K. Sam Shanmugam, John Wiley India Pvt. Ltd, 1996.
2. Digital Communication, Simon Haykin, John Wiley India Pvt. Ltd, 2008.

Reference Books:

1. ITC and Cryptography, Ranjan Bose, TMH, II edition, 2007
2. Principles of Digital Communication, J. Das, S. K. Mullick, P. K. Chatterjee, Wiley, 1986 - Technology & Engineering
3. Digital Communications – Fundamentals and Applications, Bernard Sklar, Second Edition, Pearson Education, 2016, ISBN: 9780134724058.
4. Information Theory and Coding, HariBhat, Ganesh Rao, Cengage, 2017.
5. Error Correction Coding, Todd K Moon, Wiley Std. Edition, 2006

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ELECTROMAGNETIC WAVES

Course Code	: 18EC55	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (8 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Study the different coordinate systems, Physical significance of Divergence, Curl and Gradient.
- Understand the applications of Coulomb's law and Gauss law to different charge distributions and the applications of Laplace's and Poisson's Equations to solve real time problems on capacitance of different charge distributions.
- Understand the physical significance of Biot-Savart's, Ampere's Law and Stokes' theorem for different current distributions.
- Infer the effects of magnetic forces, materials and inductance.
- Know the physical interpretation of Maxwell's equations and applications for Plane waves for their behavior in different media.
- Acquire knowledge of Poynting theorem and its application of power flow.

Module-1

Revision of Vector Calculus – **(Text 1: Chapter 1)**

Coulomb's Law, Electric Field Intensity and Flux density: Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge distribution, Field of a line charge, Field due to Sheet of charge, Electric flux density, Numerical Problems. **(Text: Chapter 2.1 to 2.5, 3.1)**

L1, L2, L3

Module-2

Gauss's law and Divergence: Gauss law, Application of Gauss law to point charge, line charge, Surface charge and volume charge, Point (differential) form of Gauss law, Divergence. Maxwell's First equation (Electrostatics), Vector Operator ∇ and divergence theorem, Numerical Problems **(Text: Chapter 3.2 to 3.7).**

Energy, Potential and Conductors: Energy expended or work done in moving a point charge in an electric field, The line integral, Definition of potential difference and potential, The potential field of point charge, Potential gradient, Numerical Problems **(Text: Chapter 4.1 to 4.4 and 4.6).** Current and Current density, Continuity of current. **(Text: Chapter 5.1, 5.2)**

L1, L2, L3

Module-3

Poisson's and Laplace's Equations: Derivation of Poisson's and Laplace's Equations, Uniqueness theorem, Examples of the solution of Laplace's equation, Numerical problems on Laplace equation **(Text: Chapter 7.1 to 7.3)**

Steady Magnetic Field: Biot-Savart Law, Ampere's circuital law, Curl, Stokes' theorem, Magnetic flux and magnetic flux density, Basic concepts Scalar and Vector Magnetic Potentials, Numerical problems. **(Text: Chapter 8.1 to 8.6)**

L1, L2, L3

Module-4

Magnetic Forces: Force on a moving charge, differential current elements, Force between differential current elements, Numerical problems **(Text: Chapter 9.1 to 9.3).**

Magnetic Materials: Magnetization and permeability, Magnetic boundary conditions, The magnetic circuit, Potential energy and forces on magnetic materials, Inductance and mutual reactance, Numerical problems **(Text: Chapter 9.6 to 9.7).**

Faraday' law of Electromagnetic Induction –Integral form and Point form, Numerical problems **(Text: Chapter 10.1)**

L1, L2, L3

Module-5

Maxwell's equations Continuity equation, Inconsistency of Ampere's law with continuity equation, displacement current, Conduction current, Derivation of Maxwell's equations in point form, and integral form, Maxwell's equations for different media, Numerical problems **(Text: Chapter 10.2 to 10.4)**

Uniform Plane Wave: Plane wave, Uniform plane wave, Derivation of plane wave equations from Maxwell's equations, Solution of wave equation for perfect dielectric, Relation between E and H, Wave propagation in free space, Solution of wave equation for sinusoidal excitation, wave propagation in any conducting media (γ, α, β, η) and good conductors, Skin effect or Depth of penetration, Poynting's theorem and wave power, Numerical problems. **(Text: Chapter 12.1 to 12.4)**

L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

1. Evaluate problems on electrostatic force, electric field due to point, linear, volume charges by applying conventional methods and charge in a volume.
2. Apply Gauss law to evaluate Electric fields due to different charge distributions and Volume Charge distribution by using Divergence Theorem.

3. Determine potential and energy with respect to point charge and capacitance using Laplace equation and Apply Biot-Savart's and Ampere's laws for evaluating Magnetic field for different current configurations
4. Calculate magnetic force, potential energy and Magnetization with respect to magnetic materials and voltage induced in electric circuits.
5. Apply Maxwell's equations for time varying fields, EM waves in free space and conductors and Evaluate power associated with EM waves using Poynting theorem

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. W.H. Hayt and J.A. Buck, —Engineering Electromagnetics, 8th Edition, Tata McGraw-Hill, 2014, ISBN-978-93-392-0327-6.

Reference Books:

1. Elements of Electromagnetics – Matthew N.O., Sadiku, Oxford university press, 4th Edn.
2. Electromagnetic Waves and Radiating systems – E. C. Jordan and K.G. Balmain, PHI, 2nd Edn.
3. Electromagnetics- Joseph Edminister, Schaum Outline Series, McGraw Hill.
4. Fundamentals of Electromagnetics for Engineering - N. Narayana Rao, Pearson.

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Verilog HDL

Course Code	: 18EC56	CIE Marks	:40
Lecture Hours/Week	: 03	SEE Marks	:60
Total Number of Lecture Hours	: 40 (08 Hrs/Module)	Exam Hours	:03
	CREDITS–03		

Course Learning Objectives: This course will enable students to:

- Learn different Verilog HDL constructs.
- Familiarize the different levels of abstraction in Verilog.
- Understand Verilog Tasks, Functions and Directives.
- Understand timing and delay Simulation.
- Understand the concept of logic synthesis and its impact in verification

Module 1

Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL-flow, why Verilog HDL?, trends in HDLs.
Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block. **L1,L2,L3**

Module 2

Basic Concepts: Lexical conventions, data types, system tasks, compiler directives.
Modules and Ports: Module definition, port declaration, connecting ports, hierarchical name referencing **L1,L2,L3**

Module 3

Gate-Level Modeling: Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays.
Dataflow Modeling: Continuous assignments, delay specification, expressions, operators, operands, operator types. **L1,L2,L3**

Module 4

Behavioral Modeling: Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks.
Tasks and Functions: Differences between tasks and functions, declaration, invocation, automatic tasks and functions. **L1,L2,L3**

Module 5

Useful Modeling Techniques: Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks.
Logic Synthesis with Verilog: Logic Synthesis, Impact of logic synthesis, Verilog HDL Synthesis, Synthesis design flow, Verification of Gate-Level Netlist. **(Chapter 14 till 14.5 of Text).** **L1,L2,L3**

Course Outcomes: At the end of this course, students will be able to

1. Write Verilog programs in gate, dataflow (RTL), behavioral and switch modeling levels of Abstraction.
2. Design and verify the functionality of digital circuit/system using test benches.
3. Identify the suitable Abstraction level for a particular digital design.
4. Write the programs more effectively using Verilog tasks, functions and directives.
5. Perform timing and delay Simulation and Interpret the various constructs in logic synthesis.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Samir Palnitkar, **"Verilog HDL: A Guide to Digital Design and Synthesis"**, Pearson Education, Second Edition.

Reference Books:

1. Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer Science+Business Media, LLC, Fifth edition.
2. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.
3. Padmanabhan, Tripura Sundari, "Design through Verilog HDL", Wiley, 2016 or earlier.

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DIGITAL SIGNAL PROCESSING LABORATORY

Course Code : **18ECL57**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to

- Simulate discrete time signals and verification of sampling theorem.
- Compute the DFT for a discrete signal and verification of its properties using MATLAB.
- Find solution to the difference equations and computation of convolution and correlation along with the verification of properties.
- Compute and display the filtering operations and compare with the theoretical values.
- Implement the DSP computations on DSP hardware and verify the result.

Laboratory Experiments

Following Experiments to be done using MATLAB / SCILAB / OCTAVE or equivalent:

1. Verification of sampling theorem (use interpolation function).
2. Linear and circular convolution of two given sequences, Commutative, distributive and associative property of convolution.
3. Auto and cross correlation of two sequences and verification of their properties
4. Solving a given difference equation.
5. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum (using DFT equation and verify it by built-in routine).
6. (i) Verification of DFT properties (like Linearity and Parseval's theorem, etc.)
   (ii) DFT computation of square pulse and Sinc function etc.

7. Design and implementation of Low pass and High pass FIR filter to meet the desired specifications (using different window techniques) and test the filter with an audio file. Plot the spectrum of audio signal before and after filtering.

8. Design and implementation of a digital IIR filter (Low pass and High pass) to meet given specifications and test with an audio file. Plot the spectrum of audio signal before and after filtering.

Following Experiments to be done using DSP kit

9. Obtain the Linear convolution of two sequences.
10. Compute Circular convolution of two sequences.
11. Compute the N-point DFT of a given sequence.
12. Determine the Impulse response of first order and second order system.
13. Generation of sine wave and standard test signals

Course Outcomes:

On the completion of this laboratory course, the students will be able to:

1. Understand the concepts of analog to digital conversion of signals and frequency domain sampling of signals.
2. Model the discrete time signals and systems and verify its properties and results.
3. Implement discrete computations using DSP processor and verify the results.
4. Realize the digital filters using a simulation tool and analyze the response of the filter for an audio signal.
5. Write programs using Matlab / Scilab/Octave to illustrate DSP concepts.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
3. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Reference Books:

1. Vinay K Ingle, John G Proakis, Digital Signal Processing using MATLAB, Fourth Edition, Cengage India Private Limited, 2017.

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HDL LABORATORY

Course Code : **18ECL58**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:

- Familiarize with the CAD tool to write HDL programs.
- Understand simulation and synthesis of digital design.
- Program FPGAs/CPLDs to synthesize the digital designs.
- Interface hardware to programmable ICs through I/O ports.
- Choose either Verilog or VHDL for a given Abstraction level.

Note: Programming can be done using any compiler. Download the programs on a FPGA/CPLD board and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

PART A

1. Write Verilog program for the following combinational design along with test bench to verify the design:
   a. 2 to 4 decoder realization using NAND gates only (structural model)
   b. 8 to 3 encoder with priority and without priority (behavioural model)
   c. 8 to 1 multiplexer using case statement and if statements
   d. 4-bit binary to gray converter using 1-bit gray to binary converter 1-bit adder and subtractor
2. Model in Verilog for a full adder and add functionality to perform logical operations of XOR, XNOR, AND and OR gates. Write test bench with appropriate input patterns to verify the modeled behaviour.
3. Verilog 32-bit ALU shown in figure below and verify the functionality of ALU by selecting appropriate test patterns. The functionality of the ALU is presented in Table 1.
   a. Write test bench to verify the functionality of the ALU considering all possible input patterns
   b. The enable signal will set the output to required functions if enabled, if disabled all the outputs are set to tri-state
   c. The acknowledge signal is set high after every operation is complete

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B. E. 2018 Scheme Sixth Semester Syllabus (EC)

Choice Based Credit System (CBCS) and Outcome Based Education (OBE)

SEMESTER – VI

DIGITAL COMMUNICATION

Course Code	: 18EC61	CIE Marks : 40
Lecture Hours/Week	: 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)		Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to:

- Understand the mathematical representation of signal, symbol, and noise.
- Understand the concept of signal processing of digital data and signal conversion to symbols at the transmitter and receiver.
- Compute performance metrics and parameters for symbol processing and recovery in ideal and corrupted channel conditions.
- Compute performance parameters and mitigate channel induced impediments in corrupted channel conditions.

Module-1

Bandpass Signal to Equivalent Low pass: Hilbert Transform, Pre-envelopes, Complex envelopes, Canonical representation of bandpass signals, Complex low pass representation of bandpass systems, Complex representation of band pass signals and systems **(Text 1: 2.8, 2.9, 2.10, 2.11, 2.12, 2.13).**

Line codes: Unipolar, Polar, Bipolar (AMI) and Manchester code and their power spectral densities **(Text 1: Ch 6.10).**
Overview of HDB3, B3ZS, B6ZS **(Ref. 1: 7.2)**

L1,L2,L3

Module-2

Signaling over AWGN Channels- Introduction, Geometric representation of signals, Gram-Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel, Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver **(Text 1: 7.1, 7.2, 7.3, 7.4).**

L1,L2,L3

Module – 3

Digital Modulation Techniques: Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M–ary PSK, M–ary QAM **(Relevant topics in Text 1 of 7.6, 7.7).**

Frequency shift keying techniques using Coherent detection: BFSK generation, detection and error probability **(Relevant topics in Text 1 of 7.8).**
Non coherent orthogonal modulation techniques: BFSK, DPSK Symbol representation, Block diagrams treatment of Transmitter and Receiver, Probability of error (without derivation of probability of error equation) **(Text 1: 7.11, 7.12. 7.13).**

L1,L2,L3

Module-4

Communication through Band Limited Channels: Digital Transmission through Band limited channels: Digital PAM Transmission through Band limited Channels, Signal design for Band limited Channels: Design of band limited signals for zero ISI–The Nyquist Criterion (statement only), Design of band limited signals with controlled ISI-Partial Response signals, Probability of error for detection of Digital PAM: Probability of error for detection of Digital PAM with Zero ISI, Symbol–by–Symbol detection of data with controlled ISI **(Text 2: 9.1, 9.2, 9.3.1, 9.3.2).**
Channel Equalization: Linear Equalizers (ZFE, MMSE), **(Text 2: 9.4.2).**

L1,L2,L3

Module-5

Principles of Spread Spectrum: Spread Spectrum Communication Systems: Model of a Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Systems, Effect of De-spreading on a narrowband Interference, Probability of error (statement only), Some applications of DS Spread Spectrum Signals, Generation of PN Sequences, Frequency Hopped Spread Spectrum, CDMA based on IS-95 **(Text 2: 11.3.1, 11.3.2, 11.3.3, 11.3.4, 11.3.5, 11.4.2).**

L1,L2,L3

Course Outcomes: At the end of the course, the students will be able to:

1. Associate and apply the concepts of Bandpass sampling to well specified signals and channels.
2. Analyze and compute performance parameters and transfer rates for low pass and bandpass symbol under ideal and corrupted non band limited channels.
3. Test and validate symbol processing and performance parameters at the receiver under ideal and corrupted bandlimited channels.

4. Demonstrate that bandpass signals subjected to corruption and distortion in a bandlimited channel can be processed at the receiver to meet specified performance criteria.
5. Understand the principles of spread spectrum communications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN 978-0-471-64735-5.
2. John G Proakis and Masoud Salehi, "Fundamentals of Communication Systems", 2014 Edition, Pearson Education, ISBN 978-8-131-70573-5.

Reference Books:

1. B.P.Lathi and Zhi Ding, "Modern Digital and Analog communication Systems", Oxford University Press, 4th Edition, 2010, ISBN: 978-0-198-07380-2.
2. Ian A Glover and Peter M Grant, "Digital Communications", Pearson Education, Third Edition, 2010, ISBN 978-0-273-71830-7.
3. Bernard Sklar and Ray, "Digital Communications - Fundamentals and Applications", Pearson Education, Third Edition, 2014, ISBN: 978-81-317-2092-9.

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EMBEDDED SYSTEMS

Course Code	: 18EC62	CIE Marks : 40
Lecture Hours/Week	: 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)		Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to:

- Explain the architectural features and instructions of 32 bit microcontroller -ARM Cortex M3.
- Develop Programs using the various instructions of ARM Cortex M3 and C language for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Develop the hardware software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

Module 1

ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence **(Text 1: Ch-1, 2, 3)**

L1,L2

Module 2

ARM Cortex M3 Instruction Sets and Programming: Assembly basics, Instruction list and description, Thumb and ARM instructions, Special instructions, Useful instructions, CMSIS, Assembly and C language Programming **(Text 1: Ch-4, Ch-10.1 to 10.6)**

L1,L2,L3

Module 3

Embedded System Components: Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Elements of an Embedded System (Block diagram and explanation), Differences between RISC and CISC, Harvard and Princeton, Big and Little Endian formats, Memory (ROM and RAM types), Sensors, Actuators, Optocoupler, Communication Interfaces (I2C, SPI, IrDA, Bluetooth, Wi-Fi, Zigbee only)

(Text 2: All the Topics from Ch-1 and Ch-2 (Fig and explanation before 2.1) 2.1.1.6 to 2.1.1.8, 2.2 to 2.2.2.3, 2.3 to 2.3.2, 2.3.3.3, selected topics of 2.4.1 and 2.4.2 only).

L1, L2

Module 4

Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modeling (excluding UML), Embedded firmware design and development (excluding C language). **Text 2: Ch-3, Ch-4 (4.1, 4.2.1 and 4.2.2 only), Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)**

L1,L2,L3

Module 5

RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques **(Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch-12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)**

L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.
2. Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
3. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
4. Develop the hardware software co-design and firmware design approaches.
5. Explain the need of real time operating system for embedded system applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", 2nd Edition, Newnes, (Elsevier), 2010.
2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2nd Edition.

Reference Books:

1. James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008, ISBN: 978-0-471-72180-2.
2. Yifeng Zhu, "Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C", 2nd Ed. Man Press LLC ©2015 ISBN: 0982692633 9780982692639.
3. K.V. K. K Prasad, Embedded Real Time Systems, Dreamtech publications, 2003.
4. Rajkamal, Embedded Systems, 2nd Edition, McGraw hill Publications, 2010.

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MICROWAVE and ANTENNAS

Course Code	: 18EC63	CIE Marks : 40
Lecture Hours/Week	: 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)		Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to:

- Describe the microwave properties and its transmission media
- Describe microwave devices for several applications
- Understand the basics of antenna theory
- Select antennas for specific applications

Module 1

Microwave Tubes: Introduction, Reflex Klystron Oscillator, Mechanism of Oscillations, Modes of Oscillations, Mode Curve (Qualitative Analysis only). **(Text 1: 9.1, 9.2.1)**

Microwave Transmission Lines: Microwave Frequencies, Microwave devices, Microwave Systems, Transmission Line equations and solutions, Reflection Coefficient and Transmission Coefficient, Standing Wave and Standing Wave Ratio, Smith Chart, Single Stub matching.
(Text 2: 0.1, 0.2, 0.3, 3.1, 3.2, 3.3, 3.5, 3.6 Except Double stub matching)
L1,L2

Module 2

Microwave Network theory: Introduction, Symmetrical Z and Y-Parameters for reciprocal Networks, S matrix representation of Multi-Port Networks. **(Text1: 6.1, 6.2, 6.3)**

Microwave Passive Devices: Coaxial Connectors and Adapters, Attenuators, Phase Shifters, Waveguide Tees, Magic tees.
(Text 1: 6.4.2,6.4.14, 6.4.15, 6.4.16) **L1,L2**

Module 3

Strip Lines: Introduction, Micro Strip lines, Parallel Strip lines, Coplanar Strip lines, Shielded Strip Lines. **(Text 2: 11.1, 11.2, 11.3, 11.4)**

Antenna Basics: Introduction, Basic Antenna Parameters, Patterns, Beam Area, Radiation Intensity, Beam Efficiency, Directivity and Gain, Antenna Apertures, Effective Height, Radio Communication Link, Antenna Field Zones. **(Text 3: 2.1 - 2.7, 2.9 – 2.11, 2.13)** **L1,L2,L3**

Module 4

Point Sources and Arrays: Introduction, Point Sources, Power Patterns, Power Theorem, Radiation Intensity, Arrays of two isotropic point sources, Linear Arrays of n Isotropic Point Sources of equal Amplitude and Spacing.
(Text 3: 5.1 – 5.6, 5.9, 5.13)

Electric Dipoles: Introduction, Short Electric Dipole, Fields of a Short Dipole, Radiation Resistance of a Short Electric Dipole, Thin Linear Antenna (Field Analyses)
(Text 3: 6.1 - 6.5)

L1,L2,L3,L4

Module 5

Loop and Horn Antenna: Introduction, Small loop, The Loop Antenna General Case, The Loop Antenna as a special case, Radiation resistance of loops, Directivity of Circular Loop Antennas with uniform current, Horn antennas Rectangular Horn Antennas.
(Text 3: 7.1, 7.2, 7.4, 7.6, 7.7, 7.8, 7.19, 7.20)

Antenna Types: The Helix geometry, Helix modes, Practical Design considerations for the mono-filar axial mode Helical Antenna, Yagi-Uda array, Parabolic reflector
(Text 3: 8.3, 8.4, 8.5, 8.8, 9.5)

L1,L2,L3

Course outcomes: At the end of the course students will be able to:

1. Describe the use and advantages of microwave transmission
2. Analyze various parameters related to microwave transmission lines and waveguides
3. Identify microwave devices for several applications
4. Analyze various antenna parameters necessary for building a RF system
5. Recommend various antenna configurations according to the applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. **Microwave Engineering** – Annapurna Das, Sisir K Das, TMH, Publication, 2nd, 2010.
2. **Microwave Devices and circuits**- Samuel Y Liao, Pearson Education
3. **Antennas and Wave Propagation**- John D. Krauss, Ronald J Marhefka, Ahmad S Khan, 4th Edition, McGraw Hill Education, 2013

Reference Books:

1. **Microwave Engineering** - David M Pozar, John Wiley India Pvt. Ltd., 3rd Edn, 2008.
2. **Microwave Engineering** – Sushrut Das, Oxford Higher Education, 2nd Edn, 2015
3. **Antennas and Wave Propagation** – Harish and Sachidananda: Oxford University Press, 2007

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EMBEDDED SYSTEMS LABORATORY

Course Code : **18ECL66**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS– 02		

Course Learning Objectives: This course will enable students to:

- Understand the instruction set of ARM Cortex M3, a 32 bit microcontroller and the software tool required for programming in Assembly and C language.
- Program ARM Cortex M3 using the various instructions in assembly level language for different applications.
- Interface external devices and I/O with ARM Cortex M3.
- Develop C language programs and library functions for embedded system applications.

Laboratory Experiments

Conduct the following experiments on an ARM CORTEX M3 evaluation board to learn ALP and using evaluation version of Embedded 'C' & Keil uVision-4 tool/compiler.

PART A:

1. ALP to multiply two 16 bit binary numbers.
2. ALP to find the sum of first 10 integer numbers.
3. ALP to find the number of 0's and 1's in a 32 bit data
4. ALP to find determine whether the given 16 bit is even or odd
5. ALP to write data to RAM

PART B:

6. Display "Hello world" message using internal UART
7. Interface and Control the speed of a DC Motor.
8. Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.
9. Interface a DAC and generate Triangular and Square waveforms.
10. Interface a 4x4 keyboard and display the key code on an LCD.
11. Demonstrate the use of an external interrupt to toggle an LED On/Off.
12. Display the Hex digits 0 to F on a 7-segment LED interface, with an appropriate delay.
13. Measure Ambient temperature using a sensor and SPI ADC IC.

Course outcomes: After studying this course, students will be able to:

1. Understand the instruction set of 32 bit microcontroller ARM Cortex M3, and the software tool required for programming in Assembly and C language.
2. Develop assembly language programs using ARM Cortex M3 for different applications.
3. Interface external devices and I/O with ARM Cortex M3.
4. Develop C language programs and library functions for embedded system applications.
5. Analyze the functions of various peripherals, peripheral registers and power saving modes of ARM Cortex M3

Conduction of Practical Examination:

- One Question from PART A and one Question from PART B to be asked in the examination.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

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COMMUNICATION LABORATORY

Course Code : **18ECL67**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:

- Design and test the communication circuits for different analog modulation schemes.
- Design and demonstrate the digital modulation techniques
- Demonstrate and measure the wave propagation in microstrip antennas
- Characteristics of microstrip devices and measurement of its parameters.
- Understand the probability of error computations of coherent digital modulation schemes.

Laboratory Experiments

PART-A: Expt. 1 to Expt. 5 have to be performed using discrete components.

1. Amplitude Modulation and Demodulation: i) Standard AM, ii)DSBSC (LM741 and LF398 ICs can be used)
2. Frequency modulation and demodulation (IC 8038/2206 can be used)
3. Pulse sampling, flat top sampling and reconstruction
4. Time Division Multiplexing and Demultiplexing of two bandlimited signals.
5. FSK and PSK generation and detection
6. Measurement of frequency, guide wavelength, power, VSWR and attenuation in microwave test bench.
7. Obtain the Radiation Pattern and Measurement of directivity and gain of microstrip dipole and Yagi antennas.
8. Determination of
   a. Coupling and isolation characteristics of microstrip directional coupler.
   b. Resonance characteristics of microstrip ring resonator and computation of dielectric constant of the substrate.
   c. Power division and isolation of microstrip power divider.

PART-B: Simulation Experiments using SCILAB/MATLAB/Simulink or LabVIEW

1. To Simulate NRZ, RZ, half-sinusoid & raised cosine pulses and generate eye diagram for binary polar signaling.
2. Pulse code modulation and demodulation system.

3. Computations of the Probability of bit error for coherent binary ASK, FSK and PSK for an AWGN Channel and compare them with their performance curves.
4. Digital Modulation Schemes i) DPSK Transmitter and Receiver, ii) QPSK Transmitter and Receiver.

Course Outcomes: On the completion of this laboratory course, the students will be able to:

1. Design and test circuits for analog modulation and demodulation schemes viz., AM, FM, etc.
2. Determine the characteristics and response of microwave waveguide.
3. Determine characteristics of microstrip antennas and devices & compute the parameters associated with it.
4. Design and test the digital and analog modulation circuits and display the waveforms.
5. Simulate the digital modulation systems and compare the error performance of basic digital modulation schemes.

Conduct of Practical Examination:

- All laboratory experiments are to be considered for practical examination.
- For examination one question from **PART-A** and one question from **PART-B or** only one question from **PART-B** experiments based on the complexity, to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

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B. E. 2018 Scheme Seventh Semester Syllabus (EC)

Choice Based Credit System (CBCS) and Outcome Based Education (OBE)

SEMESTER – VII
COMPUTER NETWORKS

Course Code	: 18EC71	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs/module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand the layering architecture of OSI reference model and TCP/IP protocol suite.
- Understand the protocols associated with each layer.
- Learn the different networking architectures and their representations.
- Learn the functions and services associated with each layer.

Module-1

Introduction: Data communication: Components, Data representation, Data flow, Networks: Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet.
(1.1,1.2, 1.3(1.3.1to 1.3.4 of Text)
Network Models: Protocol Layering: Scenarios, Principles, Logical Connections, TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP.
(2.1, 2.2, 2.3 of Text) **L1, L2**

Module-2

Data-Link Layer: Introduction: Nodes and Links, Services, Two Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services: Framing, Flow and Error Control, Data Link Layer Protocols: Simple Protocol, Stop and Wait protocol, Piggybacking.
(9.1, 9.2(9.2.1, 9.2.2), 11.1, 11.2of Text)
Media Access Control: Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA.**(12.1 of Text)**
Wired and Wireless LANs: Ethernet Protocol, Standard Ethernet. Introduction to wireless LAN: Architectural Comparison, Characteristics, Access Control.
(13.1, 13.2(13.2.1 to 13.2.5), 15.1 of Text) **L1,L2, L3**

Module-3

Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution, Forwarding of IP Packets: Based on destination Address and Label.
(18.1, 18.2, 18.4, 18.5.1, 18.5.2 of Text)
Network Layer Protocols: Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams. **(19.1of Text).**
Unicast Routing: Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing.
(20.1, 20.2of Text) **L1,L2, L3**

Module-4

Transport Layer: Introduction: Transport Layer Services, Connectionless and Connection oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-Back-N Protocol, Selective repeat protocol. **(23.1, 23.2.1, 23.2.2, 23.2.3, 23.2.4 of Text)**
Transport-Layer Protocols in the Internet:
User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Flow control, Error control, TCP congestion control.
(24.2, 24.3.1, 24.3.2, 24.3.3, 24.3.4, 24.3.5, 24.3.6, 24.3.7, 24.3.8, 24.3.9 of Text) **L1,L2, L3**

Module-5

Application Layer: Introduction: providing services, Application- layer paradigms, Standard Client –Server Protocols: World wide web, Hyper Text Transfer Protocol, FTP: Two connections, Control Connection, Data Connection, Electronic Mail: Architecture, Wed Based Mail, Telnet: Local versus remote logging.Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS, security of DNS.
(25.1, 26.1, 26.2, 26.3, 26.4, 26.6 of Text) **L1, L2**

Course Outcomes: At the end of the course, the students will be able to:

1. Understand the concepts of networking.
2. Describe the various networking architectures.
3. Identify the protocols and services of different layers.
4. Distinguish the basic network configurations and standards associated with each network.
5. Analyze a simple network and measure its parameters.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOK:

- Behrouz A Forouzan, "Data Communications and Networking", 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.

REFERENCE BOOKS:

1. James J Kurose, Keith W Ross, "Computer Networks", Pearson Education.
2. Wayne Tomasi, "Introduction to Data Communication and Networking", Pearson Education.
3. Andrew S Tanenbaum, "Computer Networks", Prentice Hall.
4. William Stallings, "Data and Computer Communications", Prentice Hall.

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VLSI DESIGN

Course Code	:18EC72	CIE Marks	:40
Lecture Hours/Week	:3	SEE Marks	:60
Total Number of Lecture Hours : 40(08 Hrs / Module)		Exam Hours	:03
CREDITS – 03			

Course Learning Objectives: The objectives of the course is to enable students to:

- Impart knowledge of MOS transistor theory and CMOS technologies
- Learn the operation principles and analysis of inverter circuits.
- Design Combinational, sequential and dynamic logic circuits as per the requirements
- Infer the operation of Semiconductors Memory circuits.
- Demonstrate the concepts of CMOS testing

Module-1

Introduction: A Brief History, MOS Transistors, CMOS Logic **(1.1 to 1.4 of TEXT2)**
MOS Transistor Theory: Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics **(2.1, 2.2, 2.4 and 2.5 of TEXT2).,** **L1, L2**

Module-2

Fabrication: CMOS Fabrication and Layout, VLSI Design Flow, Introduction, CMOS Technologies, Layout Design Rules, **(1.5 and 3.1 to 3.3 of TEXT2).**
MOSFET Scaling and Small-Geometry Effects, MOSFET Capacitances **(3.5 to 3.6 of TEXT1),** **L1, L2,**

Module-3

Delay: Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths **(4.1 to 4.5 of TEXT2, except sub-sections 4.3.7, 4.4.5, 4.4.6, 4.5.5 and 4.5.6).**
Combinational Circuit Design: Introduction, Circuit families **(9.1 to 9.2 of TEXT2, except subsection 9.2.4).,** **L1, L2, L3**

Module-4

Sequential Circuit Design: Introduction, Circuit Design for Latches and Flip-Flops **(10.1 and 10.3.1 to 10.3.4 of TEXT2)**
Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques **(9.1, 9.2, 9.4 to 9.5 of TEXT1),** **L1, L2, L3**

Module-5

Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM),
(10.1 to 10.3 of TEXT1)
Testing and Verification: Introduction, Logic Verification Principles, Manufacturing Test Principles, Design for testability
(15.1, 15.3, 15.5 15.6.1 to 15.6.3 of TEXT 2). **L1, L2**

Course outcomes: At the end of the course, the students will be able to:

1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
2. Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
3. Demonstrate ability to design Combinational, sequential and dynamic logic circuits as per the requirements
4. Interpret Memory elements along with timing considerations
5. Interpret testing and testability issues in VLSI Design

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOKS:

1. "CMOS Digital Integrated Circuits: Analysis and Design" - **Sung Mo Kang & Yosuf Leblebici,** Third Edition, Tata McGraw-Hill.
2. **"CMOS VLSI Design- A Circuits and Systems Perspective"-** Neil H. E. Weste and David Money Harris, 4th Edition, Pearson Education.

REFERENCE BOOKS:

1. Adel Sedra and K. C. Smith, "Microelectronics Circuits Theory and Applications", 6th or 7th Edition, Oxford University Press, International Version, 2009.
2. Douglas A Pucknell & Kamran Eshragian, "Basic VLSI Design", PHI 3rd Edition, (original Edition – 1994).
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.

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REAL TIME SYSTEM

Course Code	: 18EC731	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This Course will enable students to:

- Understand the fundamentals of Real-time systems and its classifications.
- Describe the concepts of computer control and hardware components for Real-Time Application.
- Discuss the languages to develop software for Real-Time Applications.
- Explain the concepts of operating system and RTS development methodologies.

Module-1

Introduction to Real-Time Systems: Historical background, Elements of a Computer Control System, RTS- Definition, Classification of Real-time Systems, Time Constraints, Classification of Programs.

Concepts of Computer Control: Introduction, Sequence Control, Loop Control, Supervisory Control, Centralized Computer Control, Hierarchical Systems.

(Text: 1.1 to 1.6 and 2.1 to 2.6), **L1, L2**

Module-2

Computer Hardware Requirements for Real-Time Applications: Introduction, General Purpose Computer, Single Chip Microcomputers and Microcontrollers, Specialized Processors, Process-Related Interfaces, Data Transfer Techniques, Communications, Standard Interface.

(Text: 3.1 to 3.8). **L1, L2**

Module-3

Languages for Real-Time Applications: Introduction, Syntax Layout and Readability, Declaration and Initialization of Variables and Constants, Cutlass, Modularity and Variables, Compilation of Modular Programs, Data types, Control Structures, Exception Handling, Low-level facilities, Co-routines, Interrupts and Device Handling, Concurrency, Real-Time Support, Overview of Real-Time Languages.

(Text: 5.1 to 5.14)., **L1,L2, L3**

Module-4

Operating Systems: Introduction, Real-Time Multi-Tasking OS, Scheduling Strategies, Priority Structures, Task Management, Scheduler and Real-Time

Clock Interrupt Handler, Memory Management, Code Sharing, Resource Control, Task Co-Operation and Communication, Mutual Exclusion.
(Text: 6.1 to 6.11). **L1, L2**

Module-5

Design of RTS – General Introduction: Introduction, Specification Document, Preliminary Design, Single-Program Approach, Foreground/Background System.
RTS Development Methodologies: Introduction, Yourdon Methodology, Ward and Mellor Method, Hately and Pirbhai Method.
(Text: 7.1 to 7.5 and 8.1, 8.2, 8.4,8.5). **L1, L2, L3**

Course Outcomes: At the end of the course, students should be able to:

1. Explain the fundamentals of Real time systems and its classifications.
2. Understand the concepts of computer control and the suitable computer hardware requirements for real-time applications.
3. Describe the operating system concepts and techniques required for real time systems.
4. Develop the software algorithms using suitable languages to meet Real time applications.
5. Apply suitable methodologies to design and develop Real-Time Systems.

Text Book:

- Real-Time Computer Control, Stuart Bennet, 2nd Edn. Pearson Education. 2008.

Reference Books:

1. "Real –Time Systems", C.M. Krishna, Kang G. Shin, McGraw –Hill International Editions, 1997.
2. Real-Time Systems Design and Analysis, Phillip. A. Laplante, second edition, PHI, 2005.
3. Embedded Systems, Raj Kamal, Tata McGraw Hill, India, third edition, 2005.

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SATELLITE COMMUNICATION

Course Code	: 18EC732	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to

- Understand the basic principle of satellite orbits and trajectories.
- Study of electronic systems associated with a satellite and the earth station.
- Understand the various technologies associated with the satellite communication.
- Focus on a communication satellite and the national satellite system.
- Study of satellite applications focusing various domains services such as remote sensing, weather forecasting and navigation.

Module-1

Satellite Orbits and Trajectories: Definition, Basic Principles, Orbital parameters, Injection velocity and satellite trajectory, Types of Satellite orbits, Orbital perturbations, Satellite stabilization, Orbital effects on satellite's performance, Eclipses, Look angles: Azimuth angle, Elevation angle. ,

L1, L2

Module-2

Satellite subsystem: Power supply subsystem, Attitude and Orbit control, Tracking, Telemetry and command subsystem, Payload.

Earth Station: Types of earth station, Architecture, Design considerations, Testing, Earth station Hardware, Satellite tracking.,

L1, L2

Module-3

Multiple Access Techniques: Introduction, FDMA (No derivation), SCPC Systems, MCPC Systems, TDMA, CDMA, SDMA.

Satellite Link Design Fundamentals: Transmission Equation, Satellite Link Parameters, Propagation considerations

L1,L2, L3

Module-4

Communication Satellites: Introduction, Related Applications, Frequency Bands, Payloads, Satellite Vs. Terrestrial Networks, Satellite Telephony, Satellite Television, Satellite radio, Regional satellite Systems, National Satellite Systems.

L1, L2

Module-5

Remote Sensing Satellites: Classification of remote sensing systems, orbits, Payloads, Types of images: Image Classification, Interpretation, Applications.
Weather Forecasting Satellites: Fundamentals, Images, Orbits, Payloads, Applications.
Navigation Satellites: Development of Satellite Navigation Systems, GPS system, Applications.,

L1,L2, L3

Course Outcomes: At the end of the course, the students will be able to:

1. Describe the satellite orbits and its trajectories with the definitions of parameters associated with it.
2. Describe the electronic hardware systems associated with the satellite subsystem and earth station.
3. Describe the communication satellites with the focus on national satellite system.
4. Compute the satellite link parameters under various propagation conditions with the illustration of multiple access techniques.
5. Describe the satellites used for applications in remote sensing, weather forecasting and navigation.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- Anil K. Maini, Varsha Agrawal, Satellite Communications, Wiley India Pvt. Ltd., 2015, ISBN: 978-81-265-2071-8.

Reference Books :

1. Dennis Roddy, Satellite Communications, 4th Edition, McGraw- Hill International edition, 2006
2. Timothy Pratt, Charles Bostian, Jeremy Allnutt, Satellite Communications, 2nd Edition, Wiley India Pvt. Ltd , 2017, ISBN: 978-81-265-0833-4

H. O. D.

DIGITAL IMAGE PROCESSING

Course Code	: 18EC733	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to

- Understand the fundamentals of digital image processing.
- Understand the image transforms used in digital image processing.
- Understand the image enhancement techniques used in digital image processing.
- Understand the image restoration techniques and methods used in digital image processing.
- Understand the Morphological Operations used in digital image processing.

Module1

Digital Image Fundamentals: Whatis Digital Image Processing?, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition.
(Text: Chapter 1 and Chapter 2: Sections 2.1 to 2.2, 2.6.2) **L1,L2**

Module-2

Image Enhancement in the Spatial Domain: Image Sampling and Quantization, Some Basic Relationships Between Pixels, Linear and Nonlinear Operations. Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters
(Text:Chapter2: Sections 2.3 to 2.62, Chapter3: Sections3.2 to 3.6), L1,L2

Module-3

Frequency Domain: Preliminary Concepts, The Discrete Fourier Transform (DFT) of Two Variables, Properties of the 2-DDFT, Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters, Selective Filtering.
(Text: Chapter4: Sections 4.2, 4.5 to 4.10), **L1,L2**

Module-4

Restoration: Noise models, Restorationin the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Linear, Position-Invariant degradations Estimating the Degradation Function, Inverse Filtering, Minimum

Mean Square Error(Wiener) Filtering, Constrained Least Squares Filtering.
(Text: Chapter 5: Sections 5.2, to 5.9) **L1,L2**

Module-5

Morphological Image Processing: Preliminaries, Erosion and Dilation, Opening and Closing.

Image Processing: Color Fundamentals, Color Models, Pseudo color Image Processing.

(Text: Chapter 6: Sections 6.1 to 6.3 Chapter 9: Sections9.1to9.3)
L1,L2

Course Outcomes: At the end of the course, students should be able to:

1. Describe the fundamentals of digital image processing.
2. Understand image formation and the role human visual system plays in perception of gray and color image data.
3. Apply image processing techniques in both the spatial and frequency (Fourier) domains.
4. Design and evaluate image analysis techniques
5. Conduct independent study and analysis of Image Enhancement and restoration techniques.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- Digital Image Processing- Rafel C Gonzalez and Richard E. Woods, PHI 3rd Edition 2010.

Reference Books:

1. Digital Image Processing- S. Jayaraman, S. Esakkirajan,T. Veerakumar, Tata Mc Graw Hill 2014.
2. Fundamentals of Digital Image Processing- A. K. Jain, Pearson 2004.
3. Image Processing analysis and Machine vision with Mind Tap by Milan Sonka and Roger Boile, Cengage Publications, 2018.

D. V.

DSP ALGORITHMS and ARCHITECTURE

Course Code	: 18EC734	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Figure out the knowledge and concepts of digital signal processing techniques.
- Understand the computational building blocks of DSP processors and its speed issues.
- Understand the various addressing modes, peripherals, interrupts and pipelining structure of TMS320C54xx processor.
- Learn how to interface the external devices to TMS320C54xx processor in various modes.
- Understand basic DSP algorithms with their implementation.

Module -1

Introduction to Digital Signal Processing:
Introduction, A Digital Signal – Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation.

Computational Accuracy in DSP Implementations:
Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementation.

L1,L2

Module -2

Architectures for Programmable Digital Signal – Processing Devices:
Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.

L1,L2

Module -3

Programmable Digital Signal Processors:
Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54XX, Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and

Programming, On – Chip Peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor.

L1,L2

Module -4

Implementation of Basic DSP Algorithms:

Introduction, The Q – notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case).

Implementation of FFT Algorithms:

Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit – Reversed Index. Generation & Implementation on the TMS32OC54xx.

L1,L2

Module -5

Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices:

Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA).

Interfacing and Applications of DSP Processors:

Introduction, Synchronous Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System.

L1,L2

Course Outcomes: At the end of this course, students would be able to:

1. Comprehend the knowledge and concepts of digital signal processing techniques.
2. Apply the knowledge of DSP computational building blocks to achieve speed in DSP architecture or processor.
3. Apply knowledge of various types of addressing modes, interrupts, peripherals and pipelining structure of TMS320C54xx processor.
4. Develop basic DSP algorithms using DSP processors.
5. Discuss about synchronous serial interface and multichannel buffered serial port (McBSP) of DSP device and demonstrate the programming of CODEC interfacing.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.

- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- "Digital Signal Processing", Avatar Singh and S. Srinivasan, Thomson Learning, 2004.

Reference Books:

1. "Digital Signal Processing: A practical approach", Ifeachor E. C., Jervis B. W Pearson-Education, PHI, 2002.
2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2nd, 2010
3. "Architectures for Digital Signal Processing", Peter Pirsch John Wiley, 2008

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IoT & WIRELESS SENSOR NETWORKS

Course Code	: 18EC741	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Describe the OSI Model for IoT/M2M Systems.
- Understand the architecture and design principles for device supporting IoT.
- Develop competence in programming for IoT Applications.
- Identify the uplink and downlink communication protocols which best suits the specific application of IoT / WSNs.

Module-1

Overview of Internet of Things: IoT Conceptual Framework, IoT Architectural View, Technology Behind IoT, Sources of IoT,M2M communication, Examples of IoT. Modified OSI Model for the IoT/M2M Systems, data enrichment, data consolidation and device management at IoT/M2M Gateway, web communication protocols used by connected IoT/M2M devices, Message communication protocols (CoAP-SMS, CoAP-MQ, MQTT,XMPP) for IoT/M2M devices. – Refer Chapter 1, 2 and 3 of Text 1.

L1, L2

Module-2

Architecture and Design Principles for IoT: Internet connectivity, Internet-based communication,IPv4, IPv6,6LoWPAN protocol, IP Addressing in the IoT, Application layer protocols: HTTP, HTTPS,FTP,TELNET and ports.

Data Collection, Storage and Computing using a Cloud Platform: Introduction, Cloud computing paradigm for data collection, storage and computing, Cloud service models, IoT Cloud- based data collection, storage and computing services using Nimbits. - Refer Chapter 4 and 6 of Text 1.

L1, L2

Module-3

Prototyping and Designing Software for IoT Applications: Introduction, Prototyping Embedded device software, Programming Embedded Device Arduino Platform using IDE, Reading data from sensors and devices, Devices, Gateways, Internet and Web/Cloud services software development.

Programming MQTT clients and MQTT server. Introduction to IoT privacy

and security. Vulnerabilities, security requirements and threat analysis, IoT Security Tomography and layered attacker model. - Refer Chapter 9 and 10 of Text 1. **L1, L2, L3**

Module-4

Overview of Wireless Sensor Networks:
Challenges for Wireless Sensor Networks, Enabling Technologies for Wireless Sensor Networks.
Architectures: Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes, Operating Systems and Execution Environments, Network Architecture-Sensor Network Scenarios, Optimization Goals and Figures of Merit, Design principles for WSNs, Service interfaces of WSNs Gateway Concepts. - Refer Chapter 1, 2, 3 of Text 2.

L1, L2, L3

Module-5

Communication Protocols:
Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Contention based protocols(CSMA,PAMAS), Schedule based protocols (LEACH, SMACS, TRAMA) Address and Name Management in WSNs, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing, Hierarchical networks by clustering. - Refer Chapter 4, 5, 7 and 11 of Text 2.

L1, L2, L3

Course Outcomes: At the end of the course, students will be able to:

1. Understand choice and application of IoT & M2M communication protocols.
2. Describe Cloud computing and design principles of IoT.
3. Relate to MQTT clients, MQTT server and its programming.
4. Describe the architectures and its communication protocols of WSNs.
5. Identify the uplink and downlink communication protocols associated with specific application of IOT / WSNs

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4sub questions.
- There will be 2 full questions from each module covering all the topics of the module.

- Students will have to answer 5full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Raj Kamal, "Internet of Things-Architecture and design principles", McGraw Hill Education.
2. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless Sensor Networks", John Wiley, 2005.

Reference Books:

1. Feng Zhao & Leonidas J. Guibas, "Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
2. Kazem Sohraby, Daniel Minoli, & Taieb Znati, "Wireless Sensor Networks- Technology, Protocols and Applications", John Wiley, 2007.
3. Anna Hac, "Wireless Sensor Network Designs", John Wiley, 2003.

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VLSI LABORATORY

Course Code : **18ECL77**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:

- Design, model, simulate and verify CMOS digital circuits
- Design layouts and perform physical verification of CMOS digital circuits
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist
- Perform RTL-GDSII flow and understand the stages in ASIC design

Experiments can be conducted using any of the following or equivalent design tools: Cadence/Synopsis/Mentor Graphics/Microwind

Laboratory Experiments

Part – A

Analog Design

Use any VLSI design tools to carry out the experiments, use library files and technology files below 180 nm.

1.a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following:

i. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time period of 20ns and plot the input voltage and output voltage of designed inverter?

ii. From the simulation results compute tpHL, tpLH and td for all three geometrical settings of width?

iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter?

1. b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

2. a) Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 1. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.

2. b) Draw layout of NAND with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

3. a) Capture schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measures the Unity Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB.

3. b) Draw layout of common source amplifier, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

4.a) Capture schematic of two-stage operational amplifier and measure the following:

i. UGB
ii. dB bandwidth
iii. Gain margin and phase margin with and without coupling capacitance
iv. Use the op-amp in the inverting and non-inverting configuration and verify its functionality
v. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations.

4.b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in 4.a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

Part - B

Digital Design

Carry out the experiments using semicustom design flow or ASIC design flow, use technology library 180/90/45nm and below

Note: The experiments can also be carried out using FPGA design flow, it is required to set appropriate constraints in FPGA advanced synthesis options

1. Write verilog code for 4-bit up/down asynchronous reset counter and carry out the following:
   a. Verify the functionality using test bench
   b. Synthesize the design by setting area and timing constraint. Obtain

the gate level netlist, find the critical path and maximum frequency of operation. Record the area requirement in terms of number of cells required and properties of each cell in terms of driving strength, power and area requirement.

c. Perform the above for 32-bit up/down counter and identify the critical path, delay of critical path, and maximum frequency of operation, total number of cells required and total area.

2. Write verilog code for 4-bit adder and verify its functionality using test bench. Synthesize the design by setting proper constraints and obtain the net list. From the report generated identify critical path, maximum delay, total number of cells, power requirement and total area required. Change the constraints and obtain optimum synthesis results.
3. Write verilog code for UART and carry out the following:
   a. Perform functional verification using test bench
   b. Synthesize the design targeting suitable library and by setting area and timing constraints
   c. For various constrains set, tabulate the area, power and delay for the synthesized netlist
   d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints
4. Write verilog code for 32-bit ALU supporting four logical and four arithmetic operations, use case statement and if statement for ALU behavioral modeling.
   a. Perform functional verification using test bench
   b. Synthesize the design targeting suitable library by setting area and timing constraints
   c. For various constrains set, tabulate the area, power and delay for the synthesized netlist
   d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints

   Compare the synthesis results of ALU modeled using IF and CASE statements.
5. Write verilog code for Latch and Flip-flop, Synthesize the design and compare the synthesis report (D, SR, JK).
6. For the synthesized netlist carry out the following for any two above experiments:
   a. Floor planning (automatic), identify the placement of pads
   b. Placement and Routing, record the parameters such as no. of layers used for routing, flip method for placement of standard cells, placement of standard cells, routes of power and ground, and routing of standard cells
   c. Physical verification and record the LVS and DRC reports

d. Perform Back annotation and verify the functionality of the design
e. Generate GDSII and record the number of masks and its color composition

Course Outcomes: On the completion of this laboratory course, the students will be able to:

1. Design and simulate combinational and sequential digital circuits using Verilog HDL
2. Understand the Synthesis process of digital circuits using EDA tool.
3. Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list
4. Design and simulate basic CMOS circuits like inverter, common source amplifier and differential amplifiers.
5. Perform RTL-GDSII flow and understand the stages in ASIC design.

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