CELLULAR MOBILE COMMUNICATIONS

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC651	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course enables students to:

- Understand the application of multi user access in a cellular communication scenario.
- Understand the propagation mechanisms in an urban mobile communications using statistical and empirical models.
- Understand system architecture, call processing protocols and services of GSM, GPRS and EDGE.
- Understand system architecture, call processing protocols and services of CDMA based systems IS95 and CDMA2000.

Module-1	RBT Level
Cellular Concept: Frequency Reuse, Channel Assignment Strategies, Interference and System Capacity, Power Control for Reducing Interference, Trunking and Grade of Service, Improving Capacity in Cellular Systems. **Mobile Radio Propagation:** Large Scale path Loss- Free Space Model, Three basic propagation mechanisms, Practical Link Budget Design using Path Loss Models, Outdoor Propagation Models – Okumura, Hata, PCS Extension to Hata Model (explanations only) (Text 1).	L1, L2
Module-2	
Mobile Radio Propagation: Small-Scale Fading and Multipath: Small scale Multipath Propagation, Impulse Response Model of a Multipath Channel, Small-Scale Multipath Measurements, Parameters of Mobile Multipath Channels, Types of Small-Scale Fading, Rayleigh and Ricean Distributions, Statistical Model for Multipath Fading Channels (Clarke's Model for Flat Fading only).(Text 1)	L1, L2
Module-3	
System Architecture and Addressing: System architecture, The SIM concept, Addressing, Registers and subscriber data, Location registers (HLR and VLR) Security-related registers (AUC and EIR), Subscriber data, Network interfaces and configurations. **Air Interface – GSM Physical Layer:** Logical channels, Physical channels, Synchronization- Frequency and clock synchronization, Adaptive frame synchronization, Mapping of logical onto physical channels, Radio subsystem link control, Channel coding, source coding and speech processing, Source coding and speech processing, Channel coding, Power-up scenario. **GSM Protocols:** Protocol architecture planes, Protocol architecture of the user plane, Protocol architecture of the signaling plane, Signaling at the air interface (Um), Signaling at the A and Abis interfaces, Security-related network functions,	L1, L2

Signaling at the user interface.(Text 2)	
Module-4	
GSM Roaming Scenarios and Handover: Mobile application part interfaces, Location registration and location update, Connection establishment and termination, Handover. (up to 6.4.1 only in Text2) **Services:** Classical GSM services, Popular GSM services: SMS and MMS. **Improved data services in GSM: GPRS, HSCSD and EDGE** GPRS System architecture of GPRS , Services , Session management, mobility management and routing, Protocol architecture, Signaling plane, Interworking with IP networks, Air interface, Authentication and ciphering, Summary of GPRS . HSCSD: Architecture, Air interface, HSCSD resource allocation and capacity issues. EDGE: The EDGE concept, EDGE physical layer, modulation and coding, EDGE: effects on the GSM system architecture, ECSD and EGPRS. (Text 2)	L1, L2
Module-5	
CDMA Technology – Introduction to CDMA,CDMA frequency bands, CDMA Network and System Architecture, CDMA Channel concept, Forward Logical Channels, Reverse logical Channels, CDMA frame format, CDMA System Operations(Initialization/Registration), Call Establishment, CDMA Call handoff,IS-95B,CDMA2000,W-CDMA,UMTS,CDMA data networks, Evolution of CDMA to 3G, CDMA 2000 RAN Components, CDMA 2000 Packet Data Service. (Text 3)	L1, L2

Course outcomes: At the end of the course, the students will be able to:

- Apply the understanding of statistical characterization of urban mobile channels to compute the performance for simple modulation schemes.
- Demonstrate the limitations of GSM, GPRS and CDMA to meet high data rate requirements and limited improvements that are needed.
- Analyze the call process procedure between a calling number and called number for all scenarios in GSM or CDMA based systems.
- Test and validate voice and data call handling for various scenarios in GSM and CDMA systems for national and international interworking situations.

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Books:

1. Theodore Rapport, "Wireless Communications – Principles and Practice", Prentice Hall of India , 2nd Edition, 2007, ISBN 978-8-120-32381-0.
2. Jorg Eberspacher, Hans-Jorg Vogel, Christian Bettstetter, Christian Hartmann,

"GSM– Architecture, Protocols and Services", Wiley,3rd Edition, 2009,ISBN-978-0-470-03070-7.
3. Gary J Mullet, "Introduction To Wireless Telecommunications Systems and Networks", Cengage Learning.

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ADAPTIVE SIGNAL PROCESSING

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC652	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: The objectives of this course are to:

- Introduce to the concept and need of adaptive filters and popular adaptive signal processing algorithms
- Understand the concepts of training and convergence and the trade-off between performance and complexity.
- Introduce to common linear estimation techniques
- Demonstrate applications of adaptive systems to sample problems.
- Introduce inverse adaptive modelling.

Module-1	RBT Level
Adaptive systems: Definitions and characteristics - applications – properties-examples - adaptive linear combiner input signal and weight vectors - performance function-gradient and minimum mean square error - introduction to filtering-smoothing and prediction - linear optimum filtering-orthogonality - Wiener – Hopf equation-performance surface(Chapters 1& 2 of Text).	L1, L2
Module-2	
Searching performance surface-stability and rate of convergence: Learning curve-gradient search - Newton's method - method of steepest descent - comparison - Gradient estimation - performance penalty - variance - excess MSE and time constants – mis-adjustments (Chapters 4& 5 of Text).	L1, L2
Module-3	
LMS algorithm convergence of weight vector: LMS/Newton algorithm - properties - sequential regression algorithm - adaptive recursive filters - random-search algorithms - lattice structure - adaptive filters with orthogonal signals (Chapters 6& 8 of Text).	L1, L2, L3
Module-4	
Applications-adaptive modeling and system identification: Multipath communication channel, geophysical exploration, FIR digital filter synthesis. (Chapter 9 of Text).	L1, L2, L3
Module-5	
Inverse adaptive modeling: Equalization, and deconvolution adaptive equalization of telephone channels-adapting poles and zeros for IIR digital filter synthesis(Chapter 10 of Text).	L1, L2, L3

Course Outcomes: At the end of the course, students should be able to:

- Devise filtering solutions for optimising the cost function indicating error in estimation of parameters and appreciate the need for adaptation in design.
- Evaluate the performance of various methods for designing adaptive filters

through estimation of different parameters of stationary random process clearly considering practical application specifications.

- Analyse convergence and stability issues associated with adaptive filter design and come up with optimum solutions for real life applications taking care of requirements in terms of complexity and accuracy.
- Design and implement filtering solutions for applications such as channel equalisation, interference cancelling and prediction considering present day challenges.

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Bernard Widrow and Samuel D. Stearns, "Adaptive Signal Processing", Person Education, 1985.

Reference Books:

1. Simon Haykin, "Adaptive Filter Theory", Pearson Education, 2003.
2. John R. Treichler, C. Richard Johnson, Michael G. Larimore, "Theory and Design of Adaptive Filters", Prentice-Hall of India, 2002.

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ARITIFICAL NEURAL NETWORKS

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC653	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: The objectives of this course are:

- Understand the basics of ANN and comparison with Human brain
- Provide knowledge on Generalization and function approximation and various architectures of building an ANN
- Provide knowledge of reinforcement learning using neural networks
- Provide knowledge of unsupervised learning using neural networks.

Module-1	**RBT Level**
Introduction: Biological Neuron – Artificial Neural Model - Types of activation functions – **Architecture**: Feedforward and Feedback, Convex Sets, Convex Hull and Linear Separability, Non-Linear Separable Problem. XOR Problem, Multilayer Networks. **Learning:** Learning Algorithms, Error correction and Gradient Descent Rules, Learning objective of TLNs, Perceptron Learning Algorithm, Perceptron Convergence Theorem.	L1, L2
Module-2	
Supervised Learning: Perceptron learning and Non Separable sets, α-Least Mean Square Learning, MSE Error surface, Steepest Descent Search, μ-LMS approximate to gradient descent, Application of LMS to Noise Cancelling, Multi-layered Network Architecture, Backpropagation Learning Algorithm, Practical consideration of BP algorithm.	L1, L2, L3
Module-3	
Support Vector Machines and Radial Basis Function: Learning from Examples, Statistical Learning Theory, Support Vector Machines, SVM application to Image Classification, Radial Basis Function Regularization theory, Generalized RBF Networks, Learning in RBFNs, RBF application to face recognition.	L1, L2, L3
Module-4	
Attractor Neural Networks: Associative Learning Attractor Associative Memory, Linear Associative memory, Hopfield Network, application of Hopfield Network, Brain State in a Box neural Network, Simulated Annealing, Boltzmann Machine, Bidirectional Associative Memory.	L1, L2, L3
Module-5	
Self-organization Feature Map: Maximal Eigenvector Filtering, Extracting Principal Components, Generalized Learning Laws, Vector Quantization, Self-organization Feature Maps, Application of SOM, Growing Neural Gas.	L1, L2, L3

Course outcomes: At the end of the course, students should be able to:

- Understand the role of neural networks in engineering, artificial intelligence, and cognitive modelling.
- Understand the concepts and techniques of neural networks through the study of the most important neural network models.
- Evaluate whether neural networks are appropriate to a particular application.
- Apply neural networks to particular applications, and to know what steps to take to improve performance.

Question paper pattern:

The question paper will have ten questions.

- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Neural Networks A Classroom Approach– Satish Kumar, McGraw Hill Education (India) Pvt. Ltd, Second Edition.

Reference Books:

1. **Introduction to Artificial Neural Systems**-J.M. Zurada, Jaico Publications 1994.
2. **Artificial Neural Networks**-B. Yegnanarayana, PHI, New Delhi 1998.

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DIGITAL SWITCHING SYSTEMS

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC654	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to

- Understand the basics of telecommunication networks and digital transmission of data.
- Study about the evolution of switching systems and the digital switching.
- Study about the telecommunication traffic and its measurements.
- Learn the technologies associated with the data switching operations.
- Understand the use of software for the switching and its maintenance

Module-1	RBT Level
DEVELOPMENT OF TELECOMMUNICATIONS: Network structure, Network services, terminology, Regulation, Standards. Introduction to telecommunications transmission, Power levels, Four wire circuits, Digital transmission, FDM,TDM, PDH and SDH [Text-1]	L1, L2
Module-2	
EVOLUTION OF SWITCHING SYSTEMS: Introduction, Message switching, Circuit switching, Functions of switching systems, Distribution systems, Basics of crossbar systems, Electronic switching. **DIGITAL SWITCHING SYSTEMS:** Switching system hierarchy, Evolution of digital switching systems, Stored program control switching systems, Building blocks of a digital switching system, Basic call processing. [Text-1 and 2]	L1, L2
Module-3	
TELECOMMUNICATIONS TRAFFIC: Introduction, Unit of traffic, Congestion, Traffic measurement, Mathematical model, lost call systems, Queuing systems. **SWITCHING SYSTEMS:** Introduction, Single stage networks, Gradings, Link Systems, GOS of Linked systems. [Text-1]	L1, L2
Module-4	
TIME DIVISION SWITCHING: Introduction, space and time switching, Time switching networks, Synchronisation. **SWITCHING SYSTEM SOFTWARE:** Introduction, Basic software architecture, Software architecture for level 1to 3 control, Digital switching system software classification, Call models, Software linkages during call, Feature flow diagram, Feature interaction. [Text-1 and 2]	L1, L2
Module-5	
MAINTENANCE OF DIGITAL SWITCHING SYSTEM: Introduction , Software maintenance, Interface of a typical digital switching system central office, System outage and its impact on digital switching system reliability, Impact	L1, L2

of software patches on digital switching system maintainability, A methodology for proper maintenance of digital switching system **A GENERIC DIGITAL SWITCHING SYSTEM MODEL:** Introduction, Hardware architecture, Software architecture, Recovery strategy, Simple call through a digital system, Common characteristics of digital switching systems. Reliability analysis. [Text-2]	

Course Outcomes: At the end of the course, students should be able to:

- Describe the electromechanical switching systems and its comparison with the digital switching.
- Determine the telecommunication traffic and its measurements.
- Define the technologies associated with the data switching operations.
- Describe the software aspects of switching systems and its maintenance.

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Books:

1. Telecommunication and Switching, Traffic and Networks - J E Flood: Pearson Education, 2002.
2. Digital Switching Systems, Syed R. Ali, TMH Ed 2002.

Reference Book:

Digital Telephony - John C Bellamy: Wiley India Pvt. Ltd, 3rd Ed, 2008.

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MICROELECTRONICS

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC655	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Be familiar with the MOSFET physical structure and operation, terminal characteristics, circuit models and basic circuit applications.
- Confront integrated device and/or circuit design problems, identify the design issues, and develop solutions.
- Analyze and design microelectronic circuits for linear amplifier and digital applications.
- Contrast the input/output and gain characteristics of single-transistor, differential and common two-transistor linear amplifier building block stages.

Module-1	RBT Level
MOSFETS: Device Structure and Physical Operation, V-I Characteristics, MOSFET Circuits at DC, MOSFET as an amplifier and as a switch.	L1, L2
Module-2	
MOSFETS (continued): Biasing in MOS amplifier Circuits, Small Signal Operation and Models, Basic MOSFET amplifier, MOSFET internal capacitances, frequency response of CS amplifier.	L1, L2
Module-3	
MOSFETS (continued): Discrete circuit MOS amplifiers. **Single Stage IC Amplifier:** Comparison of MOSFET and BJT, Current sources, Current mirrors and Current steering circuits, high frequency response- general considerations.	L1, L2, L3
Module-4	
Single Stage IC Amplifier (continued):CS with active loads, high frequency response of CS, CG amplifiers with active loads, high frequency response of CG, Cascode amplifiers. CS with source degeneration (only MOS amplifiers to be dealt).	L1, L2
Module-5	
Differential and Multistage Amplifiers: The MOS differential pair, small signal operation of MOS differential pair, Differential amplifier with active loads, and frequency response of the differential amplifiers. Multistage amplifiers (only MOS amplifiers to be dealt).	L1, L2
Course outcomes: After studying this course, students will be able to: • Explain the underlying physics and principles of operation of Metaloxide-semiconductor (MOS) capacitors and MOS field effect transistors (MOSFETs). • Describe and apply simple large signal circuit models for MOSFETs. • Analyze and design microelectronic circuits for linear amplifier for digital applications.	

• Use of discrete MOS circuits to design Single stage and Multistage amplifiers to meet stated operating specifications.	

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

"Microelectronic Circuits", Adel Sedra and K.C. Smith, 6th Edition, Oxford University Press, International Version, 2009.

Reference Books:

1. **"Microelectronics An integrated approach",** Roger T Howe, Charles G Sodini, Pearson education.
2. **"Fundamentals of Microelectronics",** Behzad Razavi, John Wiley India Pvt. Ltd, 2008.
3. **"Microelectronics – Analysis and Design",** Sundaram Natarajan, Tata McGraw-Hill, 2007.

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EMBEDDED CONTROLLER LAB

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15ECL67	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory = 03	Exam Marks	80
RBT Levels	L1, L2, L3	Exam Hours	03

CREDITS – 02

Course objectives: This course will enable students to:

- Understand the instruction set of ARM Cortex M3, a 32 bit microcontroller and the software tool required for programming in Assembly and C language.
- Program ARM Cortex M3 using the various instructions in assembly level language for different applications.
- Interface external devices and I/O with ARM Cortex M3.
- Develop C language programs and library functions for embedded system applications.

Laboratory Experiments

PART-A: Conduct the following Study experiments to learn ALP using ARM Cortex M3 Registers using an Evaluation board and the required software tool.

1. ALP to multiply two 16 bit binary numbers.
2. ALP to find the sum of first 10 integer numbers.

PART-B: Conduct the following experiments on an ARM CORTEX M3 evaluation board using evaluation version of Embedded 'C' & Keil uVision-4 tool/compiler.

1. Display "Hello World" message using Internal UART.
2. Interface and Control a DC Motor.
3. Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.

4. Interface a DAC and generate Triangular and Square waveforms.
5. Interface a 4x4 keyboard and display the key code on an LCD.
6. Using the Internal PWM module of ARM controller generate PWM and vary its duty cycle.
7. Demonstrate the use of an external interrupt to toggle an LED On/Off.
8. Display the Hex digits 0 to F on a 7-segment LED interface, with an appropriate delay in between.
9. Interface a simple Switch and display its status through Relay, Buzzer and LED.
10. Measure Ambient temperature using a sensor and SPI ADC IC.

Course outcomes: After studying this course, students will be able to:

- Understand the instruction set of 32 bit microcontroller ARM Cortex M3, and the software tool required for programming in Assembly and C language.
- Develop assembly language programs using ARM Cortex M3 for different applications.
- Interface external devices and I/O with ARM Cortex M3.
- Develop C language programs and library functions for embedded system applications.

Conduction of Practical Examination:

1. PART-B experiments using Embedded-C are only to be considered for the practical examination. PART-A ALP programs are for study purpose and can be considered for Internal Marks evaluation.
2. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
3. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

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COMPUTER NETWORKS LABORATORY

B.E., VI Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15ECL68	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory = 03	Exam Marks	80
RBT Levels	L1, L2, L3	Exam Hours	03

CREDITS – 02

Course objectives: This course will enable students to:

- Choose suitable tools to model a network and understand the protocols at various OSI reference levels.
- Design a suitable network and simulate using a Network simulator tool.
- Simulate the networking concepts and protocols using C/C++ programming.
- Model the networks for different configurations and analyze the results.

Laboratory Experiments

PART-A: Simulation experiments using NS2/ NS3/ OPNET/ NCTUNS/ NetSim/ QualNet or any other equivalent tool

1. Implement a point to point network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.
2. Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent by TCP/UDP.
3. Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.
4. Implement Ethernet LAN using n nodes and assign multiple traffic to the nodes and obtain congestion window for different sources/ destinations.
5. Implement ESS with transmission nodes in Wireless LAN and obtain the performance parameters.
6. Implementation of Link state routing algorithm.

PART-B: Implement the following in C/C++

1. Write a program for a HLDC frame to perform the following.

i) Bit stuffing

ii) Character stuffing.

2. Write a program for distance vector algorithm to find suitable path for transmission.

3. Implement Dijkstra's algorithm to compute the shortest routing path.
4. For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify the program for the cases

   a. Without error

b. With error

5. Implementation of Stop and Wait Protocol and Sliding Window Protocol
6. Write a program for congestion control using leaky bucket algorithm.

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Use the network simulator for learning and practice of networking algorithms.
- Illustrate the operations of network protocols and algorithms using C programming.
- Simulate the network with different configurations to measure the performance parameters.
- Implement the data link and routing protocols using C programming.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination one question from software and one question from hardware or only one hardware experiments based on the complexity to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

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6th Semester Open Electives Syllabus for the courses offered by EC/TC Board:

DATA STRUCTURE USING C++
B.E VI Semester (Open Elective)
[As per Choice Based Credit System (CBCS) Scheme]

Course Code	**15EC661**	**IA Marks**	20
Number of Lecture Hours/Week	03	**Exam Marks**	80
Total Number of Lecture Hours	**40 (08 Hrs per Module)**	**Exam Hours**	03

CREDITS – 03

Course objectives: This course will enable students to

- Explain fundamentals of data structures and their applications essential for programming/problem solving
- Analyze Linear Data Structures: Stack, Queues, Lists
- Analyze Non Linear Data Structures: Trees
- Assess appropriate data structure during program development/Problem Solving

Module -1

INTRODUCTION: Functions and parameters, Dynamic memory allocation, Recursion.
LINEAR LISTS: Data objects and structures, Linear list data structures, Array Representation, Vector Representation, Singly Linked lists and chains. **L1, L2**

Module -2

ARRAYS AND MATRICS: Arrays, Matrices, Special matrices, Sparse matrices.

STACKS: The abstract data types, Array Representation, Linked Representation, Applications-Parenthesis Matching & Towers of Hanoi. **L1, L2, L3**

Module -3

QUEUES: The abstract data types, Array Representation, Linked Representation, Applications-Railroad car arrangement.

HASHING: Dictionaries, Linear representation, Hash table representation. **L1, L2, L3**

Module -4

BINARY AND OTHER TREES: Trees, Binary trees, Properties and representation of binary trees, Common binary tree operations, Binary tree traversal the ADT binary tree, ADT binary tree and the class linked binary tree. **L1, L2, L3**

Module -5

Priority Queues: Linear lists, Heaps, Applications-Heap Sorting.
Search Trees: Binary search trees operations and implementation, Binary Search trees with duplicates. **L1, L2, L3**

Course outcomes: After studying this course, students will be able to:

- Acquire knowledge of Dynamic memory allocation, Various types of data structures, operations and algorithms and Sparse matrices and Hashing
- Understand non Linear data structures trees and their applications
- Design appropriate data structures for solving computing problems
- Analyze the operations of Linear Data structures: Stack, Queue and Linked List and their applications

Text Book:

Data structures, Algorithms, and applications in C++, Sartaj Sahni, Universities Press, 2nd Edition, 2005.

Reference Books:

1. **Data structures, Algorithms, and applications in C++,** Sartaj Sahni, Mc. Graw Hill, 2000.
2. **Object Oriented Programming with C++,** E.Balaguruswamy, TMH, 6th Edition, 2013.
3. **Programming in C++,** E.Balaguruswamy. TMH, 4th, 2010.

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POWER ELECTRONICS

B.E., VI Semester (Open Elective)

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC662	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (08 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to

- Understand the working of various power devices.
- Study and analysis of thyristor circuits with different triggering techniques.
- Learn the applications of power devices in controlled rectifiers, converters and inverters.
- Study of power electronics circuits under different load conditions.

Module-1	**RBT Level**
Introduction - Applications of Power Electronics, Power Semiconductor Devices, Control Characteristics of Power Devices, types of Power Electronic Circuits. Power Transistors: Power BJTs: Steady state characteristics. Power MOSFETs: device operation, switching characteristics, IGBTs: device operation, output and transfer characteristics. (Text 1)	L1, L2
Module-2	
Thyristors - Introduction, Principle of Operation of SCR, Static Anode-Cathode Characteristics of SCR, Two transistor model of SCR, Gate Characteristics of SCR, Turn-ON Methods, Turn-OFF Mechanism, Turn-OFF Methods: Natural and Forced Commutation – Class A and Class B types, Gate Trigger Circuit: Resistance Firing Circuit, Resistance capacitance firing circuit. (Text 2)	L1, L2, L3
Module-3	
Controlled Rectifiers - Introduction, principle of phase controlled converter operation, Single phase full converters, Single phase dual converters. AC Voltage Controllers - Introduction, Principles of ON-OFF Control, Principle of Phase Control, Single phase control with resistive and inductive loads. (Text 1)	L1, L2, L3
Module-4	
DC-DC Converters - Introduction, principle of step-down operation and it's analysis with RL load, principle of step-up operation, Step-up converter with a resistive load, Performance parameters, Converter classification, Switching mode regulators: Buck regulator, Boost regulator, Buck-Boost Regulators. (Text 1)	L1, L2

Module-5	
Pulse Width Modulated Inverters- Introduction, principle of operation, performance parameters, Single phase bridge inverters, voltage control of single phase inverters, current source inverters, Variable DC-link inverter, Boost inverter. (Text 1)	L1, L2

Course outcomes: After studying this course, students will be able to:

- Describe the characteristics of different power devices and identify the applications.
- Illustrate the working of DC-DC converter and inverter circuit.
- Determine the output response of a thyristor circuit with various triggering options.
- Determine the response of controlled rectifier with resistive and inductive loads.

Evaluation of Internal Assessment Marks:

It is suggested that at least a few experiments of Power Electronics are conducted by the students for better understanding of the course. This activity can be considered for the evaluation of 5 marks out of 20 Internal assessment marks, reserved for the other activities.

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

1. Mohammad H Rashid, Power Electronics, Circuits, Devices and Applications, 3rd/4th Edition, Pearson Education Inc, 2014, ISBN: 978-93-325-1844-5.
2. M.D Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897.

Reference Books:

4. L. Umanand, Power Electronics, Essentials and Applications, John Wiley India Pvt. Ltd, 2009.
5. Dr. P. S. Bimbhra, "Power Electronics", Khanna Publishers, Delhi, 2012.
6. P.C. Sen, "Modern Power Electronics", S Chand & Co New Delhi, 2005.

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DIGITAL SYSTEM DESIGN USING VERILOG

B.E., VI Semester (Open Elective)

[As per Choice Based Credit System (CBCS) scheme]

Subject Code:	15EC663	IA Marks: 20
Number of Lecture Hours/Week:	03	Exam Marks: 80
Total Number of Lecture Hours:	40 (08 Hrs per module)	Exam Hours: 03
CREDITS – 03		

Course objectives: This course will enable students to:

- Understand the concepts of Verilog Language.
- Design the digital systems as an activity in a larger systems design context.
- Study the design and operation of semiconductor memories frequently used in application specific digital system.
- Inspect how effectively IC's are embedded in package and assembled in PCB's for different application.
- Design and diagnosis of processors and I/O controllers used in embedded systems.

Module -1	RBT Level
Introduction and Methodology: Digital Systems and Embedded Systems, Real-World Circuits, Models, Design Methodology (1.1, 1.3 to 1.5 of Text). **Combinational Basics:** Combinational Components and Circuits, Verification of Combinational Circuits.(2.3 and 2.4 of Text) **Sequential Basics**: Sequential Datapaths and Control Clocked Synchronous Timing Methodology (4.3 up to 4.3.1,4.4 up to 4.4.1 of Text).	L1, L2, L3
Module -2	
Memories: Concepts, Memory Types, Error Detection and Correction (Chap 5 of Text).	L1, L2, L3
Module -3	
Implementation Fabrics: Integrated Circuits, Programmable Logic Devices, Packaging and Circuit boards, Interconnection and Signal integrity (Chap 6 of Text).	L1, L2, L3
Module -4	
I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software (Chap 8 of Text).	L1, L2, L3
Module -5	
Design Methodology: Design flow, Design optimization, Design for test, Nontechnical Issues (Chap 10 of Text).	L1, L2, L3, L4

Course outcomes: After studying this course, students will be able to:

- Construct the combinational circuits, using discrete gates and programmable logic devices.
- Describe Verilog model for sequential circuits and test pattern generation.

- Design a semiconductor memory for specific chip design.
- Design embedded systems using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores.
- Synthesize different types of processor and I/O controllers that are used in embedded system.

Question paper pattern:

- The question paper will have ten questions.
- Each full Question consisting of 16 marks. There will be 2 full questions (with a maximum of Three sub questions from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using VERILOG", Elesvier, 2010.

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B.E E&C SEVENTH SEMESTER SYLLABUS

MICROWAVES AND ANTENNAS

B.E., VII Semester, Electronics &Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**15EC71**	**IA Marks**	**20**
Number of Lecture Hours/Week	**04**	**Exam Marks**	**80**
Total Number of Lecture Hours	**50 (10 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 04

Course objectives: This course will enable students to:

- Describe the microwave properties and its transmission media
- Describe microwave devices for several applications
- Understand the basics of antenna theory
- Select antennas for specific applications

Module-1

Microwave Tubes: Introduction, Reflex Klystron Oscillator, Mechanism of Oscillations, Modes of Oscillations, Mode Curve (Qualitative Analysis only). (Text 1: 9.1, 9.2.2)
Microwave Transmission Lines: Microwave Frequencies, Microwave devices, Microwave Systems, Transmission Line equations and solutions, Reflection Coefficient and Transmission Coefficient, Standing Wave and Standing Wave Ratio, Smith Chart, Single Stub matching. (Text 2: 0.1, 0.2, 0.3, 3.1, 3.2, 3.3, 3.5, 3.6 Except Double stub matching) **L1, L2**

Module-2

Microwave Network theory: Symmetrical Z and Y-Parameters for Reciprocal Networks, S matrix representation of Multi-Port Networks. (Text 1: 6.1, 6.2, 6.3)
Microwave Passive Devices: Coaxial Connectors and Adapters, Attenuators, Phase Shifters, Waveguide Tees, Magic tees. (Text 1: 6.4.2, 6.4.14, 6.4.15, 6.4.16) **L1, L2**

Module-3

Strip Lines: Introduction, Micro Strip lines, Parallel Strip lines, Coplanar Strip lines, Shielded Strip Lines. (Text 2: Chapter 11)
Antenna Basics: Introduction, Basic Antenna Parameters, Patterns, Beam Area, Radiation Intensity, Beam Efficiency, Directivity and Gain, Antenna Apertures, Effective Height, Bandwidth, Radio Communication Link, Antenna Field Zones & Polarization. (Text 3: 2.1- 2.11, 2.13,2.15) **L1, L2, L3**

Module-4
Point Sources and Arrays: Introduction, Point Sources, Power Patterns, Power Theorem, Radiation Intensity, Field Patterns, Phase Patterns, Arrays of Two Isotropic Point Sources, Pattern Multiplication, Linear Arrays of n Isotropic Point Sources of equal Amplitude and Spacing.(Text 3: 5.1 – 5.10,5.13) **Electric Dipoles:** Introduction, Short Electric Dipole, Fields of a Short Dipole (General and Far Field Analyses), Radiation Resistance of a Short Dipole, Thin Linear Antenna (Field Analyses), Radiation Resistances of Lambda/2 Antenna. (Text 3: 6.1 -6.6) **L1, L2, L3, L4**
Module-5
Loop and Horn Antenna: Introduction, Small loop, Comparison of Far fields of Small Loop and Short Dipole, The Loop Antenna General Case, Far field Patterns of Circular Loop Antenna with Uniform Current, Radiation Resistance of Loops, Directivity of Circular Loop Antennas with Uniform Current, Horn antennas Rectangular Horn Antennas.(Text 3: 7.1-7.8, 7.19, 7.20) **Antenna Types:** Helical Antenna, Helical Geometry, Practical Design Considerations of Helical Antenna, Yagi-Uda array, Parabola General Properties, Log Periodic Antenna. (Text 3: 8.3, 8.5, 8.8, 9.5, 11.7) **L1, L2, L3**
Course Outcomes: At the end of the course, students will be able to: • Describe the use and advantages of microwave transmission • Analyze various parameters related to microwave transmission lines and waveguides • Identify microwave devices for several applications • Analyze various antenna parameters necessary for building an RF system • Recommend various antenna configurations according to the applications
Text Books: 1. **Microwave Engineering** – Annapurna Das, Sisir K Das TMH Publication, 2nd, 2010. 2. **Microwave Devices and circuits**- Liao, Pearson Education. 3. **Antennas and Wave Propagation,** John D. Krauss, Ronald J Marhefka and Ahmad S Khan,4th Special Indian Edition , McGraw- Hill Education Pvt. Ltd., 2010.
Reference Books: 1. **Microwave Engineering** – David M Pozar, John Wiley India Pvt. Ltd. 3rdEdn, 2008. 2. **Microwave Engineering** – Sushrut Das, Oxford Higher Education, 2ndEdn, 2015. 3. **Antennas and Wave Propagation** – Harish and Sachidananda: Oxford University Press, 2007.

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DIGITAL IMAGE PROCESSING

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC72	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours / Module)	Exam Hours	03
CREDITS – 04			

Course Objectives: The objectives of this course are to:

- Understand the fundamentals of digital image processing
- Understand the image transform used in digital image processing
- Understand the image enhancement techniques used in digital image processing
- Understand the image restoration techniques and methods used in digital image processing
- Understand the Morphological Operations and Segmentation used in digital image processing

Module-1	RBT Level
Digital Image Fundamentals: What is Digital Image Processing?, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels, Linear and Nonlinear Operations. [Text: Chapter 1 and Chapter 2: Sections 2.1 to 2.5, 2.6.2]	L1, L2
Module-2	
Spatial Domain: Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters **Frequency Domain**: Preliminary Concepts, The Discrete Fourier Transform (DFT) of Two Variables, Properties of the 2-D DFT, Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters, Selective Filtering. [Text: Chapter 3: Sections 3.2 to 3.6 and Chapter 4: Sections 4.2, 4.5 to 4.10]	L1, L2, L3
Module-3	
Restoration: Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Linear, Position-Invariant Degradations, Estimating the Degradation Function, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering, Constrained Least Squares Filtering. [Text: Chapter 5: Sections 5.2, to 5.9]	L1, L2, L3
Module-4	

Color Image Processing: Color Fundamentals, Color Models, Pseudocolor Image Processing. **Wavelets:** Background, Multiresolution Expansions. **Morphological Image Processing:** Preliminaries, Erosion and Dilation, Opening and Closing, The Hit-or-Miss Transforms, Some Basic Morphological Algorithms. [Text: Chapter 6: Sections 6.1 to 6.3, Chapter 7: Sections 7.1 and 7.2, Chapter 9: Sections 9.1 to 9.5]	L1, L2, L3
Module-5	
Segmentation: Point, Line, and Edge Detection, Thresholding, Region-Based Segmentation, Segmentation Using Morphological Watersheds. **Representation and Description:** Representation, Boundary descriptors. [Text: Chapter 10: Sections 10.2, to 10.5 and Chapter 11: Sections 11.1 and 11.2]	L1, L2, L3
Course Outcomes: At the end of the course students should be able to: • Understand image formation and the role human visual system plays in perception of gray and color image data. • Apply image processing techniques in both the spatial and frequency (Fourier) domains. • Design image analysis techniques in the form of image segmentation and to evaluate the Methodologies for segmentation. • Conduct independent study and analysis of Image Enhancement techniques.	
Question paper pattern: • The question paper will have ten questions. • Each full question consists of 16 marks. • There will be 2 full questions (with a maximum of Three sub questions) from each module. • Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.	
Text Book: **Digital Image Processing**- Rafel C Gonzalez and Richard E. Woods, PHI 3rd Edition 2010.	
Reference Books: 1. **Digital Image Processing**- S.Jayaraman, S.Esakkirajan, T.Veerakumar, Tata McGraw Hill 2014. 2. **Fundamentals of Digital Image Processing**-A. K. Jain, Pearson 2004.	

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POWER ELECTRONICS

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

POWER ELECTRONICS B.E., VII Semester, Electronics & Communication Engineering [As per Choice Based Credit System (CBCS) Scheme]			
Course Code	**15EC73**	**IA Marks**	**20**
Number of Lecture Hours/Week	**04**	**Exam Marks**	**80**
Total Number of Lecture Hours	**50 (10 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable students to:

- Understand the construction and working of various power devices.
- Study and analysis of thyristor circuits with different triggering conditions.
- Learn the applications of power devices in controlled rectifiers, converters and inverters.
- Study of power electronics circuits under various load conditions.

Module-1

Introduction - Applications of Power Electronics, Power Semiconductor Devices, Control Characteristics of Power Devices, types of Power Electronic Circuits, Peripheral Effects. Power Transistors: Power BJTs: Steady state characteristics. Power MOSFETs: device operation, switching characteristics, IGBTs: device operation, output and transfer characteristics, di/dt and dv/dt limitations. (Text 1) **L1, L2**

Module-2

Thyristors - Introduction, Principle of Operation of SCR, Static Anode-Cathode Characteristics of SCR, Two transisitor model of SCR, Gate Characteristics of SCR, Turn-ON Methods, Turn-OFF Mechanism, Turn-OFF Methods: Natural and Forced Commutation – Class A and Class B types, Gate Trigger Circuit: Resistance Firing Circuit, Resistance capacitance firing circuit, UJT Firing Circuit. (Text 2) **L1, L2, L3**

Module-3

Controlled Rectifiers - Introduction, Principle of Phase-Controlled Converter Operation, Single-Phase Full Converter with RL Load, Single-Phase Dual Converters, Single-Phase Semi Converter with RL load.

AC Voltage Controllers - Introduction, Principles of ON-OFF Control, Principle of Phase Control, Single phase controllers with resistive and inductive loads. (Text 1) **L1, L2, L3**

Module-4

DC-DC Converters - Introduction, principle of step-down operation and it's analysis with RL load, principle of step-up operation, Step-up converter with a resistive load, Performance parameters, Converter classification, Switching mode regulators: Buck regulator, Boost regulator, Buck-Boost Regulators, Chopper circuit design. (Text 1) **L1, L2**

Module-5

Pulse Width Modulated Inverters- Introduction, principle of operation, performance parameters, Single phase bridge inverters, voltage control of single phase inverters, current source inverters, Variable DC-link inverter, Boost inverter, Inverter circuit design.

Static Switches: Introduction, Single phase AC switches, DC Switches, Solid state

relays, Microelectronic relays. (Text 1) **L1, L2**

Course Outcomes: At the end of the course students should be able to:

- Describe the characteristics of different power devices and identify the various applications associated with it.
- Illustrate the working of power circuit as DC-DC converter.
- Illustrate the operation of inverter circuit and static switches.
- Determine the output response of a thyristor circuit with various triggering options.
- Determine the response of controlled rectifier with resistive and inductive loads.

Evaluation of Internal Assessment Marks:

It is suggested that at least 4 experiments of Power Electronics to be conducted by the students. This activity can be considered for the evaluation of 05 marks out of 20 Internal Assessment (IA) Marks, reserved for the other activities.

Text Books:

1. Mohammad H Rashid, Power Electronics, Circuits, Devices and Applications, 3rd/4th Edition, Pearson Education Inc, 2014, ISBN: 978-93-325-1844-5.
2. M.D Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897

Reference Books:

1. L. Umanand, Power Electronics, Essentials and Applications, John Wiley India Pvt. Ltd, 2009.
2. Dr. P. S. Bimbhra, "Power Electronics", Khanna Publishers, Delhi, 2012.
3. P.C. Sen, "Modern Power Electronics", S Chand & Co New Delhi, 2005.
4. Earl Gose, Richard Johnsonbaugh, Steve Jost, Pattern Recognition and Image Analysis, ePub eBook.

MULTIMEDIA COMMUNICATION

B.E., VII Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based credit System (CBCS) Scheme

Subject Code	15EC741	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (08 Hours / Module)	Exam Hours	03
CREDITS – 03			

Course objectives: This course will enable students to:

- Gain fundamental knowledge in understanding the basics of different multimedia networks and applications.
- Understand digitization principle techniques required to analyze different media types.
- Analyze compression techniques required to compress text and image and gain knowledge of DMS.
- Analyze compression techniques required to compress audio and video.
- Gain fundamental knowledge about multimedia communication across different networks.

Module-1	RBT Level
Multimedia Communications: Introduction, Multimedia information representation, multimedia networks, multimedia applications, Application and networking terminology. (Chap 1 of Text 1)	L1, L2
Module-2	
Information Representation: Introduction, Digitization principles, Text, Images, Audio and Video (Chap 2 of Text 1)	L1, L2
Module-3	
Text and image compression: Introduction, Compression principles, text compression, image Compression. (Chap 3 of Text 1) **Distributed multimedia systems:** Introduction, main Features of a DMS, Resource management of DMS, Networking, Multimedia operating systems (Chap. 4 - Sections 4.1 to 4.5 of Text 2).	L1, L2, L3
Module-4	
Audio and video compression: Introduction, Audio compression, video compression, video compression principles, video compression. (Chap. 4 of Text 1).	L1, L2, L3
Module-5	
Multimedia Communication Across Networks: Packet audio/video in the network environment, Video transport across generic networks, Multimedia Transport across ATM Networks (Chap. 6 - Sections 6.1, 6.2, 6.3 of Text 2).	L1, L2

Course Outcomes: After studying this course, students will be able to:

- Understand basics of different multimedia networks and applications.
- Understand different compression techniques to compress audio and video.
- Describe multimedia Communication across Networks.
- Analyse different media types to represent them in digital form.
- Compress different types of text and images using different compression techniques and analyse DMS.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Fred Halsall, "Multimedia Communications", Pearson education, 2001 ISBN - 9788131709948.

2. K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, "Multimedia Communication Systems", Pearson education, 2004. ISBN -9788120321458

Reference Book:

Raifsteinmetz, Klara Nahrstedt, "Multimedia: Computing, Communications and Applications", Pearson education, 2002. ISBN -9788177584417

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BIOMEDICAL SIGNAL PROCESSING

B.E., VII Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC742	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: The objectives of this course are to:

- Describe the origin, properties and suitable models of important biological signals such as ECG and EEG.
- Introduce students to basic signal processing techniques in analysing biological signals.
- Develop the students mathematical and computational skills relevant to the field of biomedical signal processing.
- Develop a thorough understanding on basics of ECG signal compression algorithms.
- Increase the student's awareness of the complexity of various biological phenomena and cultivate an understanding of the promises, challenges of the biomedical engineering.

Module-1	RBT Level
Introduction to Biomedical Signals: The nature of Biomedical Signals, Examples of Biomedical Signals, Objectives and difficulties in Biomedical analysis. **Electrocardiography:** Basic electrocardiography, ECG lead systems, ECG signal characteristics. **Signal Conversion** :Simple signal conversion systems, Conversion requirements for biomedical signals, Signal conversion circuits (Text-1)	L1, L2
Module-2	
Signal Averaging: Basics of signal averaging, signal averaging as a digital filter, a typical averager, software for signal averaging, limitations of signal averaging. **Adaptive Noise Cancelling:** Principal noise canceller model, 60-Hzadaptive cancelling using a sine wave model, other applications of adaptive filtering (Text-1)	L1, L2, L3
Module-3	
Data Compression Techniques: Turning point algorithm, AZTEC algorithm, Fan algorithm, Huffman coding, data reduction algorithms The Fourier transform, Correlation, Convolution, Power spectrum estimation, Frequency domain analysis of the ECG (Text-1)	L1, L2, L3
Module-4	

Cardiological signal processing: Basic Electrocardiography, ECG data acquisition, ECG lead system, ECG signal characteristics (parameters and their estimation), Analog filters, ECG amplifier, and QRS detector, Power spectrum of the ECG, Bandpass filtering techniques, Differentiation techniques, Template matching techniques, A QRS detection algorithm, Realtime ECG processing algorithm, ECG interpretation, ST segment analyzer, Portable arrhythmia monitor. (Text -2)	L1, L2, L3
Module-5	
Neurological signal processing: The brain and its potentials, The electrophysiological origin of brain waves, The EEG signal and its characteristics (EEG rhythms, waves, and transients), Correlation. **Analysis of EEG channels:** Detection of EEG rhythms, Template matching for EEG, spike and wave detection (Text-2).	L1, L2, L3
Course outcomes: At the end of the course, students will be able to: • Possess the basic mathematical, scientific and computational skills necessary to analyse ECG and EEG signals. • Apply classical and modern filtering and compression techniques for ECG and EEG signals • Develop a thorough understanding on basics of ECG and EEG feature extraction.	
Question paper pattern: • The question paper will have ten questions. • Each full question consists of 16 marks. • There will be 2 full questions (with a maximum of Three sub questions) from each module. • Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.	
Text Books: 1. **Biomedical Digital Signal Processing-** Willis J. Tompkins, PHI 2001. 2. **Biomedical Signal Processing Principles and Techniques-** D C Reddy, McGraw-Hill publications 2005	
Reference Book: **Biomedical Signal Analysis**-Rangaraj M. Rangayyan, John Wiley & Sons 2002	

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REAL TIME SYSTEMS

B.E., VII Semester, Electronics & Communication Engineering /Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC743	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (08 Hours per Module)	Exam Hours	03

Credits – 03

Course Objectives: This Course will enable students to:

- Discuss the historical background of Real-time systems and its classifications.
- Describe the concepts of computer control and hardware components for Real-Time Application.
- Discuss the languages to develop software for Real-Time Applications.
- Explain the concepts of operating system and RTS development methodologies.

Modules	RBT Level
Module-1	
Introduction to Real-Time Systems: Historical background, Elements of a Computer Control System, RTS- Definition, Classification of Real-time Systems, Time Constraints, Classification of Programs. **Concepts of Computer Control:** Introduction, Sequence Control, Loop Control, Supervisory Control, Centralized Computer Control, Hierarchical Systems. (Text Book: 1.1 to 1.6 and 2.1 to 2.6)	L1, L2
Module-2	
Computer Hardware Requirements for Real-Time Applications: Introduction, General Purpose Computer, Single Chip Microcomputers and Microcontrollers, Specialized Processors, Process-Related Interfaces, Data Transfer Techniques, Communications, Standard Interface.(Text Book: 3.1 to 3.8)	L1, L2
Module-3	
Languages for Real-Time Applications: Introduction, Syntax Layout and Readability, Declaration and Initialization of Variables and Constants, Modularity and Variables, Compilation of Modular Programs, Data types, Control Structures, Exception Handling, Low-level facilities, Co-routines, Interrupts and Device Handling, Concurrency, Real-Time Support, Overview of Real-Time Languages. (Text Book: 5.1 to 5.14)	L1, L2, L3
Module-4	
Operating Systems: Introduction, Real-Time Multi-Tasking OS, Scheduling Strategies, Priority Structures, Task Management, Scheduler and Real-Time Clock Interrupt Handler, Memory Management, Code Sharing, Resource Control, Task Co-Operation and Communication, Mutual Exclusion.(Text Book: 6.1 to 6.11)	L1, L2

Module-5	
Design of RTS – General Introduction: Introduction, Specification Document, Preliminary Design, Single-Program Approach, Foreground/Background System. **RTS Development Methodologies:** Introduction, Yourdon Methodology, Ward and Mellor Method, Hately and Pirbhai Method. (Text Book: 7.1 to 7.5 and 8.1, 8.2, 8.4,8.5)	L1, L2, L3
Course Outcomes: At the end of the course, students should be able to: • Understand the fundamentals of Real time systems and its classifications. • Understand the concepts of computer control, operating system and the suitable computer hardware requirements for real-time applications. • Develop the software languages to meet Real time applications. • Apply suitable methodologies to design and develop Real-Time Systems.	
Question Paper Pattern: • The question paper will have ten questions. • Each full Question consisting of 16 marks • There will be 2 full questions (with a maximum of Three sub questions) from each module. • Each full question will have sub questions covering all the topics under a module. • The students will have to answer 5 full questions, selecting one full question from each module.	
Text Book: Real-Time Computer Control, by Stuart Bennet, 2nd Edn. Pearson Education. 2008.	
Reference Books: 1. C.M. Krishna, Kang G. Shin, "Real –Time Systems", McGraw –Hill International Editions, 1997. 2. Real-Time Systems Design and Analysis, Phillip. A. Laplante, second edition, PHI, 2005. 3. Embedded Systems, Raj Kamal, Tata McGraw Hill, India, third edition, 2005.	

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Cryptography

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC744	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (08 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This Course will enable students to:

- Enable students to understand the basics of symmetric key and public key cryptography.
- Equip students with some basic mathematical concepts and pseudorandom number generators required for cryptography.
- Enable students to authenticate and protect the encrypted data.
- Enrich knowledge about Email, IP and Web security.

Modules

Module-1	**RBT Level**
Basic Concepts of Number Theory and Finite Fields: Divisibility and the divisibility algorithm, Euclidean algorithm, Modular arithmetic, Groups, Rings and Fields, Finite fields of the form GF(p), Polynomial arithmetic, Finite fields of the form GF(2^n)(Text 1: Chapter 3)	L1, L2
Module-2	
Classical Encryption Techniques: Symmetric cipher model, Substitution techniques, Transposition techniques, Steganography (Text 1: Chapter 1) **SYMMETRIC CIPHERS:** Traditional Block Cipher structure, Data Encryption Standard (DES) (Text 1: Chapter 2: Section1, 2)	L1, L2
Module-3	
SYMMETRIC CIPHERS: The AES Cipher. (Text 1: Chapter 4: Section 2, 3, 4) **Pseudo-Random-Sequence Generators and Stream Ciphers:** Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs (Text 2: Chapter 16: Section 1, 2, 3, 4)	L1, L2, L3
Module-4	
More number theory: Prime Numbers, Fermat's and Euler's theorem, Primality testing, Chinese Remainder theorem, discrete logarithm. (Text 1: Chapter 7) **Principles of Public-Key Cryptosystems**: The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography (Text 1: Chapter 8, Chapter 9: Section 1, 3, 4)	L1, L2, L3
Module-5	

One-Way Hash Functions: Background, Snefru, N-Hash, MD4, MD5, Secure Hash Algorithm [SHA],One way hash functions using symmetric block algorithms, Using public key algorithms, Choosing a one-way hash functions, Message Authentication Codes. Digital Signature Algorithm, Discrete Logarithm Signature Scheme (Text 2: Chapter 18: Section 18.1 to 18.5, 18.7, 18.11 to 18.14 and Chapter 20: Section 20.1, 20.4)	L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

- Use basic cryptographic algorithms to encrypt the data.
- Generate some pseudorandom numbers required for cryptographic applications.
- Provide authentication and protection for encrypted data.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of Three sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. William Stallings , "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X

Reference Books:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

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CAD for VLSI

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC745	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03
CREDITS – 03			

Course Objectives: This course will enable students to:

- Understand various stages of Physical design of VLSI circuits
- Know about mapping a design problem to a realizable algorithm
- Become aware of graph theoretic, heuristic and genetic algorithms
- Compare performance of different algorithms

Modules	RBT Level
Module 1	
Data Structures and Basic Algorithms: Basic terminology, Complexity issues and NP-Hardness. Examples - Exponential, heuristic, approximation and special cases. Basic Algorithms. Graph Algorithms for Search, spanning tree, shortest path, min-cut and max-cut, Steiner tree. Computational Geometry Algorithms: Line sweep and extended line sweep methods.	L1, L2
Module 2	
Basic Data Structures. Atomic operations for layout editors, Linked list of blocks, Bin-based method, Neighbor pointers, corner-stitching, Multi-layer operations, Limitations of existing data structures. Layout specification languages. **Graph algorithms for physical design:** Classes of graphs in physical design, Relationship between graph classes, Graph problems in physical design, Algorithms for Interval graphs, permutation graphs and circle graphs.	L1, L2
Module 3	

Partitioning: Problem formulation, Design style specific partitioning problems, Classification of Partitioning Algorithms. Group migration algorithms: Kernighan-Lin algorithm, Fiduccia-Mattheyses Algorithm, Simulated Annealing, Simulated Evolution. **Floor Planning:** Problem formulation, Constraint based floor planning, Rectangular dualization, Simulated evolution algorithms.	L1, L2,L3
Module 4	
Pin Assignment: Problem formulation. Classification of pin assignment problems, General pin assignment problem. **Placement:** Problem formulation, Classification of placement algorithms. Simulation based placement: Simulated annealing, simulated evolution, force directed placement. Partitioning based algorithms: Breur's Algorithm, Terminal propagation algorithm, Other algorithms for placement.	L1,L2,L3
Module 5	
Global Routing: Problem formulation, Classification of Global routing algorithms, Maze routing algorithms: Lee's algorithm, Soukup's algorithm and Hadlock's Algorithm, Line probe algorithms. **Detailed Routing:** Problem formulation, Routing considerations, models, channel routing and switch box routing problems. General river routing problem, Single row routing problem. Two-layer channel routing algorithms: Basic Left Edge Algorithm, Dogleg router, Symbolic router-YACR2.	L1,L2,L3
Course Outcomes: After studying this course, students will be able to: • Appreciate the problems related to physical design of VLSI • Use genralized graph theoretic approach to VLSI problems • Design Simulated Annealing and Evolutionary algorithms • Know various approaches to write generalized algorithms	
Question paper pattern: • The question paper will have 10 full questions carrying equal marks. • Each full question consists of 16 marks with a maximum of Three sub questions. • There will be 2 full questions from each module covering all the topics of the module • The students will have to answer 5 full questions, selecting one full question from each module.	

Text Book:

Algorithms for VLSI Physical Design Automation, 3rd Ed, Naveed Sherwani, 1999 Kluwer Academic Publishers, Reprint 2009 Springer (India) Private Ltd. ISBN 978-81-8128-317-7.

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DSP Algorithms and Architecture

B.E., VII Semester, Electronics & Communication Engineering /Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC751	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Figure out the knowledge and concepts of digital signal processing techniques.
- Understand the computational building blocks of DSP processors and its speed issues.
- Understand the various addressing modes, peripherals, interrupts and pipelining structure of TMS320C54xx processor.
- Learn how to interface the external devices to TMS320C54xx processor in various modes.
- Understand basic DSP algorithms with their implementation.

Module-1	RBT Level
Introduction to Digital Signal Processing: Introduction, A Digital Signal – Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation. **Computational Accuracy in DSP Implementations:** Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementation.	L1, L2
Module-2	
Architectures for Programmable Digital Signal – Processing Devices: Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.	L1, L2, L3
Module-3	
Programmable Digital Signal Processors: Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54XX, Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and Programming, On – Chip Peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor.	L1, L2, L3
Module-4	

Implementation of Basic DSP Algorithms: Introduction, The Q – notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case). **Implementation of FFT Algorithms:** Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit – Reversed Index. Generation & Implementation on the TMS32OC54xx.	L1, L2, L3
Module-5	
Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices: Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA). **Interfacing and Applications of DSP Processors:** Introduction, Synchronous Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System.	L1, L2, L3
Course Outcomes: At the end of this course, students would be able to • Comprehend the knowledge and concepts of digital signal processing techniques. • Apply the knowledge of DSP computational building blocks to achieve speed in DSP architecture or processor. • Apply knowledge of various types of addressing modes, interrupts, peripherals and pipelining structure of TMS320C54xx processor. • Develop basic DSP algorithms using DSP processors. • Discuss about synchronous serial interface and multichannel buffered serial port (McBSP) of DSP device. • Demonstrate the programming of CODEC interfacing.	
Question paper pattern: • The question paper will have 10 full questions carrying equal marks. • Each full question consists of 16 marks with a maximum of Three sub questions. • There will be 2 full questions from each module covering all the topics of the module • The students will have to answer 5 full questions, selecting one full question from each module.	
Text Book: "Digital Signal Processing", Avatar Singh and S. Srinivasan, Thomson Learning, 2004.	
Reference Books: 1. "Digital Signal Processing: A practical approach", Ifeachor E. C., Jervis B. W Pearson-Education, PHI, 2002. 2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2nd, 2010 3. "Architectures for Digital Signal Processing", Peter Pirsch John Weily, 2008	

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IoT & WIRELESS SENSOR NETWORKS

B.E., VII Semester, Electronics & Communication Engineering /Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC752	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Understand various sources of IoT & M2M communication protocols.
- Describe Cloud computing and design principles of IoT.
- Become aware of MQTT clients, MQTT server and its programming.
- Understand the architecture and design principles of WSNs.
- Enrich the knowledge about MAC and routing protocols in WSNs.

Module-1	RBT Level
Overview of Internet of Things: IoT Conceptual Framework, IoT Architectural View, Technology Behind IoT, Sources of IoT,M2M communication, Examples of IoT. Modified OSI Model for the IoT/M2M Systems, data enrichment, data consolidation and device management at IoT/M2M Gateway, web communication protocols used by connected IoT/M2M devices, Message communication protocols (CoAP-SMS, CoAP-MQ, MQTT,XMPP) for IoT/M2M devices.	L1, L2
Module-2	
Architecture and Design Principles for IoT: Internet connectivity, Internet-based communication,IPv4, IPv6,6LoWPAN protocol, IP Addressing in the IoT, Application layer protocols: HTTP, HTTPS,FTP,TELNET and ports. **Data Collection, Storage and Computing using a Cloud Platform:** Introduction, Cloud computing paradigm for data collection, storage and computing, Cloud service models, IoT Cloud- based data collection, storage and computing services using Nimbits.	L1, L2
Module-3	

Prototyping and Designing Software for IoT Applications: Introduction, Prototyping Embedded device software, Programming Embedded Device Arduino Platform using IDE, Reading data from sensors and devices, Devices, Gateways, Internet and Web/Cloud services software development. Programming MQTT clients and MQTT server. Introduction to IoT privacy and security. Vulnerabilities, security requirements and threat analysis, IoT Security Tomography and layered attacker model.	L1, L2, L3
Module-4	
Overview of Wireless Sensor Networks: Challenges for Wireless Sensor Networks, Enabling Technologies for Wireless Sensor Networks. **Architectures**: Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes, Operating Systems and Execution Environments, Network Architecture-Sensor Network Scenarios, Optimization Goals and Figures of Merit, Design principles for WSNs, Service interfaces of WSNs Gateway Concepts.	L1, L2, L3
Module-5	
Communication Protocols: Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Contention based protocols(CSMA,PAMAS), Schedule based protocols (LEACH, SMACS, TRAMA) Address and Name Management in WSNs, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing, Hierarchical networks by clustering.	L1, L2, L3
Course Outcomes: At the end of the course, students will be able to: • Describe the OSI Model for the IoT/M2M Systems. • Understand the architecture and design principles for IoT. • Learn the programming for IoT Applications. • Identify the communication protocols which best suits the WSNs.	
Question paper pattern: • The question paper will have ten questions. • Each full Question consisting of 16 marks. • There will be 2 full questions (with a maximum of Three sub questions) from each module. • Each full question will have sub questions covering all the topics under a module. • The students will have to answer 5 full questions, selecting one full question from each module.	

Text Books:

1. Raj Kamal, "Internet of Things-Architecture and design principles", McGraw Hill Education.
2. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless Sensor Networks" , John Wiley, 2005.
3. Feng Zhao & Leonidas J. Guibas, "Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.

Reference Books:

1. Kazem Sohraby, Daniel Minoli, & Taieb Znati, "Wireless Sensor Networks- Technology, Protocols, And Applications", John Wiley, 2007.
2. Anna Hac, "Wireless Sensor Network Designs", John Wiley, 2003.

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PATTERN RECOGNITION

B.E., VII Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC753	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Course Objectives: The objectives of this course are to:

- Introduce mathematical tools needed for Pattern Recognition
- Impart knowledge about the fundamentals of Pattern Recognition.
- Provide knowledge of recognition, decision making and statistical learning problems
- Introduce parametric and non-parametric techniques, supervised learning and clustering concepts of pattern recognition

Modules

Module-1	RBT Level
Introduction: Importance of pattern recognition, Features, Feature Vectors, and Classifiers, Supervised, Unsupervised, and Semi-supervised learning, Introduction to Bayes Decision Theory, Discriminant Functions and Decision Surfaces, Gaussian PDF and Bayesian Classification for Normal Distributions.	L1, L2
Module-2	
Data Transformation and Dimensionality Reduction: Introduction, Basis Vectors, The Karhunen Loeve (KL) Transformation, Singular Value Decomposition, Independent Component Analysis (Introduction only). Nonlinear Dimensionality Reduction, Kernel PCA.	L1, L2
Module-3	
Estimation of Unknown Probability Density Functions: Maximum Likelihood Parameter Estimation, Maximum a Posteriori Probability estimation, Bayesian Interference, Maximum Entropy Estimation, Mixture Models, Naive-Bayes Classifier, The Nearest Neighbor Rule.	L1, L2, L3
Module-4	
Linear Classifiers: Introduction, Linear Discriminant Functions and Decision Hyperplanes, The Perceptron Algorithm, Mean Square Error Estimate, Stochastic Approximation of LMS Algorithm, Sum of Error Estimate.	L1, L2, L3
Module-5	
Nonlinear Classifiers: The XOR Problem, The two Layer Perceptron, Three Layer Perceptron, Back propagation Algorithm, Basic Concepts of Clustering, Introduction to Clustering , Proximity Measures.	L1, L2, L3

Course outcomes: At the end of the course, students will be able to:

- Identify areas where Pattern Recognition and Machine Learning can offer a solution.
- Describe the strength and limitations of some techniques used in computational Machine Learning for classification, regression and density estimation problems
- Describe genetic algorithms, validation methods and sampling techniques
- Describe and model data to solve problems in regression and classification
- Implement learning algorithms for supervised tasks

Question paper pattern:

The question paper will have ten questions.

- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Pattern Recognition: Sergios Theodoridis, Konstantinos Koutroumbas, Elsevier India Pvt. Ltd (Paper Back), 4th edition.

Reference Books:

1. **The Elements of Statistical Learning:** Trevor Hastie, Springer-Verlag New York, LLC (Paper Back), 2009.
2. **Pattern Classification:** Richard O. Duda, Peter E. Hart, David G. Stork. John Wiley & Sons, 2012.
3. **Pattern Recognition and Image Analysis Earl Gose:** Richard Johnsonbaugh, Steve Jost, ePub eBook.

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ADVANCED COMPUTER ARCHITECTURE

B.E., VII Semester, Electronics & Communication Engineering /Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC754	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Course Objectives: This course will enable students to:

- Understand the various parallel computer models and conditions of parallelism
- Explain the control flow, dataflow and demand driven machines
- Study CISC, RISC, superscalar, VLIW and multiprocessor architectures
- Understand the concept of pipelining and memory hierarchy design
- Explain cache coherence protocols.

Module-1	RBT Level
Parallel Computer Models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputer, Multivectors and SIMD computers. **Program and Network Properties:** Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency.	L1, L2
Module-2	
Program flow mechanisms: Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms. **Principles of Scalable Performance**: Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches.	L1, L2, L3
Module-3	
Speedup Performance Laws: Amdhal's law, Gustafson's law, Memory bounded speed up model, Scalability Analysis and Approaches. **Advanced Processors:** Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures.	L1, L2, L3
Module-4	
Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design. **Memory Hierarchy Design:** Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.	L1, L2, L3

Module-5	
Multiprocessor Architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols.	L1, L2, L3

Course Outcomes: At the end of the course, the students will be able to:

- Explain parallel computer models and conditions of parallelism
- Differentiate control flow, dataflow, demand driven mechanisms
- Explain the principle of scalable performance
- Discuss advanced processors architectures like CISC, RISC, superscalar and VLIW
- Understand the basics of instruction pipelining and memory technologies
- Explain the issues in multiprocessor architectures

Question paper pattern:

The question paper will have ten questions.

- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Kai Hwang, "Advanced computer architecture"; TMH.

Reference Books:

1. Kai Hwang and Zu, "Scalable Parallel Computers Architecture"; MGH.
2. M.J Flynn, "Computer Architecture, Pipelined and Parallel Processor Design"; Narosa Publishing.
3. D.A.Patterson, J.L.Hennessy, "Computer Architecture :A quantitative approach"; Morgan Kauffmann Feb, 2002.

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SATELLITE COMMUNICATION

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS)]

Subject Code	15EC755	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to

- Understand the basic principle of satellite orbits and trajectories.
- Study of electronic systems associated with a satellite and the earth station.
- Understand the various technologies associated with the satellite communication.
- Focus on a communication satellite and the national satellite system.
- Study of satellite applications focusing various domains services such as remote sensing, weather forecasting and navigation.

Module-1	RBT Level
Satellite Orbits and Trajectories: Definition, Basic Principles, Orbital parameters, Injection velocity and satellite trajectory, Types of Satellite orbits, Orbital perturbations, Satellite stabilization, Orbital effects on satellite's performance, Eclipses, Look angles: Azimuth angle, Elevation angle.	L1, L2
Module-2	
Satellite subsystem: Power supply subsystem, Attitude and Orbit control, Tracking, Telemetry and command subsystem, Payload. **Earth Station:** Types of earth station, Architecture, Design considerations, Testing, Earth station Hardware, Satellite tracking.	L1, L2
Module-3	
Multiple Access Techniques: Introduction, FDMA (No derivation), SCPC Systems, MCPC Systems, TDMA, CDMA, SDMA. **Satellite Link Design Fundamentals:** Transmission Equation, Satellite Link Parameters, Propagation considerations.	L1, L2, L3
Module-4	
Communication Satellites: Introduction, Related Applications, Frequency Bands, Payloads, Satellite Vs. Terrestrial Networks, Satellite Telephony, Satellite Television, Satellite radio, Regional satellite Systems, National Satellite Systems.	L1, L2
Module-5	

Remote Sensing Satellites: Classification of remote sensing systems, orbits, Payloads, Types of images: Image Classification, Interpretation, Applications. **Weather Forecasting Satellites**: Fundamentals, Images, Orbits, Payloads, Applications. **Navigation Satellites**: Development of Satellite Navigation Systems, GPS system, Applications.	L1, L2, L3

Course Outcomes: At the end of the course, the students will be able to:

- Describe the satellite orbits and its trajectories with the definitions of parameters associated with it.
- Describe the electronic hardware systems associated with the satellite subsystem and earth station.
- Describe the various applications of satellite with the focus on national satellite system.
- Compute the satellite link parameters under various propagation conditions with the illustration of multiple access techniques.

Question Paper pattern:

- The Question paper will have ten questions.
- Each full Question consisting of 16 marks
- There will be 2 full Questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The Students will have to answer 5 full Questions, selecting one full Question from each module.

Text Book:

Anil K. Maini, Varsha Agrawal, Satellite Communications, Wiley India Pvt. Ltd., 2015, ISBN: 978-81-265-2071-8.

Reference Books :

1. Dennis Roddy, Satellite Communications, 4th Edition, McGraw- Hill International edition, 2006
2. Timothy Pratt, Charles Bostian, Jeremy Allnutt, Satellite Communications, 2nd Edition, Wiley India Pvt. Ltd , 2017, ISBN: 978-81-265-0833-4

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ADVANCED COMMUNICATION LAB

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15ECL76	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory = 03	Exam Marks	80
RBT Levels	L1, L2, L3	Exam Hours	03

CREDITS – 02

Course objectives: This course will enable students to:

- Design and demonstrate the digital modulation techniques
- Demonstrate and measure the wave propagation in microstrip antennas
- Characteristics of microstrip devices and measurement of its parameters.
- Model an optical communication system and study its characteristics.
- Simulate the digital communication concepts and compute and display various parameters along with plots/figures.

Laboratory Experiments

PART-A: Following Experiments No. 1 to 4 has to be performed using discrete components.

1. Time Division Multiplexing and Demultiplexing of two bandlimited signals.
2. ASK generation and detection
3. FSK generation and detection
4. PSK generation and detection
5. Measurement of frequency, guide wavelength, power, VSWR and attenuation in microwave test bench.
6. Measurement of directivity and gain of microstrip dipole and Yagi antennas.
7. Determination of
   a. Coupling and isolation characteristics of microstrip directional coupler.
   b. Resonance characteristics of microstrip ring resonator and computation of dielectric constant of the substrate.
   c. Power division and isolation of microstrip power divider.
8. Measurement of propagation loss, bending loss and numerical aperture of an optical fiber.

PART-B: Simulation Experiments using SCILAB/MATLAB/Simulink or LabView
1. Simulate NRZ, RZ, half-sinusoid and raised cosine pulses and generate eye diagram for binary polar signaling. 2. Simulate the Pulse code modulation and demodulation system and display the waveforms. 3. Simulate the QPSK transmitter and receiver. Plot the signals and its constellation diagram. 4. Test the performance of a binary differential phase shift keying system by simulating the non-coherent detection of binary DPSK.
Course outcomes: On the completion of this laboratory course, the students will be able to: • Determine the characteristics and response of microwave devices and optical waveguide. • Determine the characteristics of microstrip antennas and devices and compute the parameters associated with it. • Simulate the digital modulation schemes with the display of waveforms and computation of performance parameters. • Design and test the digital modulation circuits/systems and display the waveforms.
Conduct of Practical Examination: • All laboratory experiments are to be considered for practical examination. • For examination one question from **PART-A** and one question from **PART-B or** only one question from **PART-B** experiments based on the complexity, to be set. • Students are allowed to pick one experiment from the lot. • Strictly follow the instructions as printed on the cover page of answer script for breakup of marks. • Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

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VLSI LAB

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15ECL77	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory = 03	Exam Marks	80
RBT Levels	L1, L2, L3	Exam Hours	03

CREDITS – 02

Course objectives: This course will enable students to:

- Explore the CAD tool and understand the flow of the Full Custom IC design cycle.
- Learn DRC, LVS and Parasitic Extraction of the various designs.
- Design and simulate the various basic CMOS analog circuits and use them in higher circuits like data converters using design abstraction concepts.
- Design and simulate the various basic CMOS digital circuits and use them in higher circuits like adders and shift registers using design abstraction concepts.

Experiments can be conducted using any of the following or equivalent design tools: Cadence/Synopsis/Mentor Graphics/Microwind

Laboratory Experiments

PART - A

ASIC-DIGITAL DESIGN

1. Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with technological library with given constraints*. Do the initial timing verification with gate level simulation.
   i. An inverter
   ii. A Buffer
   iii. Transmission Gate
   iv. Basic/universal gates
   v. Flip flop -RS, D, JK, MS, T
   vi. Serial & Parallel adder
   vii. 4-bit counter [Synchronous and Asynchronous counter]
   viii. Successive approximation register [SAR]

PART - B
ANALOG DESIGN

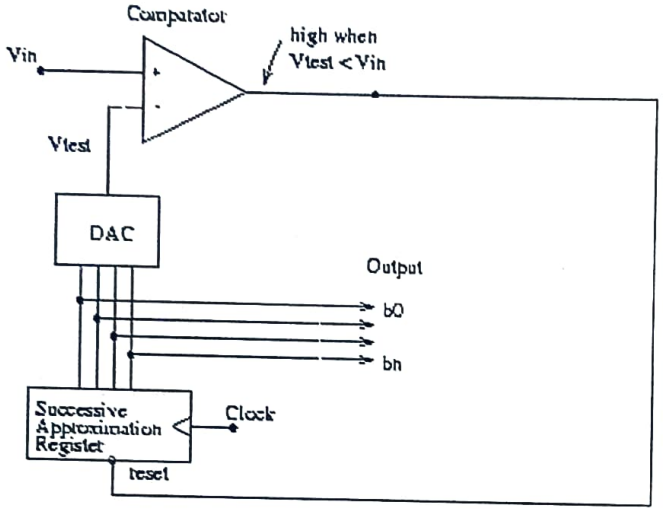
1. Design an Inverter with given specifications**, completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design
   e. Verify & Optimize for Time, Power and Area to the given constraint*

2. Design the (i) Common source and Common Drain amplifier and (ii) A Single Stage differential amplifier, with given specifications**, completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design.

3. Design an op-amp with given specification** using given differential amplifier Common source and Common Drain amplifier in library*** and completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii). AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design.

4. Design a 4 bit R-2R based DAC for the given specification and completing the design flow mentioned using given op-amp in the library***.
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC

5. For the SAR based ADC mentioned in the figure below draw the mixed signal schematic and verify the functionality by completing ASIC Design FLOW. [Specifications to GDS-II]



* An appropriate constraint should be given.

** Appropriate specification should be given.

*** Applicable Library should be added & information should be given to the Designer.

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Write test bench to simulate various digital circuits.
- Interpret concepts of DC Analysis, AC Analysis and Transient Analysis in analog circuits.
- Design and simulate basic CMOS circuits like inverter, common source amplifier and differential amplifiers.
- Use basic amplifiers and further design higher level circuits like operational amplifier and analog/digital converters to meet desired parameters.
- Use transistors to design gates and further using gates realize shift registers and adders to meet desired parameters.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination, one question from **PART-A** and one question from **PART-B** to be set.
- Students are allowed to pick one experiment from the lot.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

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B.E E&C EIGTH SEMESTER SYLLABUS

Wireless Cellular and LTE 4G Broadband

B.E., VIII Semester, Electronics &Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC81	IA Marks	20
Number of Lecture	04	Exam Marks	80
Total Number	50 (10 Hours / Module)	Exam Hours	03

CREDITS – 04

Course Objectives: This course will enable students to:

- Understand the basics of LTE standardization phases and specifications.
- Explain the system architecture of LTE and E-UTRAN, the layer of LTE, based on the use of OFDMA and SC-FDMA principles.
- Analyze the role of LTE radio interface protocols to set up, reconfigure and release the Radio Bearer, for transferring the EPS bearer.
- Analyze the main factors affecting LTE performance including mobile speed and transmission bandwidth.

Module – 1	**RBT Level**
Key Enablers for LTE features: OFDM, Single carrier FDMA, Single carrier FDE, Channel Dependent Multiuser Resource Scheduling, Multi antenna Techniques, IP based Flat network Architecture, LTE Network Architecture. (Sec 1.4- 1.5 of Text). **Wireless Fundamentals:** Cellular concept, Broadband wireless channel (BWC), Fading in BWC, Modeling BWC – Empirical and Statistical models, Mitigation of Narrow band and Broadband Fading (Sec 2.2 – 2.7of Text).	L1, L2
Module – 2	
Multicarrier Modulation: OFDM basics, OFDM in LTE, Timing and Frequency Synchronization, PAR, SC-FDE (Sec 3.2 – 3.6 of Text). **OFDMA and SC-FDMA:**OFDM with FDMA,TDMA,CDMA, OFDMA, SC-FDMA, OFDMA and SC-FDMA in LTE (Sec 4.1 – 4.3, 4.5 of Text). **Multiple Antenna Transmission and Reception:** Spatial Diversity overview, Receive Diversity, Transmit Diversity, Interference cancellation and signal enhancement, Spatial Multiplexing, Choice between Diversity, Interference suppression and Spatial Multiplexing (Sec 5.1 – 5.6 of Text).	L1, L2
Module – 3	
Overview and Channel Structure of LTE: Introduction to LTE, Channel Structure of LTE, Downlink OFDMA Radio Resource, Uplink	L1, L2

SC-FDMA Radio Resource(Sec 6.1 – 6.4 of Text). . **Downlink Transport Channel Processing:** Overview, Downlink shared channels, Downlink Control Channels, Broadcast channels, Multicast channels, Downlink physical channels, H-ARQ on Downlink(Sec 7.1 – 7.7 of Text).	
Module – 4	
Uplink Channel Transport Processing: Overview, Uplink shared channels, Uplink Control Information, Uplink Reference signals, Random Access Channels, H-ARQ on uplink (Sec 8.1 – 8.6 of Text). **Physical Layer Procedures:** Hybrid – ARQ procedures, Channel Quality Indicator CQI feedback, Precoder for closed loop MIMO Operations, Uplink channel sounding, Buffer status Reporting in uplink, Scheduling and Resource Allocation, Cell Search, Random Access Procedures, Power Control in uplink(Sec 9.1- 9.6, 9.8, 9.9, 9.10 Text).	L1, L2
Module – 5	
Radio Resource Management and Mobility Management: PDCP overview, MAC/RLC overview, RRC overview, Mobility Management, Inter-cell Interference Coordination(Sec 10.1 – 10.5 of Text).	L1, L2

Course Outcomes: At the end of the course, students will be able to:

- Understand the system architecture and the functional standard specified in LTE 4G.
- Analyze the role of LTE radio interface protocols and EPS Data convergence protocols to set up, reconfigure and release data and voice from users.
- Demonstrate the UTRAN and EPS handling processes from set up to release including mobility management for a variety of data call scenarios.
- Test and Evaluate the Performance of resource management and packet data processing and transport algorithms.

Question Paper pattern:

- The Question paper will have ten questions.
- Each full Question consisting of 16 marks
- There will be 2 full Questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The Students will have to answer 5 full Questions, selecting one full Question from each module.

Text Book:

Arunabha Ghosh, Jan Zhang, Jefferey Andrews, Riaz Mohammed, 'Fundamentals of LTE', Prentice Hall, Communications Engg. and Emerging Technologies.

Reference Books:

1. LTE for UMTS Evolution to LTE-Advanced' Harri Holma and Antti Toskala, Second Edition - 2011, John Wiley & Sons, Ltd. Print ISBN: 9780470660003.
2. 'EVOLVED PACKET SYSTEM (EPS) ; THE LTE AND SAE EVOLUTION OF 3G UMTS' by Pierre Lescuyer and Thierry Lucidarme, 2008, John Wiley & Sons, Ltd. Print ISBN:978-0-470-05976-0.
3. 'LTE – The UMTS Long Term Evolution ; From Theory to Practice' by Stefania Sesia, Issam Toufik, and Matthew Baker, 2009 John Wiley & Sons Ltd, ISBN 978-0-470-69716-0.

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FIBER OPTICS and NETWORKS

B.E., VIII Semester, Electronics &Communication Engineering

[As per Choice Based Credit System (CBCS)]

Subject Code	15EC82	IA Marks	20
Number of Lecture Hours/Week	4	Exam Marks	80
Total Number of Lecture Hours	50(10 Hours / Module)	Exam Hours	03
CREDITS – 04			

Course Objectives: This course will enable students to:

- Learn the basic principle of optical fiber communication with different modes of light propagation.
- Understand the transmission characteristics and losses in optical fiber.
- Study of optical components and its applications in optical communication networks.
- Learn the network standards in optical fiber and understand the network architectures along with its functionalities.

Module -1	**RBT Level**
Optical fiber Communications: Historical development, The general system, Advantages of optical fiber communication, Optical fiber waveguides: Ray theory transmission, Modes in planar guide, Phase and group velocity, Cylindrical fiber: Modes, Step index fibers, Graded index fibers, Single mode fibers, Cutoff wavelength, Mode field diameter, effective refractive index. Fiber Materials, Photonic crystal fibers. (Text 2)	L1, L2
Module -2	
Transmission characteristics of optical fiber: Attenuation, Material absorption losses, Linear scattering losses, Nonlinear scattering losses, Fiber bend loss, Dispersion, Chromatic dispersion, Intermodal dispersion: Multimode step index fiber. **Optical Fiber Connectors:** Fiber alignment and joint loss, Fiber splices, Fiber connectors, Fiber couplers. (Text 2)	L1, L2
Module -3	
Optical sources: Energy Bands, Direct and Indirect Bandgaps, Light Emitting diodes: LED Structures, Light Source Materials, Quantum Efficiency and LED Power, Modulation. Laser Diodes: Modes and Threshold conditions, Rate equation, External Quantum Efficiency, Resonant frequencies, Laser Diode structures and Radiation Patterns: Single mode lasers. **Photodetectors:** Physical principles of Photodiodes, Photodetector noise, Detector response time. **Optical Receiver:** Optical Receiver Operation: Error sources,	L1, L2

Front End Amplifiers, Receiver sensitivity, Quantum Limit. (Text 1)	
Module -4	
WDM Concepts and Components: Overview of WDM: Operational Principles of WDM, WDM standards, Mach-Zehnder Interferometer Multiplexers, Isolators and Circulators, Fiber grating filters, Dielectric Thin-Film Filters, Diffraction Gratings, Active Optical Components, Tunable light sources, **Optical amplifiers:** Basic application and Types, Semiconductor optical amplifiers, Erbium Doped Fiber Amplifiers, Raman Amplifiers, Wideband Optical Amplifiers. (Text 1)	L1, L2
Module -5	
Optical Networks: Optical network evolution and concepts: Optical networking terminology, Optical network node and switching elements, Wavelength division multiplexed networks, Public telecommunication network overview. Optical network transmission modes, layers and protocols: Synchronous networks, Asynchronous transfer mode, OSI reference model, Optical transport network, Internet protocol, Wavelength routing networks: Routing and wavelength assignment, Optical switching networks: Optical circuit switched networks, packet switched networks, Multiprotocol Label Switching, Optical burst switching networks, Optical network deployment: Long-haul networks, Metropoliton area networks, Access networks, Local area networks. (Text 2)	L1, L2

Course Outcomes: At the end of the course, students will be able to:

1. Classification and working of optical fiber with different modes of signal propagation.
2. Describe the transmission characteristics and losses in optical fiber communication.
3. Describe the construction and working principle of optical connectors, multiplexers and amplifiers.
4. Describe the constructional features and the characteristics of optical sources and detectors.
5. Illustrate the networking aspects of optical fiber and describe various standards associated with it.

Question Paper pattern:

- The Question paper will have ten questions.
- Each full Question consisting of 16 marks
- There will be 2 full Questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The Students will have to answer 5 full Questions, selecting one full Question from each module.

Text Books:

1. Gerd Keiser , Optical Fiber Communication, 5th Edition, McGraw Hill

Education(India) Private Limited, 2015. ISBN:1-25-900687-5.
2. John M Senior, Optical Fiber Communications, Principles and Practice, 3rd Edition, Pearson Education, 2010, ISBN:978-81-317-3266-3

Reference Book:

Joseph C Palais, Fiber Optic Communication , Pearson Education, 2005, ISBN:0130085103

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