1. **Modern Digital and Analog Communication Systems,** B. P. Lathi, Oxford University Press., 4th edition.
2. **An Introduction to Analog and Digital Communication**, Simon Haykins, John Wiley India Pvt. Ltd., 2008, ISBN 978–81–265–3653–5.
3. **Principles of Communication Systems**, H.Taub & D.L.Schilling, TMH, 2011.
4. **Communication Systems**, Harold P.E, Stern Samy and A.Mahmond, Pearson Edition, 2004.
5. **Communication Systems: Analog and Digital,** R.P.Singh and S.Sapre: TMH 2nd edition, 2007.

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**LINEAR INTEGRATED CIRCUITS**

[As per Choice Based Credit System (CBCS) scheme]

**SEMESTER – IV (EC/TC)**

| | | | |
|---|---|---|---|
| Subject Code | 15EC46 | IA Marks | 20 |
| Number of Lecture Hours/Week | 04 | Exam Marks | 80 |
| Total Number of Lecture Hours | 50(10 Hours per Module) | Exam Hours | 03 |

CREDITS – 04

**Course objectives:** This course will enable students to:

- Define and describe various parameters of Op-Amp, its characteristics and specifications.
- Discuss the effects of Input and Output voltage ranges upon Op-Amp circuits.
- Sketch and Analyze Op-Amp circuits to determine Input Impedances, output Impedances and other performance parameters.
- Sketch and Explain typical Frequency Response graphs for each of the Filter circuits showing Butterworth and Chebyshev responses where ever appropriate.
- Describe and Sketch the various switching circuits of Op-Amps and analyze its operations.
- Differentiate between various types of DACs and ADCs and evaluate the performance of each with neat circuit diagrams and assuming suitable inputs.

| Modules | RBT Level |
|---|---|
| **Module -1** | |
| **Operational Amplifier Fundamentals:** Basic Op-amp circuit, Op-Amp parameters – Input and output voltage, CMRR and PSRR, offset voltages and currents, Input and output impedances, Slew rate and Frequency limitations. **OP-Amps as DC Amplifiers** – Biasing OP-amps, Direct coupled voltage followers, Non-inverting amplifiers, inverting amplifiers, Summing amplifiers, and Difference amplifiers. Interpretation of OP-amp LM741 & TL081 datasheet.**(Text1)** | **L1, L2,L3** |
| **Module -2** | |
| **Op-Amps as AC Amplifiers:** Capacitor coupled voltage follower, High input impedance – Capacitor coupled voltage follower, Capacitor coupled non inverting amplifiers, High input impedance – Capacitor coupled Non inverting amplifiers, Capacitor coupled inverting amplifiers, setting the upper cut-off frequency, Capacitor coupled difference amplifier. **OP-Amp Applications:** Voltage sources, current sources and current sinks, current amplifiers, instrumentation amplifier, precision rectifiers.**(Text1)** | **L1, L2,L3** |
| **Module-3** | |
| **More Applications :** Limiting circuits, Clamping circuits, Peak detectors, Sample and hold circuits, V to I and I to V converters, Differentiating Circuit, Integrator Circuit, Phase shift oscillator, Wien bridge oscillator, Crossing detectors, inverting Schmitt trigger. **(Text 1)** Log and antilog amplifiers, Multiplier and divider. **(Text2)** | **L1, L2,L3** |

| Module -4 | |
|---|---|
| **Active Filters:** First order and second order active Low-pass and high pass filters, Bandpass Filter, Bandstop Filter.<br>**(Text 1)**<br>**Voltage Regulators:** Introduction, Series Op-amp regulator, IC voltage regulators. 723 general purpose regulators.<br>**(Text 2)** | **L1, L2,L3** |
| **Module -5** | |
| **Phase locked loop:** Basic Principles, Phase detector/comparator, VCO.<br>**DAC and ADC convertor**: DAC using R-2R, ADC using Successive approximation.<br>**Other IC Application:** 555 timer, Basic timer circuit, 555 timer used as astable and monostable multivibrator.<br>**(Text 2)** | **L1, L2,L3** |

**Course Outcomes:** After studying this course, students will be able to:

- Explain Op-Amp circuit and parameters including CMRR, PSRR, Input & Output Impedances and Slew Rate.
- Design Op-Amp based Inverting, Non-inverting, Summing & Difference Amplifier, and AC Amplifiers including Voltage Follower.
- Test circuits of Op-Amp based Voltage/ Current Sources & Sinks, Current, Instrumentation and Precision Amplifiers.
- Test circuits of Op-Amp based linear and non-linear circuits comprising of limiting, clamping, Sample & Hold, Differentiator/ Integrator Circuits, Peak Detectors, Oscillators and Multiplier & Divider.
- Design first & second order Low Pass, High Pass, Band Pass, Band Stop Filters and Voltage Regulators using Op-Amps.
- Explain applications of linear ICs in phase detector, VCO, DAC, ADC and Timer.

**Question paper pattern:**

- The question paper will have ten questions.
- Each full Question consisting of 16 marks.
- There will be 2 full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Books:**


1. "Operational Amplifiers and Linear IC's", David A. Bell, 2nd edition, PHI/Pearson, 2004. ISBN 978-81-203-2359-9.
2. "Linear Integrated Circuits", D. Roy Choudhury and Shail B. Jain, 4th edition, Reprint 2006, New Age International ISBN 978-81-224-3098-1.

**Reference Books:**


1. Ramakant A Gayakwad, "Op-Amps and Linear Integrated Circuits", Pearson, 4th Ed, 2015. ISBN 81-7808-501-1.
2. B Somanathan Nair, "Linear Integrated Circuits: Analysis, Design & Applications," Wiley India, 1st Edition, 2015.
3. James Cox, "Linear Electronics Circuits and Devices", Cengage Learning, Indian Edition, 2008, ISBN-13: 978-07-668-3018-7.
4. Data Sheet: http://www.ti.com/lit/ds/symlink/tl081.pdf.


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## MICROPROCESSOR LABORATORY

[As per Choice Based Credit System (CBCS) scheme]

**SEMESTER – IV (EC/TC)**

| | | | |
|---|---|---|---|
| Laboratory Code | 15ECL47 | IA Marks | 20 |
| Number of Lecture Hours/Week | 01Hr Tutorial (Instructions) + 02 Hours Laboratory | Exam Marks | 80 |
| RBT Level | L1, L2, L3 | Exam Hours | 03 |

CREDITS – 02

**Course objectives:** This course will enable students to:

- Get familiarize with 8086 instructions and DOS 21H interrupts and function calls.
- Develop and test assembly language programs to use instructions of 8086.
- Get familiarize with interfacing of various peripheral devices with 8086 microprocessor for simple applications.

**Laboratory Experiments:**

**1. Programs involving:**

**Data transfer instructions like**:

i) Byte and word data transfer in different addressing Modes
ii) Block move (with and without overlap)
iii) Block interchange

**2. Programs involving:**

**Arithmetic & logical operations like**:

i) Addition and Subtraction of multi precision nos.
ii) Multiplication and Division of signed and unsigned Hexadecimal nos.
iii) ASCII adjustment instructions.
iv) Code conversions.

**3. Programs involving:**

**Bit manipulation instructions like checking**:

i) Whether given data is positive or negative
ii) Whether given data is odd or even
iii) Logical 1's and 0's in a given data
iv) 2 out 5 code
v) Bit wise and nibble wise palindrome

**4. Programs involving:**

**Branch/ Loop instructions like**

i) Arrays: addition/subtraction of N nos., Finding largest and smallest nos., Ascending and descending order.
ii) Two application programs using Procedures and Macros (Subroutines).

**5. Programs involving**

String manipulation like string transfer, string reversing, searching for a string.

**6. Programs involving**

Programs to use DOS interrupt INT 21h Function calls for Reading a Character from keyboard, Buffered Keyboard input, Display of character/ String on console.

**7. Interfacing Experiments:**

Experiments on interfacing 8086 with the following interfacing modules through DIO (Digital Input/Output - PCI bus compatible card / 8086 Trainer )

1. Matrix keyboard interfacing
2. Seven segment display interface
3. Logical controller interface
4. Stepper motor interface
5. ADC and DAC Interface (8 bit)
6. Light dependent resistor (LDR), Relay and Buzzer Interface to make light operated switches

**Course Outcomes:** On the completion of this laboratory course, the students will be able to:

- Write and execute 8086 assembly level programs to perform data transfer, arithmetic and logical operations.
- Understand assembler directives, branch, loop operations and DOS 21H Interrupts.
- Write and execute 8086 assembly level programs to sort and search elements in a given array.
- Perform string transfer, string reversing, searching a character in a string with string manipulation instructions of 8086.
- Utilize procedures and macros in programming 8086.
- Demonstrate the interfacing of 8086 with 7 segment display, matrix keyboard, logical controller, stepper motor, ADC, DAC, and LDR for simple applications.

**Conduct of Practical Examination:**

- All laboratory experiments are to be included for practical examination.
- For examination, one question from software and one question from hardware interfacing to be set.
- Students are allowed to pick one experiment from the lot.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

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## LINEAR ICS AND COMMUNICATION LAB

As per Choice Based Credit System (CBCS) scheme]

**SEMESTER – IV (EC/TC)**

| | | | |
|---|---|---|---|
| Laboratory Code | 15ECL48 | IA Marks | 20 |
| Number of Lecture Hours/Week | 01Hr Tutorial (Instructions) + 02 Hours Laboratory | Exam Marks | 80 |
| RBT Level | L1, L2, L3 | Exam Hours | 03 |

CREDITS – 02

**Course objectives:** This laboratory course enables students to:

- Design, Demonstrate and Analyze instrumentation amplifier, filters, DAC, adder, differentiator and integrator circuits, using op-amp.
- Design, Demonstrate and Analyze multivibrators and oscillator circuits using Op-amp
- Design, Demonstrate and Analyze analog systems for AM, FM and Mixer operations.
- Design, Demonstrate and Analyze balance modulation and frequency synthesis.
- Demonstrate and Analyze pulse sampling and flat top sampling.

**Laboratory Experiments:**

1. Design an instrumentation amplifier of a differential mode gain of 'A' using three amplifiers.
2. Design of RC Phase shift and Wien's bridge oscillators using Op-amp.
3. Design active second order Butterworth low pass and high pass filters.
4. Design 4 bit R – 2R Op-Amp Digital to Analog Converter (i) using 4 bit binary input from toggle switches and (ii) by generating digital inputs using mod-16 counter.
5. Design Adder, Integrator and Differentiator using Op-Amp.
6. Design of Monostable and Astable Multivibrator using 555 Timer.
7. Demonstrate Pulse sampling, flat top sampling and reconstruction.
8. Amplitude modulation using transistor/FET (Generation and detection).
9. Frequency modulation using IC 8038/2206 and demodulation.
10. Design BJT/FET Mixer.
11. DSBSC generation using Balance Modulator IC 1496/1596.
12. Frequency synthesis using PLL.

**Course Outcomes:** This laboratory course enables students to:

- Illustrate the pulse and flat top sampling techniques using basic circuits.
- Demonstrate addition and integration using linear ICs, and 555 timer operations to generate signals/pulses.
- Demonstrate AM and FM operations and frequency synthesis.
- Design and illustrate the operation of instrumentation amplifier, LPF, HPF, DAC and oscillators using linear IC.

**Conduct of Practical Examination:**

- All laboratory experiments are to be included for practical examination.
- Students are allowed to pick one experiment from the lot.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

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## B.E E&C FIFTH SEMESTER SYLLABUS

## MANAGEMENT AND ENTREPRENEURSHIP DEVELOPMENT

**B.E., V Semester, EC/TC/EI/BM/ML**

[As per Choice Based Credit System (CBCS) scheme]

| | | | |
|---|---|---|---|
| Subject Code | 15ES51 | IA Marks | 20 |
| Number of Lecture Hours/Week | 04 | Exam Marks | 80 |
| Total Number of Lecture Hours | 50 (10 Hours / Module) | Exam Hours | 03 |
| CREDITS – 04 | | | |

**Course Objectives:** This course will enable students to:

- Understand basic skills of Management
- Understand the need for Entrepreneurs and their skills
- Understand Project identification and Selection
- Identify the Management functions and Social responsibilities
- Distinguish between management and administration

| Module-1 | RBT Level |
|---|---|
| **Management:** Nature and Functions of Management – Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management & Administration, Management as a Science, Art & Profession (Selected topics of Chapter 1, Text 1).<br><br>**Planning:** Planning-Nature, Importance, Types, Steps and Limitations of Planning; Decision Making – Meaning, Types and Steps in Decision Making(Selected topics from Chapters 4 & 5, Text 1). | L1, L2 |
| **Module-2** | |
| **Organizing and Staffing: Organization**-Meaning, Characteristics, Process of Organizing, Principles of Organizing, Span of Management (meaning and importance only), Departmentalisation, Committees–Meaning, Types of Committees; Centralization Vs Decentralization of Authority and Responsibility; **Staffing**-Need and Importance, Recruitment and Selection Process (Selected topics from Chapters 7, 8 & 11,Text 1).<br><br>**Directing and Controlling:** Meaning and Requirements of Effective Direction, Giving Orders; Motivation-Nature of Motivation, Motivation Theories (Maslow's Need-Hierarchy Theory and Herzberg's Two Factor Theory); Communication – Meaning, Importance and Purposes of Communication; Leadership-Meaning, Characteristics, Behavioural Approach of Leadership; Coordination-Meaning, Types, Techniques of Coordination; Controlling – Meaning, Need for Control System, Benefits of Control, Essentials of Effective Control System, Steps in Control Process (Selected topics from Chapters 15 to 18 and 9, Text 1). | L1, L2 |
| **Module-3** | |
| **Social Responsibilities of Business:** Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance (Selected topics from Chapter 3, Text 1). | L1, L2 |

| | |
|---|---|
| **Entrepreneurship**: Definition of Entrepreneur, Importance of Entrepreneurship, concepts of Entrepreneurship, Characteristics of successful Entrepreneur, Classification of Entrepreneurs, Myths of Entrepreneurship, Entrepreneurial Development models, Entrepreneurial development cycle, Problems faced by Entrepreneurs and capacity building for Entrepreneurship (Selected topics from Chapter 2, Text 2). | |
| **Module-4** | |
| **Modern Small Business Enterprises:** Role of Small Scale Industries, Impact of Globalization and WTO on SSIs, Concepts and definitions of SSI Enterprises, Government policy and development of the Small Scale sector in India, Growth and Performance of Small Scale Industries in India, Sickness in SSI sector, Problems for Small Scale Industries, Ancillary Industry and Tiny Industry (Definition only)(Selected topics from Chapter1, Text 2).<br><br>**Institutional Support for Business Enterprises:** Introduction, Policies & Schemes of Central Level Institutions, State Level Institutions (Selected topics from Chapter 4, Text 2). | L1, L2 |
| **Module-5** | |
| **Projects Management:** AProject. Search for a Business idea: Introduction, Choosing an Idea, Selection of product, The Adoption process, Product Innovation, Product Planning and Development Strategy, Product Planning and Development Process. Concepts of Projects and Classification: Introduction, Meaning of Projects, Characteristics of a Project, Project Levels, Project Classification, Aspects of a Project, The project Cycle, Features and Phases of Project management, Project Management Processes. Project Identification: Feasibility Report, Project Feasibility Analysis. Project Formulation: Meaning, Steps in Project formulation, Sequential Stages of Project Formulation, Project Evaluation.<br><br>**Project Design and Network Analysis:** Introduction, Importance of Network Analysis, Origin of PERT and CPM, Network, Network Techniques, Need for Network Techniques, Steps in PERT, CPM, Advantages, Limitations and Differences.<br><br>(Selected topics from Chapters 16 to 20 of Unit 3, Text 3). | L1, L2, L3 |

**Course Outcomes:** After studying this course, students will be able to:

- Understand the fundamental concepts of Management and Entrepreneurship
- Select a best Entrepreneurship model for the required domain of establishment
- Describe the functions of Managers, Entrepreneurs and their social responsibilities
- Compare various types of Entrepreneurs
- Analyze the Institutional support by various state and central government agencies

**Question paper pattern**

- The question paper will have TEN questions.
- Each full question carries 16 marks.
- There will be two full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Books:**

1. Principles of Management – P.C Tripathi, P.N Reddy, McGraw Hill Education, 6th Edition, 2017. ISBN-13:978-93-5260-535-4.
2. Entrepreneurship Development Small Business Enterprises- Poornima M Charantimath, Pearson Education 2008, ISBN 978-81-7758-260-4.
3. Dynamics of Entrepreneurial Development and Management by Vasant Desai. HPH 2007, ISBN: 978-81-8488-801-2.

**Reference Book:**

Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93-392-2286-4.

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# DIGITAL SIGNAL PROCESSING

**B.E., V Semester, Electronics & Communication Engineering / Telecommunication Engineering**

[As per Choice Based Credit System (CBCS) scheme]

| | | | |
|---|---|---|---|
| Subject Code | 15EC52 | IA Marks | 20 |
| Number of Lecture Hours/Week | 04 | Exam Marks | 80 |
| Total Number of Lecture Hours | 50 (10 Hours / Module) | Exam Hours | 03 |
| CREDITS – 04 | | | |

**Course objectives:** This course will enable students to

- Understand the frequency domain sampling and reconstruction of discrete time signals.
- Study the properties and the development of efficient algorithms for the computation of DFT.
- Realization of FIR and IIR filters in different structural forms.
- Learn the procedures to design of IIR filters from the analog filters using impulse invariance and bilinear transformation.
- Study the different windows used in the design of FIR filters and design appropriate filters based on the specifications.

**Modules**

| **Module-1** | **RBT Level** |
|---|---|
| Discrete Fourier Transforms (DFT): Frequency domain sampling and reconstruction of discrete time signals. DFT as a linear transformation, its relationship with other transforms. Properties of DFT, multiplication of two DFTs- the circular convolution. | L1, L2 |
| **Module-2** | |
| Additional DFT properties, use of DFT in linear filtering, overlap-save and overlap-add method. Fast-Fourier-Transform (FFT) algorithms: Direct computation of DFT, need for efficient computation of the DFT (FFT algorithms). | L1, L2, L3 |
| **Module-3** | |
| Radix-2 FFT algorithm for the computation of DFT and IDFT–decimation-in-time and decimation-in-frequency algorithms. Goertzel algorithm, and chirp-z transform. | L1, L2, L3 |
| **Module-4** | |
| Structure for IIR Systems: Direct form, Cascade form, Parallel form structures.<br>IIR filter design: Characteristics of commonly used analog filter – Butterworth and Chebyshev filters, analog to analog frequency transformations.<br>Design of IIR Filters from analog filter using Butterworth filter: Impulse invariance, Bilinear transformation. | L1, L2, L3 |
| **Module-5** | |
| Structure for FIR Systems: Direct form, Linear Phase, Frequency sampling | L1, L2, |

| | |
|---|---|
| structure, Lattice structure.<br>FIR filter design: Introduction to FIR filters, design of FIR filters using - Rectangular, Hamming, Hanning and Bartlett windows. | L3 |

**Course Outcomes:** After studying this course, students will be able to:

- Determine response of LTI systems using time domain and DFT techniques.
- Compute DFT of real and complex discrete time signals.
- Computation of DFT using FFT algorithms and linear filtering approach.
- Solve problems on digital filter design and realize using digital computations.

**Question paper pattern:**

- The question paper will have ten questions
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Book:**

**Digital signal processing – Principles Algorithms & Applications**, Proakis & Monalakis, Pearson education, 4th Edition, New Delhi, 2007.

**Reference Books:**

1. Discrete Time Signal Processing, Oppenheim & Schaffer, PHI, 2003.
2. Digital Signal Processing, S. K. Mitra, Tata Mc-Graw Hill, 3rd Edition, 2010.
3. Digital Signal Processing, Lee Tan: Elsevier publications, 2007.

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## Verilog HDL

**B.E., V Semester, Electronics & Communication Engineering/ Telecommunication Engineering**

[As per Choice Based Credit System (CBCS) scheme]

| | | | |
|---|---|---|---|
| Subject Code | 15EC53 | IA Marks | 20 |
| Number of Lecture Hours/Week | 04 | Exam Marks | 80 |
| Total Number of Lecture Hours | 50 (10 Hours / Module) | Exam Hours | 03 |

CREDITS – 04

**Course objectives:** This course will enable students to:

- Differentiate between Verilog and VHDL descriptions.
- Learn different Verilog HDL and VHDL constructs.
- Familiarize the different levels of abstraction in Verilog.
- Understand Verilog Tasks and Directives.
- Understand timing and delay Simulation.
- Learn VHDL at design levels of data flow, behavioral and structural for effective modeling of digital circuits.

| Module-1 | RBT Level |
|---|---|
| **Overview of Digital Design with Verilog HDL**<br>Evolution of CAD, emergence of HDLs, typical HDL-flow, why Verilog HDL?, trends in HDLs. (Text1)<br>**Hierarchical Modeling Concepts**<br>Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block. (Text1) | L1, L2, L3 |
| **Module-2** | |
| **Basic Concepts**<br>Lexical conventions, data types, system tasks, compiler directives. (Text1)<br>**Modules and Ports**<br>Module definition, port declaration, connecting ports, hierarchical name referencing. (Text1) | L1, L2, L3 |
| **Module-3** | |
| **Gate-Level Modeling**<br>Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays. (Text1)<br>**Dataflow Modeling**<br>Continuous assignments, delay specification, expressions, operators, operands, operator types. (Text1) | L1, L2, L3 |
| **Module-4** | |
| **Behavioral Modeling**<br>Structured procedures, initial and always, blocking and non-blocking | L1, L2, L3 |

| | |
|---|---|
| statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks. (Text1) | |
| **Module-5** | |
| **Introduction to VHDL**<br>**Introduction:** Why use VHDL?, Shortcomings, Using VHDL for Design Synthesis, Design tool flow, Font conventions.<br>**Entities and Architectures:** Introduction, A simple design, Design entities, Identifiers, Data objects, Data types, and Attributes. (Text 2) | L1, L2, L3 |
| **Course Outcomes:** At the end of this course, students should be able to<br>• Write Verilog programs in gate, dataflow (RTL), behavioral and switch modeling levels of Abstraction.<br>• Write simple programs in VHDL in different styles.<br>• Design and verify the functionality of digital circuit/system using test benches.<br>• Identify the suitable Abstraction level for a particular digital design.<br>• Write the programs more effectively using Verilog tasks and directives.<br>• Perform timing and delay Simulation. | |
| **Question paper pattern:**<br>• The question paper will have ten questions<br>• Each full question consists of 16 marks.<br>• There will be 2 full questions (with a maximum of three sub questions) from each module.<br>• Each full question will have sub questions covering all the topics under a module<br>• The students will have to answer 5 full questions, selecting one full question from each module | |
| **Text Books:**<br>1. Samir Palnitkar, **"Verilog HDL: A Guide to Digital Design and Synthesis"**, Pearson Education, Second Edition.<br>2. Kevin Skahill, **"VHDL for Programmable Logic"**, PHI/Pearson education, 2006. | |
| **Reference Books:**<br>1. Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer Science+Business Media, LLC, Fifth edition.<br>2. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.<br>3. Padmanabhan, Tripura Sundari, "Design through Verilog HDL", Wiley, 2016 or earlier. | |

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# INFORMATION THEORY AND CODING

**B.E., V Semester, Electronics & Communication Engineering / Telecommunication Engineering**

[As per Choice Based Credit System (CBCS) scheme]

| | | | |
|---|---|---|---|
| Subject Code | 15EC54 | IA Marks | 20 |
| Number of Lecture Hours/Week | 04 | Exam Marks | 80 |
| Total Number of Lecture Hours | 50 (10 Hours / Module) | Exam Hours | 03 |
| CREDITS – 04 | | | |

**Course Objectives:** This course will enable students to:

- Understand the concept of Entropy, Rate of information and order of the source with reference to dependent and independent source.
- Study various source encoding algorithms.
- Model discrete & continuous communication channels.
- Study various error control coding algorithms.

**Modules**

| **Module-1** | **RBT Level** |
|---|---|
| **Information Theory:** Introduction, Measure of information, Information content of message, Average Information content of symbols in Long Independent sequences, Average Information content of symbols in Long dependent sequences, Markov Statistical Model of Information Sources, Entropy and Information rate of Markoff Sources (Section 4.1, 4.2 of Text 1). | L1, L2, L3 |
| **Module-2** | |
| **Source Coding**: Source coding theorem, Prefix Codes, Kraft McMillan Inequality property – KMI (Section 2.2 of Text 2).<br>Encoding of the Source Output, Shannon's Encoding Algorithm (Sections 4.3, 4.3.1 of Text 1).<br>Shannon Fano Encoding Algorithm, Huffman codes, Extended Huffman coding, Arithmetic Coding, Lempel – Ziv Algorithm (Sections 3.6, 3.7, 3.8, 3.10 of Text 3). | L1, L2, L3 |
| **Module-3** | |
| **Information Channels:** Communication Channels ( Section 4.4 of Text 1). Channel Models, Channel Matrix, Joint probabilty Matrix, Binary Symmetric Channel, System Entropies, Mutual Information, Channel Capacity, Channel Capacity of : Binary Symmetric Channel, Binary Erasure Channel, Muroga,s Theorem, Contineuos Channels (Sections 4.2, 4.3, 4.4, 4.6, 4.7 of Text 3). | L1, L2, L3 |
| **Module-4** | |

| | |
|---|---|
| **Error Control Coding**:<br>Introduction, Examples of Error control coding, methods of Controlling Errors, Types of Errors, types of Codes, Linear Block Codes: matrix description of Linear Block Codes, Error Detection and Error Correction Capabilities of Linear Block Codes, Single Error Correcting hamming Codes, Table lookup Decoding using Standard Array.<br>**Binary Cyclic Codes:** Algebraic Structure of Cyclic Codes, Encoding using an (n-k) Bit Shift register, Syndrome Calculation, Error Detection and Correction<br>(Sections 9.1, 9.2, 9.3, 9.3.1, 9.3.2, 9.3.3 of Text 1). | L1, L2, L3 |
| **Module-5** | |
| **Some Important Cyclic Codes:** Golay Codes, BCH Codes( Section 8.4 – Article 5 of Text 2).<br>**Convolution Codes**: Convolution Encoder, Time domain approach, Transform domain approach, Code Tree, Trellis and State Diagram, The Viterbi Algorithm) (Section 8.5 – Articles 1,2 and 3, 8.6- Article 1 of Text 2). | L1, L2, L3 |

**Course Outcomes:** At the end of the course the students will be able to:

- Explain concept of Dependent & Independent Source, measure of information, Entropy, Rate of Information and Order of a source
- Represent the information using Shannon Encoding, Shannon Fano, Prefix and Huffman Encoding Algorithms
- Model the continuous and discrete communication channels using input, output and joint probabilities
- Determine a codeword comprising of the check bits computed using Linear Block codes, cyclic codes & convolutional codes
- Design the encoding and decoding circuits for Linear Block codes, cyclic codes, convolutional codes, BCH and Golay codes.

**Question paper pattern:**

- The question paper will have ten questions
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

**Text Books:**


1. Digital and analog communication systems, K. Sam Shanmugam, John Wiley India Pvt. Ltd, 1996.
2. Digital communication, Simon Haykin, John Wiley India Pvt. Ltd, 2008.
3. Information Theory and Coding, Muralidhar Kulkarni, K.S. Shivaprakasha, Wiley India Pvt. Ltd, 2015, ISBN:978-81-265-5305-1.


**Reference Books:**


1. ITC and Cryptography, Ranjan Bose, TMH, II edition, 2007
2. Principles of digital communication, J. Das, S. K. Mullick, P. K. Chatterjee, Wiley, 1986 - Technology & Engineering

3. Digital Communications – Fundamentals and Applications, Bernard Sklar, Second Edition, Pearson Education, 2016, ISBN: 9780134724058.
4. Information Theory and Coding, K.N.Haribhat, D.Ganesh Rao, Cengage Learning, 2017.

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## NANOELECTRONICS

**B.E., V Semester, Electronics & Communication Engineering / Telecommunication Engineering**

[As per Choice Based Credit System (CBCS) scheme]

| | | | |
|---|---|---|---|
| Subject Code | 15EC551 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam Marks | 80 |
| Total Number of Lecture Hours | 40 (8 Hours / Module) | Exam Hours | 03 |

CREDITS – 03

**Course Objectives:** This course will enable students to:

- Enhance basic engineering science and technical knowledge of nanoelectronics.
- Explain basics of top-down and bottom-up fabrication process, devices and systems.
- Describe technologies involved in modern day electronic devices.
- Know various nanostructures of carbon and the nature of the carbon bond itself.
- Learn the photo physical properties of sensor used in generating a signal.

| Module-1 | RBT Level |
|---|---|
| **Introduction:** Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moore's law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometerlength scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems (Text 1). | L1, L2 |
| **Module-2** | |
| **Characterization:** Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques (Text 1).<br>**Inorganic semiconductor nanostructures:** overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states (Text 1). | L1, L2 |
| **Module-3** | |
| **Fabrication techniques:** requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques.(Text 1).<br>**Physical processes:** modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical | L1, L2 |

| | |
|---|---|
| electrical and structural (Text 1). | |
| **Module-4** | |
| **Carbon Nanostructures:** Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes. (Text 2) | L1, L2 |
| **Module-5** | |
| **Nanosensors:** Introduction, What is Sensor and Nanosensors?, What makes them Possible?, Order From Chaos, Characterization, Perception, Nanosensors Based On Quantum Size Effects, Electrochemical Sensors, Sensors Based On Physical Properties, Nanobiosensors, Smart dust Sensor for the future. (Text 3)<br>**Applications:** Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS (Text 1). | L1, L2 |
| **Course outcomes:** After studying this course, students will be able to:<br>• Know the principles behind Nanoscience engineering and Nanoelectronics.<br>• Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.<br>• Know the properties of carbon and carbon nanotubes and its applications.<br>• Know the properties used for sensing and the use of smart dust sensors.<br>• Apply the knowledge to prepare and characterize nanomaterials.<br>• Analyse the process flow required to fabricate state-of-the-art transistor technology. | |
| **Question paper pattern:**<br>• The question paper will have ten questions<br>• Each full question consists of 16 marks.<br>• There will be 2 full questions (with a maximum of three sub questions) from each module.<br>• Each full question will have sub questions covering all the topics under a module<br>• The students will have to answer 5 full questions, selecting one full question from each module | |
| **Text Books:**<br>1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, "Nanoscale Science and Technology", John Wiley, 2007.<br>2. Charles P Poole, Jr, Frank J Owens, "Introduction to Nanotechnology", John Wiley, Copyright 2006, Reprint 2011.<br>3. T Pradeep, "Nano: The essentials-Understanding Nanoscience and Nanotechnology", TMH. | |
| **Reference Book:**<br>Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, "Hand Book of Nanoscience Engineering and Technology", CRC press, 2003. | |



D.V.P

## SWITCHING & FINITE AUTOMATA THEORY

**B.E., V Semester, Electronics & Communication Engineering / Telecommunication Engineering**

[As per Choice Based Credit System (CBCS) scheme]

| | | | |
|---|---|---|---|
| Subject Code | 15EC552 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam Marks | 80 |
| Total Number of Lecture Hours | 40 (8 Hours / Module) | Exam Hours | 03 |
| CREDITS – 03 | | | |

**Course Objectives:** This course will enable students to:

1. Understand the basics of threshold logic, effect of hazards on digital circuits and techniques of fault detection
2. Explain finite state model and minimization techniques
3. Know structure of sequential machines, and state identification
4. Understand the concept of fault detection experiments

**Modules**

| **Module-1** | **RBT Level** |
|---|---|
| **Threshold Logic:** Introductory Concepts: Threshold element, capabilities and limitations of threshold logic, Elementary Properties, Synthesis of Threshold networks: Unate functions, Identification and realization of threshold functions, The map as a tool in synthesizing threshold networks. (Sections 7.1, 7.2 of Text) | L1, L2, L3 |
| **Module-2** | |
| **Reliable Design and Fault Diagnosis:** Hazards, static hazards, Design of Hazard-free Switching Circuits, Fault detection in combinational circuits, Fault detection in combinational circuits: The faults, The Fault Table, Covering the fault table, Fault location experiments: Preset experiments, Adaptive experiments, Boolean differences, Fault detection by path sensitizing. (Sections 8.1, 8.2, 8.3, 8.4, 8.5 of Text) | L1, L2, L3 |
| **Module-3** | |
| **Sequential Machines: Capabilities, Minimization and Transformation** The Finite state model and definitions, capabilities and limitations of finite state machines, State equivalence and machine minimization: k-equivalence, The minimization Procedure, Machine equivalence, Simplification of incompletely specified machines. (Section 10.1, 10.2, 10.3, 10.4 of Text) | L1, L2, L3 |
| **Module-4** | |
| **Structure of Sequential Machines:** Introductory example, State assignment using partitions: closed partitions, The lattice of closed partitions, Reduction of output dependency, Input dependence and autonomous clocks, Covers and generation of closed partitions by state splitting: Covers, The implication graph, An application of state splitting to parallel decomposition. (Section 12.1, 12.2, 12.3, 12.4, 12.5, 12.6 of Text) | L1, L2, L3 |
| **Module-5** | |
| **State-Identification and Fault Detection Experiments:** Experiments, Homing experiments, Distinguishing experiments, Machine identification, | L1, L2, L3 |

| | |
|---|---|
| Fault detection experiments, Design of diagnosable machines, Second algorithm for the design of fault detection experiments. (Sections 13.1, 13.2, 13.3, 13.4, 13.5, 13.6, 13.7 of Text) | |

**Course outcomes:** At the end of the course, students should be able to:

- Explain the concept of threshold logic
- Understand the effect of hazards on digital circuits and fault detection and analysis
- Define the concepts of finite state model
- Analyze the structure of sequential machine
- Explain methods of state identification and fault detection experiments

**Question paper pattern:**

- The question paper will have ten questions
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

**Text Book:**

**Switching and Finite Automata Theory** – Zvi Kohavi, McGraw Hill, 2nd edition, 2010 ISBN: 0070993874.

**Reference Books:**

1. **Fault Tolerant And Fault Testable Hardware Design**-Parag K Lala, Prentice Hall Inc. 1985.
2. **Digital Circuits and Logic Design**.-Charles Roth Jr, Larry L. Kinney, Cengage Learning, 2014, ISBN: 978-1-133-62847-7.

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## OPERATING SYSTEM

**B.E., V Semester, Electronics & Communication Engineering / Telecommunication Engineering**

[As per Choice Based Credit System (CBCS) scheme]

| | | | |
|---|---|---|---|
| Subject Code | 15EC553 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam Marks | 80 |
| Total Number of Lecture Hours | 40 (8 Hours / Module) | Exam Hours | 03 |
| CREDITS – 03 | | | |

**Course objectives:** This course will enable students to:

- Understand the services provided by an operating system.
- Understand how processes are synchronized and scheduled.
- Understand different approaches of memory management and virtual memory management.
- Understand the structure and organization of the file system
- Understand interprocess communication and deadlock situations.

| Module-1 | RBT Level |
|---|---|
| **Introduction to Operating Systems** OS, Goals of an OS, Operation of an OS, Computational Structures, Resource allocation techniques, Efficiency, System Performance and User Convenience, Classes operating System, Batch processing, Multi programming, Time Sharing Systems, Real Time and distributed Operating Systems (Topics from Sections 1.2, 1.3, 2.2 to 2.8 of Text). | L1, L2 |
| **Module-2** | |
| **Process Management:** OS View of Processes, PCB, Fundamental State Transitions, Threads, Kernel and User level Threads, Non-preemptive scheduling- FCFS and SRN, Preemptive Scheduling- RR and LCN, Long term, medium term and short term scheduling in a time sharing system (Topics from Sections 3.3, 3.3.1 to 3.3.4, 3.4, 3.4.1, 3.4.2 , 4.2, 4.3, 4.4.1 of Text). | L1, L2 |
| **Module-3** | |
| **Memory Management:** Contiguous Memory allocation, Non-Contiguos Memory Allocation, Paging, Segmentation, Segmentation with paging, Virtual Memory Management, Demand Paging, Paging Hardware, VM handler, FIFO, LRU page replacement policies (Topics from Sections 5.5 to 5.9, 6.1 to 6.3, except Optimal policy and 6.3.1of Text). | L1, L2 |
| **Module-4** | |
| **File Systems:** File systems and IOCS, File Operations, File Organizations, Directory structures, File Protection, Interface between File system and IOCS, Allocation of disk space, Implementing file access (Topics from Sections 7.1 to 7.8 of Text). | L1, L2, L3 |
| **Module-5** | |
| **Message Passing and Deadlocks**: Overview of Message Passing, Implementing message passing, Mailboxes, Deadlocks, Deadlocks in resource allocation, Resource state modelling, Deadlock detection algorithm, Deadlock Prevention (Topics from Sections 10.1 to 10.3, 11.1 to | L1, L2, L3 |

| 11.5 of Text). | |
|---|---|

**Course outcomes:** After studying this course, students will be able to:

- Explain the goals, structure, operation and types of operating systems.
- Apply scheduling techniques to find performance factors.
- Explain organization of file systems and IOCS.
- Apply suitable techniques for contiguous and non-contiguous memory allocation.
- Describe message passing, deadlock detection and prevention methods.

**Question paper pattern:**

- The question paper will have ten questions
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

**Text Book:**

Operating Systems – A concept based approach, by Dhamdare, TMH, 2nd edition.

**Reference Books:**


1. Operating systems concepts, Silberschatz and Galvin, John Wiley India Pvt. Ltd, 5th edition,2001.
2. Operating system–internals and design system, William Stalling, Pearson Education, 4th ed, 2006.
3. Design of operating systems, Tannanbhaum, TMH, 2001.


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## ELECTRICAL ENGINEERING MATERIALS

**B.E., V Semester, Electronics & Communication Engineering/ Telecommunication Engineering**

[As per Choice Based Credit System (CBCS) scheme]

| | | | |
|---|---|---|---|
| Subject Code | 15EC554 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam Marks | 80 |
| Total Number of Lecture Hours | 40 (8 Hours/Module) | Exam Hours | 03 |
| CREDITS – 03 | | | |

**Course Objectives:** This course will enable students to:

- Understand the formation of bands in materials and the classification of materials on the basis of band theory
- Understand the classification of magnetic materials on the basis of their behavior in an external magnetizing field.
- Understand the characteristics and properties of conducting and superconducting materials
- Understand the electrical characteristics of the material to be considered on the basis of their uses.
- Classify electrical engineering materials into low and high resistance materials

**Modules**

| **Module-1** | **RBT Level** |
|---|---|
| **Band Theory of Solids:** Introduction to free electron theory, Kroning-Penney Model, Explanation for Discontinuities in E vs. K curve, Formation of Solid Material, Formation of Band in Metals, Formation of Bands in Semiconductors and Insulating Materials, Classification of Materials on the Basis of Band Structure, Explanation for differences in the Electrical properties of different Materials. Important Characteristics of a Band Electron, Number of energy states per band, Explanation for Insulating and Metallic Behavior of Materials, Concept of Hole. | L1, L2 |
| **Module-2** | |
| **Magnetic Properties of Materials:** Introduction, Origin of Magnetism, Basic Terms in Magnetism, Relation between Magnetic Permeability and Susceptibility, Classification of magnetic Materials, Characteristics of Diamagnetic Materials, Paramagnetic Materials, Ferromagnetic Materials, Ferrimagnetic Materials, Langevin's Theory of Diamagnetism, Explanation of Dia, Para and Ferromagnetism, Ampere's Lam in Dia, Para and Ferromagnetism, Hystersis and Hystersis loss, Langevin's Theory of paramagnetism, Modification in the Langevin's Theory, Anti-Ferromagnetism and Neel Temperature, Ferrimagnetic Materials, Properties of some important Magnetic Materials, Magentostriction and Magnetostrictive Materials, Hard and Soft Ferromagnetic Materials and their Applications. | L1, L2 |
| **Module-3** | |
| **Behavior of Dielectric Materials in AC and DC Fields:** Introduction, Classification of Dielectric Materials at Microscopic level, Polar Dielectric Materials, Non-polar Dielectric Materials, Kinds of Polarizations, behavior of | L1, L2 |

| | |
|---|---|
| dielectric materials, Three electric Vectors, Gauss's Law in a Dielectric, Electric Susceptibility and Static Dielectric constant, Effect of Dielectric medium upon capacitance, macroscopic electric field, Microscopic Electric field, temperature dependence of dielectric constant, polar dielectric in ac and dc fields, behavior of polar dielectric at high frequencies, Dielectric loss, Dielectric strength and Dielectric Breakdown, Various kinds of Dielectric Materials, Hysteresis in Ferroelectric Materials, Applications of Ferroelectric Materials in Devices. | |
| **Module-4** | |
| **Conductivity of Metals and Superconductivity:** Introduction, Ohm's law, Explanation for the dependence of electrical resistivity upon temperature, Free-electron theory of metals, Application of Lorentz-Drude free-electron theory, Effect of various parameters on Electrical Conductivity, Resistivity Ratio, Variation of resistivity of alloys with temperature, Thermal Conductivity of Materials, Heat produced in Current Carrying Conductor, Thermoelectric Effect, Thermoelectric Series, Seebeck's Experiment.<br><br>Discovery of superconductivity, superconductivity and transition temperature, superconducting materials, explanation of superconductivity phenomenon, characteristics of superconductors, change in thermodynamic parameters in superconducting state, frequency dependence of superconductivity, current status of high temperature superconductors, practical applications of superconductors. | L1, L2 |
| **Module-5** | |
| **Electrical Conducting and Insulating materials:** Introduction, Classification of conducting materials, difference in properties of Hard-Drawn and Annealed copper, standard conductors, comparison between some popular Low-Resistivity Materials, Low-Resistivity Copper Alloys, Electrical contact materials and their selection, classification of contact materials, Materials for Lamp Filaments, Preparation of Tungsten Filaments.<br><br>Insulating gases, Liquids and solids and their characteristics, Selection of the insulating material, other important properties of Insulating materials, Thermal characteristics, chemical properties of Insulating materials, classification of Insulating materials on the basis of structure. | L1, L2 |
| **Course Outcomes:** At the end of the course, students will be able to<br>• Understand the various kinds of materials and their applications in ac and dc fields.<br>• Understand the conductivity of superconductivity of materials.<br>• Explain the electrical properties of different materials and metallic behavior of materials on the basis of band theory.<br>• Explain the properties and applications of all kind of magnetic materials.<br>• Explain the properties of electrical conducting and insulating materials.<br>• Assess a variety of approaches in developing new materials with enhanced performance to replace existing materials. | |
| **Question paper pattern:**<br>• The question paper will have ten questions | |

- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

**Text Book:**

R K Shukla and Archana Singh, "Electrical Engineering Materials" McGraw Hill, 2012, ISBN: 978-1-25-90062-03.

**Reference Books:**


1. S.O. KASAP, "Electronic Materials and Devices" 3rd edition, McGraw Hill, 2014, ISBN-978-0-07-064820-3.
2. C.S.Indulkar and S. Thiruvengadam, S., "An Introduction to Electrical Engineering Materials", ISBN-9788121906661.


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## MSP430 MICROCONTROLLER

**B.E., V Semester, Electronics & Communication Engineering**

[As per Choice Based Credit System (CBCS) scheme]

| | | | |
|---|---|---|---|
| Subject Code | 15EC555 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam Marks | 80 |
| Total Number of Lecture Hours | 40 (8 Hours / Module) | Exam Hours | 03 |

CREDITS – 03

**Course objectives:** This course will enable students to:

- Understand the architectural features and instruction set of 16 bit microcontroller MSP430.
- Program MSP430 using the various instructions for different applications.
- Understand the functions of the various peripherals which are interfaced with MSP430.
- Describe the power saving modes in MSP430.
- Explain the low power applications using MSP430.

| Module-1 | RBT Level |
|---|---|
| **MSP430 Architecture:** Introduction –Where does the MSP430 fit, The outside view, The inside view-Functional block diagram, Memory, Central Processing Unit, Memory Mapped Input and Output, Clock Generator, Exceptions: Interrupts and Resets, MSP430 family.<br>(Text: Ch1- 1.3 to 1.7, Ch2- 2.1 to 2.7, Ch5- 5.1, 5.7 up to 5.7.1) | L1, L2 |
| **Module-2** | |
| **Addressing Modes & Instruction Set-**Addressing Modes, Instruction set, Constant Generator and Emulated Instructions, Program Examples.<br>(Text: Ch5- 5.2 to 5.5) | L1, L2, L3 |
| **Module-3** | |
| **Clock System, Interrupts and Operating Modes-**Clock System, Interrupts, What happens when an interrupted is requested, Interrupt Service Routines, Low Power Modes of Operation, Watchdog Timer, Basic Timer1, Real Time Clock, Timer-A: Timer Block, Capture/Compare Channels, Interrupts from Timer-A.<br>(Text: Ch5 - 5.8 upto 5.8.4, Ch 6-6.6 to 6.8, 6.10, Ch8 -8.1, 8.2, 8.3) | L1, L2 |
| **Module-4** | |
| **Analog Input-Output and PWM** - Comparator-A, ADC10, ADC12, Sigma-Delta ADC, Internal Operational Amplifiers, DAC, Edge Aligned PWM, Simple PWM, Design of PWM.<br>LCD interfacing.<br>(Text: Ch9 – 9.1 up to 9.1.2, 9.4, 9.5 up to 9.5.1, 9.7, 9.8 up to 9.8.1, 9.11.5, 9.12 (without 9.12.1), 8.6.2 to 8.6.4) | L1, L2 |
| **Module-5** | |

| | |
|---|---|
| **Digital Input-Output and Serial Communication:**<br>Parallel Ports, Lighting LEDs, Flashing LEDs, Read Input from a Switch, Toggle the LED state by pressing the push button, LCD interfacing. Asynchronous Serial Communication, Asynchronous Communication with USCI_A, Communications, Peripherals in MSP430, Serial Peripheral Interface.<br>(Text: Selected topics from Ch4 & Ch7 and Ch7- 7.1, Ch10 – 10.1, 10.2, and 10.12) | L1, L2, L3 |
| **Course outcomes:** After studying this course, students will be able to:<br>• Understand the architectural features and instruction set of 16 bit microcontroller MSP430.<br>• Develop programs using the various instructions of MSP430 for different applications.<br>• Understand the functions of the various peripherals which are interfaced with MSP430 microcontroller.<br>• Describe the power saving modes in MSP430.<br>• Explain the low power applications using MSP430 microcontroller. | |
| **Evaluation of Internal Assessment Marks:**<br>It is suggested that at least a few simple programs to be executed by students using any evaluation board of MSP430 for better understanding of the course. This activity can be considered for the evaluation of 5 marks out of 20 Internal assessment marks, reserved for the other activities. | |
| **Question paper pattern:**<br>• The question paper will have ten questions<br>• Each full question consists of 16 marks.<br>• There will be 2 full questions (with a maximum of three sub questions) from each module.<br>• Each full question will have sub questions covering all the topics under a module<br>• The students will have to answer 5 full questions, selecting one full question from each module | |
| **Text Book:**<br>John H Davies, MSP430 Microcontroller Basics, Newnes Publications, Elsevier, 2008. | |
| **References:**<br>1. Chris Nagy, Embedded Systems Design using TI MSP430 Series, Newnes Publications, Elsevier, 2003.<br>2. User Guide from Texas Instruments. | |

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## DSP Lab

**B.E., V Semester, EC/TC**

[As per Choice Based Credit System (CBCS) scheme]

| Subject Code | 15ECL57 | IA Marks | 20 |
|---|---|---|---|
| Number of Lecture Hours/Week | 01Hr Tutorial (Instructions) + 02 Hours Laboratory=03 | Exam Marks | 80 |
| RBT Levels | L1, L2, L3 | Exam Hours | 03 |

**CREDITS – 02**

**Course objectives:** This course will enable students to

- Simulate discrete time signals and verification of sampling theorem.
- Compute the DFT for a discrete signal and verification of its properties using MATLAB.
- Find solution to the difference equations and computation of convolution and correlation along with the verification of properties.
- Compute and display the filtering operations and compare with the theoretical values.
- Implement the DSP computations on DSP hardware and verify the result.

**Laboratory Experiments**

**Following Experiments to be done using MATLAB / SCILAB / OCTAVE or equivalent:**

1. Verification of sampling theorem.
2. Linear and circular convolution of two given sequences, Commutative, distributive and associative property of convolution.
3. Auto and cross correlation of two sequences and verification of their properties
4. Solving a given difference equation.
5. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum (using DFT equation and verify it by built-in routine).
6. (i) Verification of DFT properties (like Linearity and Parseval's theorem, etc.) (ii) DFT computation of square pulse and Sinc function etc.
7. Design and implementation of FIR filter to meet given specifications (using different window techniques).
8. Design and implementation of IIR filter to meet given specifications.

**Following Experiments to be done using DSP kit**

9. Linear convolution of two sequences
10. Circular convolution of two sequences
11. N-point DFT of a given sequence
12. Impulse response of first order and second order system
13. Implementation of FIR filter

**Course outcomes:** On the completion of this laboratory course, the students will be able to:

- Understand the concepts of analog to digital conversion of signals and frequency domain sampling of signals.

- Modelling of discrete time signals and systems and verification of its properties and results.
- Implementation of discrete computations using DSP processor and verify the results.
- Realize the digital filters using a simulation tool and a DSP processor and verify the frequency and phase response.

**Conduct of Practical Examination:**

1. All laboratory experiments are to be included for practical examination.
2. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
3. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

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## HDL Lab

**B.E., V Semester, EC/TC**

[As per Choice Based Credit System (CBCS) scheme]

| | | | |
|---|---|---|---|
| Subject Code | 15ECL58 | IA Marks | 20 |
| Number of Lecture Hours/Week | 01 Hr Tutorial (Instructions) + 02 Hours Laboratory = 03 | Exam Marks | 80 |
| RBT Levels | L1, L2, L3 | Exam Hours | 03 |

**CREDITS – 02**

**Course objectives:** This course will enable students to:

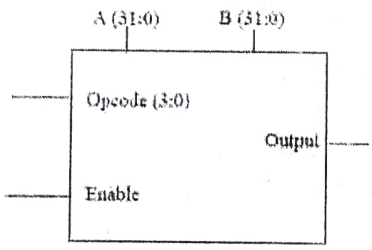
- Familiarize with the CAD tool to write HDL programs.
- Understand simulation and synthesis of digital design.
- Program FPGAs/CPLDs to synthesise the digital designs.
- Interface hardware to programmable ICs through I/O ports.
- Choose either Verilog or VHDL for a given Abstraction level.

**Note:** Programming can be done using any compiler. Download the programs on a FPGA/CPLD boards such as Apex/Acex/Max/Spartan/Sinfi or equivalent and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

**Laboratory Experiments**

**Part–A: PROGRAMMING**

1. Write Verilog code to realize all the logic gates
2. Write a Verilog program for the following combinational designs
   a. 2 to 4 decoder
   b. 8 to 3 (encoder without priority & with priority)
   c. 8 to 1 multiplexer.
   d. 4 bit binary to gray converter
   e. Multiplexer, de-multiplexer, comparator.
3. Write a VHDL and Verilog code to describe the functions of a Full Adder using three modeling styles.
4. Write a Verilog code to model 32 bit ALU using the schematic diagram shown below




- ALU should use combinational logic to calculate an output based on the four bit op-code input.
- ALU should pass the result to the out bus when enable line in high, and tri-state the out bus when the enable line is low.

- ALU should decode the 4 bit op-code according to the example given below.

| OPCODE | ALU Operation |
|---|---|
| 1. | A+B |
| 2. | A-B |
| 3. | A Complement |
| 4. | A*B |
| 5. | A AND B |
| 6. | A OR B |
| 7. | A NAND B |
| 8. | A XOR B |

5. Develop the Verilog code for the following flip-flops, SR, D, JK and T.
6. Design a 4 bit binary, BCD counters (Synchronous reset and Asynchronous reset) and "any sequence" counters, using Verilog code.

**Part–B: INTERFACING (at least four of the following must be covered using VHDL/Verilog)**

1. Write HDL code to display messages on an alpha numeric LCD display.
2. Write HDL code to interface Hex key pad and display the key code on seven segment display.
3. Write HDL code to control speed, direction of DC and Stepper motor.
4. Write HDL code to accept Analog signal, Temperature sensor and display the data on LCD or Seven segment display.
5. Write HDL code to generate different waveforms (Sine, Square, Triangle, Ramp etc.,) using DAC - change the frequency.
6. Write HDL code to simulate Elevator operation.

**Course Outcomes:** At the end of this course, students should be able to:

- Write the Verilog/VHDL programs to simulate Combinational circuits in Dataflow, Behavioral and Gate level Abstractions.
- Describe sequential circuits like flip flops and counters in Behavioral description and obtain simulation waveforms.
- Synthesize Combinational and Sequential circuits on programmable ICs and test the hardware.
- Interface the hardware to the programmable chips and obtain the required output.

**Conduct of Practical Examination:**

1. All laboratory experiments are to be included for practical examination.
2. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
3. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.



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## 5th Semester Open Electives Syllabus for the Courses offered by EC/TC Board

**Automotive Electronics**
**B.E V Semester (Open Elective)**
[As per Choice Based Credit System (CBCS) scheme

| | | | |
|---|---|---|---|
| Subject Code | 15EC561 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam Marks | 80 |
| Total Number of Lecture Hours | 40(08 Hrs per Module) | Exam Hours | 03 |

CREDITS – 03

**Course objectives:** This course will enable students to:

- Understand the basics of automobile dynamics and design electronics to complement those features.
- Design and implement the electronics that attribute the reliability, safety, and smartness to the automobiles, providing add-on comforts.

| Module-1 | RBT Level |
|---|---|
| **Automotive Fundamentals Overview** – Evolution of Automotive Electronics, Automobile Physical Configuration, Survey of Major Automotive Systems, The Engine – Engine Block, Cylinder Head, Four Stroke Cycle, Engine Control, Ignition System - Spark plug, High voltage circuit and distribution, Spark pulse generation, Ignition Timing, Diesel Engine, Drive Train - Transmission, Drive Shaft, Differential, Suspension, Brakes, Steering System (Text 1: Chapter1), Starter Battery –Operating principle: (Text 2: Pg. 407-410) (4 hours)<br><br>**The Basics of Electronic Engine Control** – Motivation for Electronic Engine Control – Exhaust Emissions, Fuel Economy, Concept of an Electronic Engine control system, Definition of General terms, Definition of Engine performance terms, Engine mapping, Effect of Air/Fuel ratio, spark timing and EGR on performance, Control Strategy, Electronic Fuel control system, Analysis of intake manifold pressure, Electronic Ignition. (Text 1: Chapter 5) (4 hours) | L1, L2 |
| **Module-2** | |

| | |
|---|---|
| Automotive Control System applications of Sensors and Actuators – Typical Electronic Engine Control System, Variables to be measured (Text 1: Chapter 6) (1 hour)<br>**Automotive Sensors** – Airflow rate sensor, Strain Gauge MAP sensor, Engine Crankshaft Angular Position Sensor, Magnetic Reluctance Position Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Throttle Angle Sensor (TAS), Engine Coolant Temperature (ECT) Sensor, Exhaust Gas Oxygen (O2/EGO) Lambda Sensors, Piezoelectric Knock Sensor. (Text 1: Chapter 6) (5 hours)<br>**Automotive Actuators** – Solenoid, Fuel Injector, EGR Actuator, Ignition System (Text 1: Chapter 6) (2 hours) | L1, L2 |
| **Module-3** | |
| **Digital Engine Control Systems** – Digital Engine control features, Control modes for fuel Control (Seven Modes), EGR Control, Electronic Ignition Control - Closed loop Ignition timing, Spark Advance Correction Scheme, Integrated Engine Control System - Secondary Air Management, Evaporative Emissions Canister Purge, Automatic System Adjustment, System Diagnostics. (Text 1: Chapter 7) (6 hours)<br><br>**Control Units** – Operating conditions, Design, Data processing, Programming, Digital modules in the Control unit, Control unit software. (Text 2: Pg. 196-207) (2 hours) | L1, L2 |
| **Module-4** | |
| **Automotive Networking** –Bus Systems – Classification, Applications in the vehicle, Coupling of networks, Examples of networked vehicles (Text 2: Pg. 85-91), Buses - CAN Bus, LIN Bus, MOST Bus, Bluetooth, Flex Ray, Diagnostic Interfaces. (Text 2: Pg. 92-151) (6 hours)<br><br>**Vehicle Motion Control** – Typical Cruise Control System, Digital Cruise Control System, Digital Speed Sensor, Throttle Actuator, Digital Cruise Control configuration, Cruise Control Electronics (Digital only), Antilock Brake System (ABS) (Text 1: Chapter 8) (2 hours) | L1, L2 |
| **Module-5** | |
| **Automotive Diagnostics**–Timing Light, Engine Analyzer, On-board diagnostics, Off-board diagnostics, Expert Systems, Occupant Protection Systems – Accelerometer based Air Bag systems. (Text 1: Chapter 10) (2 hours)<br><br>**Future Automotive Electronic Systems** – Alternative Fuel Engines, Electric and Hybrid vehicles, Fuel cell powered cars, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Heads Up display, Speech Synthesis, Navigation – Navigation Sensors - Radio Navigation, Signpost navigation, dead reckoning navigation, Voice Recognition Cell Phone dialing, Advanced Cruise Control, Stability Augmentation, Automatic driving Control (Text 1: Chapter 11) (6 hours) | L1, L2, L3 |

**Course Outcomes:** At the end of the course, students will be able to:

- Acquire an overview of automotive components, subsystems, and basics of Electronic Engine Control in today's automotive industry.
- Use available automotive sensors and actuators while interfacing with microcontrollers / microprocessors during automotive system design.
- Understand the networking of various modules in automotive systems, communication protocols and diagnostics of the sub systems.
- Design and implement the electronics that attribute the reliability, safety, and smartness to the automobiles, providing add-on comforts and get fair idea on future Automotive Electronic Systems.

**Question paper pattern:**

- The question paper will have ten questions.
- Each full Question consisting of 16 marks
- There will be 2 full questions (with a maximum of three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Books:**


1. William B. Ribbens, "Understanding Automotive Electronics", 6th Edition, Elsevier Publishing.
2. Robert Bosch Gmbh (Ed.) Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive, 5th edition, John Wiley& Sons Inc., 2007.


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# Object Oriented Programming Using C++

**B.E. V Semester (Open Elective)**

[As per Choice Based Credit System (CBCS)scheme]

| | | | |
|---|---|---|---|
| Subject Code | 15EC562 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam Marks | 80 |
| Total Number of Lecture Hours | 40 (08 Hrs/ Module | Exam Hours | 03 |

CREDITS – 03

**Course objectives:** This course will enable students to:

- Define Encapsulation, Inheritance and Polymorphism.
- Solve the problem with object oriented approach.
- Analyze the problem statement and build object oriented system model.
- Describe the characters and behavior of the objects that comprise a system.
- Explain function overloading, operator overloading and virtual functions.
- Discuss the advantages of object oriented programming over procedure oriented programming.

| **Module -1** | **RBT Level** |
|---|---|
| **Beginning with C++ and its features:** What is C++?, Applications and structure of C++ program, Different Data types, Variables, Different Operators, expressions, operator overloading and control structures in C++ (Topics from Ch -2,3 of Text). | L1, L2 |
| **Module -2** | |
| **Functions, classes and Objects:** Functions, Inline function, function overloading, friend and virtual functions, Specifying a class, C++ program with a class, arrays within a class, memory allocation to objects, array of objects, members, pointers to members and member functions (Selected Topics from Chap-4,5 of Text). | L1, L2, L3 |
| **Module -3** | |
| **Constructors, Destructors and Operator overloading:** Constructors, Multiple constructors in a class, Copy constructor, Dynamic constructor, Destructors, Defining operator overloading, Overloading Unary and binary operators, Manipulation of strings using operators (Selected topics from Chap-6, 7 of Text). | L1, L2, L3 |
| **Module -4** | |
| **Inheritance, Pointers, Virtual Functions, Polymorphism:** Derived Classes, Single, multilevel, multiple inheritance, Pointers to objects and derived classes, this pointer, Virtual and pure virtual functions (Selected topics from Chap-8,9 of Text). | L1, L2, L3 |

| Module -5 | |
|---|---|
| **Streams and Working with files:** C++ streams and stream classes, formatted and unformatted I/O operations, Output with manipulators, Classes for file stream operations, opening and closing a file, EOF (Selected topics from Chap-10, 11 of Text). | L1, L2, L3 |

**Course Outcomes:** At the end of the course, students will be able to:

- Explain the basics of Object Oriented Programming concepts.
- Apply the object initialization and destroy concept using constructors and destructors.
- Apply the concept of polymorphism to implement compile time polymorphism in programs by using overloading methods and operators.
- Use the concept of inheritance to reduce the length of code and evaluate the usefulness.
- Apply the concept of run time polymorphism by using virtual functions, overriding functions and abstract class in programs.
- Use I/O operations and file streams in programs.

**Question paper pattern:**

- The question paper will have ten questions.
- Each full Question consisting of 16 marks
- There will be 2 full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Book:**

Object Oriented Programming with C++, E.Balaguruswamy, TMH, 6th Edition, 2013.

**Reference Book:**

Object Oriented Programming using C++, Robert Lafore, Galgotia publication 2010.

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# 8051 MICROCONTROLLER

**B.E., V Semester (Open Elective)**

[As per Choice Based Credit System (CBCS) scheme]

| | | | |
|---|---|---|---|
| Subject Code | 15EC563 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam Marks | 80 |
| Total Number of Lecture Hours | 40 (08 Hrs/ Module) | Exam Hours | 03 |

CREDITS – 03

**Course objectives:** This course will enable students to:

- Understand the difference between a Microprocessor and a Microcontroller and embedded microcontrollers.
- Familiarize the basic architecture of 8051 microcontroller.
- Program 8051microprocessor using Assembly Level Language and C.
- Understand the interrupt system of 8051 and the use of interrupts.
- Understand the operation and use of inbuilt Timers/Counters and Serial port of 8051.
- Interface 8051 to external memory and I/O devices using its I/O ports.

| **Module -1** | **RBT Level** |
|---|---|
| **8051 Microcontroller:** Microprocessor Vs Microcontroller, Embedded Systems, Embedded Microcontrollers, 8051 Architecture- Registers, Pin diagram, I/O ports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing. | L1, L2 |
| **Module -2** | |
| **8051 Instruction Set:** Addressing Modes, Data Transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Bit manipulation instructions. Simple Assembly language program examples (without loops) to use these instructions. | L1, L2 |
| **Module -3** | |
| **8051 Stack, I/O Port Interfacing and Programming:** 8051 Stack, Stack and Subroutine instructions. Assembly language program examples on subroutine and involving loops - Delay subroutine, Factorial of an 8 bit number (result maximum 8 bit), Block move without overlap, Addition of N 8 bit numbers, Picking smallest/largest of N 8 bit numbers.<br>Interfacing simple switch and LED to I/O ports to switch on/off LED with respect to switch status. | L1, L2, L3 |
| **Module -4** | |
| **8051 Timers and Serial Port:** 8051 Timers and Counters – Operation and Assembly language programming to generate a pulse | L1, L2, L3 |

| | |
|---|---|
| using Mode-1 and a square wave using Mode-2 on a port pin.<br>8051 Serial Communication- Basics of Serial Data Communication, RS-232 standard, 9 pin RS232 signals, Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially. | |
| **Module -5** | |
| **8051 Interrupts and Interfacing Applications:** 8051 Interrupts. 8051 Assembly language programming to generate an external interrupt using a switch, 8051 C programming to generate a square waveform on a port pin using a Timer interrupt.<br>Interfacing 8051 to ADC-0804, LCD and Stepper motor and their 8051 Assembly language interfacing programming. | L1, L2, L3 |

**Evaluation of Internal Assessment Marks:**

It is suggested that at least a few simple programs to be executed by students using a simulation software or an 8051 microcontroller kit for better understanding of the course. This activity can be considered for the evaluation of 5 marks out of 20 Internal assessment marks, reserved for the other activities.

**Course outcomes:** At the end of the course, students will be able to:

- Explain the difference between Microprocessors & Microcontrollers, Architecture of 8051 Microcontroller, Interfacing of 8051 to external memory and Instruction set of 8051.
- Write 8051 Assembly level programs using 8051 instruction set.
- Explain the Interrupt system, operation of Timers/Counters and Serial port of 8051.
- Write 8051 Assembly language program to generate timings and waveforms using 8051 timers, to send & receive serial data using 8051 serial port and to generate an external interrupt using a switch.
- Write 8051 C programs to generate square wave on 8051 I/O port pin using interrupt and to send & receive serial data using 8051 serial port.
- Interface simple switches, simple LEDs, ADC 0804, LCD and Stepper Motor to 8051 using 8051 I/O ports.

**Question paper pattern:**

- The question paper will have ten questions.
- Each full Question consisting of 16 marks
- There will be 2 full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

**TEXT BOOKS:**

1. **"The 8051 Microcontroller and Embedded Systems – using assembly and C ",** Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay; PHI, 2006 / Pearson, 2006.
2. **"The 8051 Microcontroller",** Kenneth J. Ayala, 3rd Edition, Thomson/Cengage Learning.

**REFERENCE BOOKS:**

1. **"The 8051 Microcontroller Based Embedded Systems",** Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4.
2. **"Microcontrollers: Architecture, Programming, Interfacing and System Design",** Raj Kamal, Pearson Education, 2005.

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## B.E E&C SIXTH SEMESTER SYLLABUS

## DIGITAL COMMUNICATION

**B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering**

[As per Choice Based Credit System (CBCS) scheme]

| | | | |
|---|---|---|---|
| Subject Code | 15EC61 | IA Marks | 20 |
| Number of Lecture Hours/Week | 04 | Exam Marks | 80 |
| Total Number of Lecture Hours | 50 (10 Hours/Module) | Exam Hours | 03 |
| CREDITS – 04 | | | |

**Course Objectives:** The objectives of the course is to enable students to:

- Understand the mathematical representation of signal, symbol, noise and channels.
- Apply the concept of signal conversion to symbols and signal processing to symbols in transmitter and receiver functional blocks.
- Compute performance issues and parameters for symbol processing and recovery in ideal and corrupted channel conditions.
- Compute performance parameters and mitigate for these parameters in corrupted and distorted channel conditions.

| Module-1 | RBT Level |
|---|---|
| **Bandpass Signal to Equivalent Lowpass**: Hilbert Transform, Pre-envelopes, Complex envelopes, Canonical representation of bandpass signals, Complex low pass representation of bandpass systems, Complex representation of band pass signals and systems (Text 1: 2.8, 2.9, 2.10, 2.11, 2.12, 2.13).<br>**Line codes:** Unipolar, Polar, Bipolar (AMI) and Manchester code and their power spectral densities (Text 1: Ch 6.10).<br>Overview of HDB3, B3ZS, B6ZS (Ref. 1: 7.2) | L1, L2, L3 |
| **Module-2** | |
| **Signaling over AWGN Channels**- Introduction, Geometric representation of signals, Gram-Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel, Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver (Text 1: 7.1, 7.2, 7.3, 7.4). | L1, L2, L3 |
| **Module-3** | |
| **Digital Modulation Techniques**: Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M–ary PSK, M–ary QAM (Relevant topics in Text 1 of 7.6, 7.7).<br>Frequency shift keying techniques using Coherent detection: BFSK | |

| | |
|---|---|
| generation, detection and error probability (Relevant topics in Text 1 of 7.8).<br><br>Non coherent orthogonal modulation techniques: BFSK, DPSK Symbol representation, Block diagrams treatment of Transmitter and Receiver, Probability of error (without derivation of probability of error equation) (Text 1: 7.11, 7.12. 7.13). | |
| **Module-4** | |
| **Communication through Band Limited Channels**: Digital Transmission through Band limited channels: Digital PAM Transmission through Band limited Channels, Signal design for Band limited Channels: Design of band limited signals for zero ISI–The Nyquist Criterion (statement only), Design of band limited signals with controlled ISI-Partial Response signals, Probability of error for detection of Digital PAM: Probability of error for detection of Digital PAM with Zero ISI, Symbol–by–Symbol detection of data with controlled ISI (Text 2: 9.1, 9.2, 9.3.1, 9.3.2).<br><br>Channel Equalization: Linear Equalizers (ZFE, MMSE), Adaptive Equalizers (Text 2: 9.4.2). | L1, L2, L3 |
| **Module-5** | |
| **Principles of Spread Spectrum:** Spread Spectrum Communication Systems: Model of a Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Systems, Effect of De-spreading on a narrowband Interference, Probability of error (statement only), Some applications of DS Spread Spectrum Signals, Generation of PN Sequences, Frequency Hopped Spread Spectrum, CDMA based on IS-95 (Text 2: 11.3.1, 11.3.2, 11.3.3, 11.3.4, 11.3.5, 11.4.2). | L1, L2, L3 |
| **Course Outcomes:** At the end of the course, the students will be able to:<br>• Associate and apply the concepts of Bandpass sampling to well specified signals and channels.<br>• Analyze and compute performance parameters and transfer rates for low pas and bandpass symbol under ideal and corrupted non band limited channels.<br>• Test and validate symbol processing and performance parameters at the receiver under ideal and corrupted bandlimited channels.<br>• Demonstrate by simulation and emulation that bandpass signals subjected to corrupted and distorted symbols in a bandlimited channel, can be demodulated and estimated at receiver to meet specified performance criteria. | |
| **Question paper pattern:**<br>• The question paper will have ten questions<br>• Each full question consists of 16 marks.<br>• There will be 2 full questions (with a maximum of Three sub questions) from each module.<br>• Each full question will have sub questions covering all the topics under a module<br>• The students will have to answer 5 full questions, selecting one full question from each module | |
| **Text Books:** | |

1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN 978-0-471-64735-5.
2. John G Proakis and Masoud Salehi, "Fundamentals of Communication Systems", 2014 Edition, Pearson Education, ISBN 978-8-131-70573-5.

**Reference Books:**

1. B.P.Lathi and Zhi Ding, "Modern Digital and Analog communication Systems", Oxford University Press, 4th Edition, 2010, ISBN: 978-0-198-07380-2.
2. Ian A Glover and Peter M Grant, "Digital Communications", Pearson Education, Third Edition, 2010, ISBN 978-0-273-71830-7.
3. John G Proakis and Masoud Salehi, "Communication Systems Engineering", 2nd Edition, Pearson Education, ISBN 978-93-325-5513-6.

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# ARM MICROCONTROLLER & EMBEDDED SYSTEMS

**B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering**
[As per Choice Based Credit System (CBCS) scheme]

| ARM MICROCONTROLLER & EMBEDDED SYSTEMS<br>**B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering**<br>**[As per Choice Based Credit System (CBCS) Scheme]** | | | |
|---|---|---|---|
| **Course Code** | **15EC62** | **IA Marks** | **20** |
| **Number of Lecture Hours/Week** | **04** | **Exam Marks** | **80** |
| **Total Number of Lecture Hours** | **50 (10 Hours / Module)** | **Exam Hours** | **03** |

**CREDITS – 04**

**Course objectives:** This course will enable students to:

- Understand the architectural features and instruction set of 32 bit microcontroller ARM Cortex M3.
- Program ARM Cortex M3 using the various instructions and C language for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Develop the hardware software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

**Module-1**

**ARM-32 bit Microcontroller:** Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Text 1: Ch 1, 2, 3) **L1, L2**

**Module-2**

**ARM Cortex M3 Instruction Sets and Programming:** Assembly basics, Instruction list and description, Useful instructions, Memory mapping, Bit-band operations and CMSIS, Assembly and C language Programming (Text 1: Ch-4, Ch-5, Ch-10 (10.1, 10.2, 10.3, 10.5 only) **L1, L2, L3**

**Module-3**

**Embedded System Components:** Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Core of an Embedded System including all types of processor/controller, Memory, Sensors, Actuators, LED, 7 segment LED display, Optocoupler, Relay, Piezo buzzer, Push button switch, Communication Interface (onboard and external types), Embedded firmware, Other system components.
(Text 2: All the Topics from Ch-1 and Ch-2, excluding 2.3.3.4 (stepper motor), 2.3.3.8 (keyboard) and 2.3.3.9 (PPI) sections). **L1, L2, L3**

**Module-4**

**Embedded System Design Concepts:** Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded

Systems-Application and Domain specific, Hardware Software Co-Design and Program Modelling (excluding UML), Embedded firmware design and development (excluding C language).

(Text 2: Ch-3, Ch-4, Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only) **L1, L2, L3**

**Module-5**

**RTOS and IDE for Embedded System Design:** Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques

(Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch 12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only) **L1, L2, L3**

**Course outcomes:** After studying this course, students will be able to:

- Describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.
- Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Develop the hardware /software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

**Text Books:**


1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", 2nd Edition, Newnes, (Elsevier), 2010.

2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2nd Edition.


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## VLSI Design

**B.E., VI Semester, Electronics & Communication Engineering**

[As per Choice Based Credit System (CBCS) scheme]

| | | | |
|---|---|---|---|
| Subject Code | 15EC63 | IA Marks | 20 |
| Number of Lecture Hours/Week | 04 | Exam Marks | 80 |
| Total Number of Lecture Hours | 50 (10 Hours / Module) | Exam Hours | 03 |
| CREDITS – 04 | | | |

**Course Objectives:** The objectives of the course is to enable students to:

- Impart knowledge of MOS transistor theory and CMOS technologies
- Impart knowledge on architectural choices and performance tradeoffs involved in designing and realizing the circuits in CMOS technology
- Cultivate the concepts of subsystem design processes
- Demonstrate the concepts of CMOS testing

| Module-1 | RBT Level |
|---|---|
| **Introduction:** A Brief History, MOS Transistors, MOS Transistor Theory, Ideal I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics (1.1, 1.3, 2.1, 2.2, 2.4, 2.5 of TEXT2).<br>**Fabrication:** nMOS Fabrication, CMOS Fabrication [P-well process, N-well process, Twin tub process], BiCMOS Technology (1.7, 1.8,1.10 of TEXT1). | L1, L2 |
| **Module-2** | |
| **MOS and BiCMOS Circuit Design Processes**: MOS Layers, Stick Diagrams, Design Rules and Layout.<br>**Basic Circuit Concepts:** Sheet Resistance, Area Capacitances of Layers, Standard Unit of Capacitance, Some Area Capacitance Calculations, Delay Unit, Inverter Delays, Driving Large Capacitive Loads (3.1 to 3.3, 4.1, 4.3 to 4.8 of TEXT1). | L1, L2, L3 |
| **Module-3** | |
| **Scaling of MOS Circuits**: Scaling Models & Scaling Factors for Device Parameters<br>**Subsystem Design Processes:** Some General considerations, An illustration of Design Processes, **Illustration of the Design Processes**- Regularity, Design of an ALU Subsystem, The Manchester Carry-chain and Adder Enhancement Techniques(5.1, 5.2, 7.1, 7.2, 8.2, 8.3, 8.4.1, 8.4.2 of TEXT1). | L1, L2, L3 |
| **Module-4** | |
| **Subsystem Design:** Some Architectural Issues, Switch Logic, Gate(restoring) Logic, Parity Generators, Multiplexers, The Programmable Logic Array (PLA) (6.1to 6.3, 6.4.1, 6.4.3, 6.4.6 of TEXT1).<br>**FPGA Based Systems:** Introduction, Basic concepts, Digital design and FPGA's, FPGA based System design, FPGA architecture, Physical design for FPGA's<br>(1.1 to 1.4, 3.2, 4.8 of TEXT3). | L1, L2, L3 |
| **Module-5** | |
| **Memory, Registers and Aspects of system Timing**- System Timing Considerations, Some commonly used Storage/Memory elements (9.1, 9.2 of TEXT1). | L1, L2, L3 |

| | |
|---|---|
| **Testing and Verification:** Introduction, Logic Verification, Logic Verification Principles, Manufacturing Test Principles, Design for testability (12.1, 12.1.1, 12.3, 12.5, 12.6 of TEXT 2). | |

**Course outcomes:** At the end of the course, the students will be able to:

- Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
- Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
- Interpret Memory elements along with timing considerations
- Demonstrate knowledge of FPGA based system design
- Interpret testing and testability issues in VLSI Design
- Analyze CMOS subsystems and architectural issues with the design constraints.

**Question paper pattern:**

- The question paper will have ten questions
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

**Text Books:**


1. **"Basic VLSI Design"**- Douglas A. Pucknell& Kamran Eshraghian, PHI 3rd Edition (original Edition – 1994).
2. **"CMOS VLSI Design- A Circuits and Systems Perspective"**- Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.
3. **"FPGA Based System Design"-** Wayne Wolf, Pearson Education, 2004, Technology and Engineering.


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## COMPUTER COMMUNICATION NETWORKS

**B.E., VI Semester, Electronics & Communication Engineering / Telecommunication Engineering**

[As per Choice Based Credit System (CBCS) scheme]

| COMPUTER COMMUNICATION NETWORKS<br>B.E., VI Semester, Electronics & Communication Engineering / Telecommunication Engineering<br>[As per Choice Based Credit System (CBCS) Scheme] | | | |
|---|---|---|---|
| **Course Code** | **15EC64** | **IA Marks** | **20** |
| **Number of Lecture Hours/Week** | **04** | **Exam Marks** | **80** |
| **Total Number of Lecture Hours** | **50 (10 Hours / Module)** | **Exam Hours** | **03** |

**CREDITS – 04**

**Course Objectives:** This course will enable students to:

- Understand the layering architecture of OSI reference model and TCP/IP protocol suite.
- Understand the protocols associated with each layer.
- Learn the different networking architectures and their representations.
- Learn the various routing techniques and the transport layer services.

**Module-1**

**Introduction:** Data Communications: Components, Representations, Data Flow, Networks: Physical Structures, Network Types: LAN, WAN, Switching, Internet.
**Network Models:** Protocol Layering: Scenarios, Principles, Logical Connections, TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP.
**Data-Link Layer:** Introduction: Nodes and Links, Services, Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services: Framing, Flow and Error Control, Data Link Layer Protocols: Simple Protocol, Stop and Wait protocol, Piggybacking. **L1, L2**

**Module-2**

**Media Access Control:** Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA. Controlled Access: Reservation, Polling, Token Passing.
**Wired LANs: Ethernet:** Ethernet Protocol: IEEE802, Ethernet Evolution, Standard Ethernet: Characteristics, Addressing, Access Method, Efficiency, Implementation, Fast Ethernet: Access Method, Physical Layer, Gigabit Ethernet: MAC Sublayer, Physical Layer, 10 Gigabit Ethernet. **L1, L2**

**Module-3**

**Wireless LANs:** Introduction: Architectural Comparison, Characteristics, IEEE 802.11: Architecture, MAC Sublayer, Addressing Mechanism, Physical Layer, Bluetooth: Architecture, Layers.
**Connecting Devices:** Hubs, Switches, **Virtual LANs:** Membership, Configuration, Communication between Switches and Routers, Advantages.
**Network Layer:** Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing,

DHCP, Network Address Resolution, Forwarding of IP Packets: Based on destination Address and Label. **L1, L2**

**Module-4**

**Network Layer Protocols:** Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams, ICMPv4: Messages, Debugging Tools, Mobile IP: Addressing, Agents, Three Phases, Inefficiency in Mobile IP.

**Unicast Routing:** Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing, Unicast Routing Protocol: Internet Structure, Routing Information Protocol, Open Shortest Path First, Border Gateway Protocol Version 4. **L1, L2, L3**

**Module-5**

**Transport Layer:** Introduction: Transport Layer Services, Connectionless and Connection oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-Back-N Protocol, Selective repeat protocol, User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Flow control, Error control, TCP congestion control. **L1, L2**

**Course Outcomes:** At the end of the course, the students will be able to:

- Identify the protocols and services of Data link layer.
- Identify the protocols and functions associated with the transport layer services.
- Describe the layering architecture of computer networks and distinguish between the OSI reference model and TCP/IP protocol suite.
- Distinguish the basic network configurations and standards associated with each network.
- Construct a network model and determine the routing of packets using different routing algorithms.

**Text Book:**

Data Communications and Networking , Forouzan, 5th Edition, McGraw Hill, 2016 ISBN: 1-25-906475-3

**Reference Books:**

1. Computer Networks, James J Kurose, Keith W Ross, Pearson Education, 2013, ISBN: 0-273-76896-4
2. Introduction to Data Communication and Networking, Wayarles Tomasi, Pearson Education, 2007, ISBN:0130138282

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