VISVESVARAYA TECHNOLOGICAL UNIVERSITY

"Jnana Sangama" Belagavi – 590 010

PROJECT REPORT ON

"DESIGN AND IMPLEMENTATION OF KOGGE-STONE ADDER USING CADENCE VIRTUOSO PLATFORM"

Submitted in partial fulfillment of the requirements for the award of degree

BACHELOR OF ENGINEERING
IN
ELECTRONICS & COMMUNICATION ENGINEERING

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CERTIFICATE

Certified that the project work entitled "**DESIGN AND IMPLEMENTATION OF KOGGE-STONE ADDER USING CADENCE VIRTUOSO PLATFORM**" *is a bona fide work carried out by*

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in partial fulfillment for the award of BACHELOR OF ENGINEERING in **ELECTRONICS & COMMUNICATION ENGINEERING** of the **VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI** during the year 2018–2019. It is certified that all corrections/suggestions indicated for Internal Assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the Bachelor of Engineering Degree.

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ABSTRACT

In this technical era, high speed and low area of Very Large Scale Integration (VLSI) chip are very essential factors. Day by day, the number of transistors and other active and passive elements are growing on the VLSI chip. In the integral part of most processors, adders play an important role. An adder forms a major part in various arithmetic logical operations. Parallel Prefix Adders (PPA) have been built up as the most essential and efficient circuit for binary addition. Their Particular structure and execution performance are very attractive for VLSI implementation. The Adders are a practically mandatory part of each contemporary digital Integrated Circuit (IC). The essential property of the adder is that it should be primarily faster and efficiency must higher with respect to power utilization and the area occupied. PPA'S are tree based structure which speed up the binary addition, Hence prefix adders are used for fast addition algorithms.

The proposed work of the 32-bit Kogge-Stone Adder (KSA) is designed in front end by using Verilog code and the 8-bit KSA is designed in back end using CMOS logic which includes different modules such as white cell, gray cell and black cell and it is implemented in Cadence Virtuoso platform using 180nm technology. The comparative analysis of the delay and power has been done with previous paper. The experimental result shows that the addition by using KSA reduces power consumption and delay.