VISVESVARAYA TECHNOLOGICAL UNIVERSITY

"Jnana Sangama" Belagavi – 590 010

PROJECT REPORT ON

"DESIGN AND IMPLEMENTATION OF POWER REDUCTION TECHNIQUE IN CMOS VLSI CIRCUITS"

Submitted in partial fulfillment of the requirements for the award of degree

BACHELOR OF ENGINEERING
IN
ELECTRONICS & COMMUNICATION ENGINEERING

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(Affiliated to VTU, **BELAGAVI**)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

CERTIFICATE

Certified that the project work entitled "**DESIGN AND IMPLEMENTATION OF POWER REDUCTION TECHNIQUE IN CMOS VLSI CIRCUITS**" *is a bona fide work carried out by*

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in partial fulfillment for the award of **BACHELOR** OF ENGINEERING in **ELECTRONICS & COMMUNICATION ENGINEERING of the VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI** during the year 2018–2019. It is certified that all corrections/suggestions indicated for Internal Assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the Bachelor of Engineering Degree.

13/05/19

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ABSTRACT

In (Very Large-Scale Integration) VLSI, it is important to introduce low-power design techniques, which reduces the power consumption of the circuit during normal mode of operation. More power consumption also reduces the battery life of the devices. Therefore, reducing power consumption during normal operation has become a critical objective in today's VLSI circuit designs. Designers have different options to reduce the power consumption in the various design stages. Power dissipation in CMOS circuits can be dynamic or static. Dynamic power dissipation takes place due to switching activities and static power consumption is due to leakage.

The lector technique in combination with sleep and stack technique is used in this project. Two leakage control transistors (a p-type and a n-type) within the logic gate circuit are introduced for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other. In this arrangement, one of the LCTs is always near its cut-off voltage for any input combination. This increases the resistance of the path from supply to ground, leading to significant decrease in leakage current. Stack technique is used to store the current state of the transistors whereas sleep technique is used to turn off the circuit when there is no input to given circuit.