VISVESVARAYA TECHNOLOGICAL UNIVERSITY

"Jnana Sangama" Belagavi – 590010

PROJECT REPORT ON

"DESIGN OF LOW POWER HIGH SPEED AREA EFFICIENT WALLACE TREE MULTIPLIER USING REDUCTION LOGIC"

Submitted in partial fulfillment of the requirements for the award of degree

BACHELOR OF ENGINEERING
IN
ELECTRONICS & COMMUNICATION ENGINEERING

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CERTIFICATE

Certified that the project work entitled **"DESIGN OF LOW POWER HIGH SPEED AREA EFFICIENT WALLACE TREE MULTIPLIER USING REDUCTION LOGIC"** is a bonafide work carried out by

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in partial fulfillment for the award of **BACHELOR** of ENGINEERING in **ELECTRONICS & COMMUNICATION ENGINEERING** of the **VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI** during the year 2017–2018. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of project work prescribed for the Bachelor of Engineering degree.

24/05/18 D.V. 24/05/18

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ABSTRACT

Multiplier is a vital block in high speed digital signal processing applications. The more stress in modern very large scale integrated circuits design under which main constraints are power, silicon area and delay, in all the high-speed application in very large scale integrated circuits fields. Wallace tree multiplier is a three-stage operation, which again leads to lesser number of stages and subsequently less number of transistors which resolves the hardware complexity and ultimately reduces the delay, area.

The disadvantage in the standard wallace tree multiplier is that if there are two bits in a particular column of group of three rows half adders are used in every stage, so area and complexity of circuit increases and consumes more power. The proposed wallace tree multiplier design incorporates reduction logic and low power full adder. It is similar to that of standard wallace tree multiplier, difference is that it uses half adders when necessary. The reduction logic method helps in reducing the complexity greatly denying the half adders with 65-75% reduction, which in turn makes the wallace tree multiplier low power, high speed and area efficient.