VISVESVARAYA TECHNOLOGICAL UNIVERSITY

Belagavi – 590 010

PROJECT REPORT

ON

"DESIGN AND IMPLEMENTATION OF LOW POWER ADDER USING CADENCE VIRTUOSO PLATFORM"

Submitted in partial fulfillment of the requirements for the award of degree

BACHELOR OF ENGINEERING
IN
ELECTRONICS & COMMUNICATION ENGINEERING

Submitted By

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

CERTIFICATE

Certified that the project work entitled "**DESIGN AND IMPLEMENTATION OF LOW POWER ADDER USING CADENCE VIRTUOSO PLATFORM** *"is a bonafide work carried out by*

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in partial fulfillment for the award of BACHELOR OF ENGINEERING in **ELECTRONICS & COMMUNICATION ENGINEERING** of the **VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI** during the year 2015–2016. It is certified that all corrections/suggestions indicated for Internal Assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the Bachelor of Engineering Degree.

21/05/16

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ABSTRACT

The Gate Diffusion Input is a novel technique for a low power digital circuit design. This technique reduces the power dissipation, propagation delay, area of digital circuits and it maintains low complexity of logic design. Power management has become major issue in the development of digital system especially, in the portable devices in which enhancement of battery life time and reducing charging time are becoming challenging issues day by day.

The major problem in the power management is power dissipation. Performance comparison with traditional CMOS and various PTL design techniques is presented, with respect to layout area, number of devices, delay and power dissipation, showing advantages and drawbacks of GDI as compared to other methods.Full adder circuit is functional building block of microprocessors, digital signal processors orany ALUs. In this paper leakage power is reduced by using less number of transistors with thetechniques like GDI (Gate Diffusion Input) and PTL (Pass Transistor Logic) techniques.

The whole processes for development of digital circuits and simulation was done by using CADENCE backend tool. This method can also extended to the processors and other level designs for optimization of power dissipation, area and delay in order to increase the circuit efficiency.