

VLSI LAB

B.E., VII Semester, Electronics & Communication Engineering
[Choice Based Credit System (CBCS) Scheme]

Course Code	17ECL77	CIE Marks	40
Number of Lecture Hours/Week	01 Hr Tutorial (Instructions) + 02 Hours Laboratory = 03	SEE Marks	60
RBT Levels	L1, L2, L3	Exam Hours	03

CREDITS - 02

Course objective: This course will enable students to:

- Explore the CAD tool and understand the flow of the Full Custom IC design cycle.
- Learn DRC, LVS and Parasitic Extraction of the various designs.
- Design and simulate the various basic CMOS analog circuits and use them in higher circuits like op-amp, converters using design abstraction concepts.
- Design and simulate the various basic CMOS digital circuits and use them in higher circuits like mux, and shift registers using design abstraction concepts.

Experiments can be conducted using any of the following or equivalent design tools: Cadence Synopsys/Mentor Graphics/Microwind

Laboratory Experiments**PART - A****ASIC-DIGITAL DESIGN**

1. Write Verilog code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with technological library with given constraints. Do the initial timing verification with gate level simulation.
 - i. Arithmetic
 - ii. Arithmetic
 - iii. Transmission Gate
 - iv. Basic universal gates
 - v. Flip-flop D, JK, MS, T
 - vi. Static CMOS adder
 - vii. 4 bit counter [Synchronous and Asynchronous counter]
 - viii. Static CMOS approximation register [SAR]

VLSI LAB

B.E., VII Semester, Electronics & Communication Engineering
[As per Choice Based Credit System (CBCS) Scheme]

Course Code	17ECL77	CIE Marks	40
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory = 03	SEE Marks	60
RBT Levels	L1, L2, L3	Exam Hours	03

CREDITS - 02

Course objectives: This course will enable students to:

- Explore the CAD tool and understand the flow of the Full Custom IC design cycle.
- Learn DRC, LVS and Parasitic Extraction of the various designs.
- Design and simulate the various basic CMOS analog circuits and use them in higher circuits like data converters using design abstraction concepts.
- Design and simulate the various basic CMOS digital circuits and use them in higher circuits like adders and shift registers using design abstraction concepts.

Experiments can be conducted using any of the following or equivalent design tools: Cadence/Synopsis/Mentor Graphics/Microwind

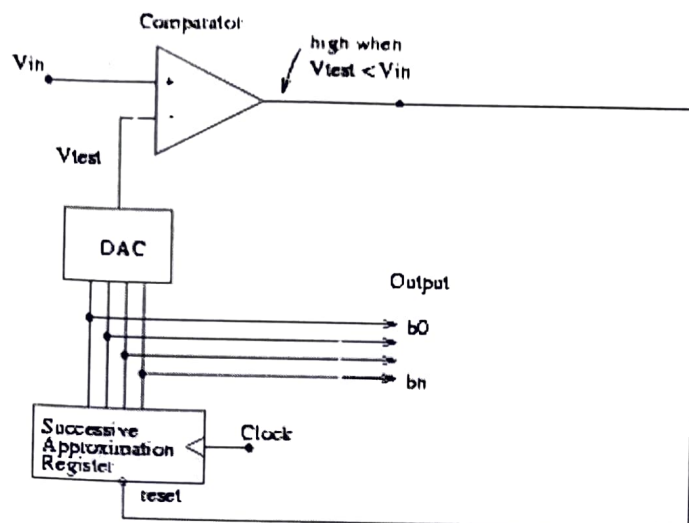
Laboratory Experiments**PART - A****ASIC-DIGITAL DESIGN**

1. Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with technological library with given constraints*. Do the initial timing verification with gate level simulation.
 - i. An inverter
 - ii. A Buffer
 - iii. Transmission Gate
 - iv. Basic/universal gates
 - v. Flip flop -RS, D, JK, MS, T
 - vi. Serial & Parallel adder
 - vii. 4-bit counter [Synchronous and Asynchronous counter]
 - viii. Successive approximation register [SAR]

PART - B
ANALOG DESIGN

1. Design an Inverter with given specifications**, completing the design flow mentioned below:
 - a. Draw the schematic and verify the following
 - i) DC Analysis
 - ii) Transient Analysis
 - b. Draw the Layout and verify the DRC, ERC
 - c. Check for LVS
 - d. Extract RC and back annotate the same and verify the Design
 - e. Verify & Optimize for Time, Power and Area to the given constraint*
2. Design the (i) Common source and Common Drain amplifier and (ii) A Single Stage differential amplifier, with given specifications**, completing the design flow mentioned below:
 - a. Draw the schematic and verify the following
 - i) DC Analysis
 - ii) AC Analysis
 - iii) Transient Analysis
 - b. Draw the Layout and verify the DRC, ERC
 - c. Check for LVS
 - d. Extract RC and back annotate the same and verify the Design.
3. Design an op-amp with given specification** using given differential amplifier Common source and Common Drain amplifier in library*** and completing the design flow mentioned below:
 - a. Draw the schematic and verify the following
 - i) DC Analysis
 - ii). AC Analysis
 - iii) Transient Analysis
 - b. Draw the Layout and verify the DRC, ERC
 - c. Check for LVS
 - d. Extract RC and back annotate the same and verify the Design.
4. Design a 4 bit R-2R based DAC for the given specification and completing the design flow mentioned using given op-amp in the library***.
 - a. Draw the schematic and verify the following
 - i) DC Analysis
 - ii) AC Analysis
 - iii) Transient Analysis
 - b. Draw the Layout and verify the DRC, ERC

5. For the SAR based ADC mentioned in the figure below draw the mixed signal schematic and verify the functionality by completing ASIC Design FLOW.
[Specifications to GDS-II]



- * An appropriate constraint should be given.
- ** Appropriate specification should be given.
- *** Applicable Library should be added & information should be given to the Designer.

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Write test bench to simulate various digital circuits.
- Interpret concepts of DC Analysis, AC Analysis and Transient Analysis in analog circuits.
- Design and simulate basic CMOS circuits like inverter, common source amplifier and differential amplifiers.
- Use basic amplifiers and further design higher level circuits like operational amplifier and analog/digital converters to meet desired parameters.
- Use transistors to design gates and further using gates realize shift registers and adders to meet desired parameters.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination, one question from **PART-A** and one question from **PART-B** to be set.
- Students are allowed to pick one experiment from the lot.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

D.V. [Signature]

H. O. D.

Dept. Of Electronics & Communication
MRCET Institute of Engg. & Technology
Wizag, MCGOBIKOTI - 574 225