SWITCHING & FINITE AUTOMATA THEORY

B.E., V Semester, Electronics & Communication Engineering / Telecommunication Engineering

[As per Choice Based Credit System (CBCS) Scheme]

Course Code	**17EC552**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Objectives: This course will enable students to:

- Understand the basics of threshold logic, effect of hazards on digital circuits and techniques of fault detection
- Explain finite state model and minimization techniques
- Know structure of sequential machines, and state identification
- Understand the concept of fault detection experiments

Module-1

Threshold Logic: Introductory Concepts: Threshold element, capabilities and limitations of threshold logic, Elementary Properties, Synthesis of Threshold networks: Unate functions, Identification and realization of threshold functions, The map as a tool in synthesizing threshold networks. (Sections 7.1, 7.2 of Text)
L1, L2, L3

Module-2

Reliable Design and Fault Diagnosis: Hazards, static hazards, Design of Hazard-free Switching Circuits, Fault detection in combinational circuits, Fault detection in combinational circuits: The faults, The Fault Table, Covering the fault table, Fault location experiments: Preset experiments, Adaptive experiments, Boolean differences, Fault detection by path sensitizing. (Sections 8.1, 8.2, 8.3, 8.4, 8.5 of Text)
L1, L2, L3

Module-3

Sequential Machines: Capabilities, Minimization and Transformation
The Finite state model and definitions, capabilities and limitations of finite state machines, State equivalence and machine minimization: k-equivalence, The minimization Procedure, Machine equivalence, Simplification of incompletely specified machines. (Section 10.1, 10.2, 10.3, 10.4 of Text) **L1, L2, L3**

Module-4

Structure of Sequential Machines: Introductory example, State assignment using partitions: closed partitions, The lattice of closed partitions, Reduction of output dependency, Input dependence and autonomous clocks, Covers and generation of closed partitions by state splitting: Covers, The implication graph, An application of state splitting to parallel decomposition. (Section 12.1, 12.2, 12.3, 12.4, 12.5, 12.6 of Text) **L1, L2, L3**

Module-5

State-Identification and Fault Detection Experiments: Experiments, Homing experiments, Distinguishing experiments, Machine identification, Fault detection experiments, Design of diagnosable machines, Second algorithm for the design of

fault detection experiments. (Sections 13.1, 13.2, 13.3, 13.4, 13.5, 13.6, 13.7 of Text) **L1, L2, L3**

Course outcomes: At the end of the course, students should be able to:

- Explain the concept of threshold logic
- Understand the effect of hazards on digital circuits and fault detection and analysis
- Define the concepts of finite state model
- Analyze the structure of sequential machine
- Explain methods of state identification and fault detection experiments

Text Book:

Switching and Finite Automata Theory – Zvi Kohavi, McGraw Hill, 2nd edition, 2010 ISBN: 0070993874.

Reference Books:

1. **Fault Tolerant And Fault Testable Hardware Design**-Parag K Lala, Prentice Hall Inc. 1985.
2. **Digital Circuits and Logic Design**.-Charles Roth Jr, Larry L. Kinney, Cengage Learning, 2014, ISBN: 978-1-133-62847-7.

H. O. D.
Dept. Of Electronics & Communication
Alva's Institute of Engg. & Technology
Mijar MOODBIDRI - 574 225