VERILOG HDL

B.E., V Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) Scheme]

Course Code	**17EC53**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 04

Course objectives: This course will enable students to:

- Differentiate between Verilog and VHDL descriptions.
- Learn different Verilog HDL and VHDL constructs.
- Familiarize the different levels of abstraction in Verilog.
- Understand Verilog Tasks and Directives.
- Understand timing and delay Simulation.
- Learn VHDL at design levels of data flow, behavioral and structural for effective modeling of digital circuits.

Module-1

Overview of Digital Design with Verilog HDL

Evolution of CAD, emergence of HDLs, typical HDL-flow, why Verilog HDL?, trends in HDLs. (Text1)

Hierarchical Modeling Concepts

Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block. (Text1)

L1, L2, L3

Module-2

Basic Concepts

Lexical conventions, data types, system tasks, compiler directives. (Text1)

Modules and Ports

Module definition, port declaration, connecting ports, hierarchical name referencing. (Text1) **L1, L2, L3**

Module-3

Gate-Level Modeling

Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays. (Text1)

Dataflow Modeling

Continuous assignments, delay specification, expressions, operators, operands, operator types. (Text1) **L1, L2, L3**

Module-4

Behavioral Modeling

Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks. (Text1) **L1, L2, L3**

Module-5

Introduction to VHDL

Introduction: Why use VHDL?, Shortcomings, Using VHDL for Design Synthesis,

Design tool flow, Font conventions.

Entities and Architectures: Introduction, A simple design, Design entities, Identifiers, Data objects, Data types, and Attributes. (Text 2) **L1, L2, L3**

Course Outcomes: At the end of this course, students should be able to

- Write Verilog programs in gate, dataflow (RTL), behavioral and switch modeling levels of Abstraction.
- Write simple programs in VHDL in different styles.
- Design and verify the functionality of digital circuit/system using test benches.
- Identify the suitable Abstraction level for a particular digital design.
- Write the programs more effectively using Verilog tasks and directives.
- Perform timing and delay Simulation.

Text Books:

1. Samir Palnitkar, **"Verilog HDL: A Guide to Digital Design and Synthesis"**, Pearson Education, Second Edition.
2. Kevin Skahill, **"VHDL for Programmable Logic"**, PHI/Pearson education, 2006.

Reference Books:

1. Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer Science+Business Media, LLC, Fifth edition.
2. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.
3. Padmanabhan, Tripura Sundari, "Design through Verilog HDL", Wiley, 2016 or earlier.

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