MICROPROCESSORS
SEMESTER – IV (EC/TC)
[As per Choice Based Credit System (CBCS) Scheme]

Course Code	**17EC46**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 03

Course objectives: This course will enable students to:

- Familiarize basic architecture of 8086 microprocessor
- Program 8086 Microprocessor using Assembly Level Language
- Use Procedures in 8086 Programs
- Understand interfacing of 16 bit microprocessor with memory and peripheral chips involving system design
- Understand the Von-Neumann, Harvard, CISC & RISC CPU architecture.

Module -1

8086 PROCESSOR: Historical background (refer Reference Book 1), 8086 CPU Architecture (1.1 – 1.3 of Text).

Addressing modes, Machine language instruction formats. (2.2, 2.1 of Text).

INSTRUCTION SET OF 8086: Data transfer and arithmetic instructions. Control/Branch Instructions, Illustration of these instructions with example programs (2.3 of Text). **L1, L2, L3**

Module -2

Logical Instructions, String manipulation instructions, Flag manipulation and Processor control instructions, Illustration of these instructions with example programs. Assembler Directives and Operators, Assembly Language Programming and example programs (2.3, 2.4, 3.4 of Text). **L1, L2, L3**

Module -3

Stack and Interrupts:
Introduction to stack, Stack structure of 8086, Programming for Stack. Interrupts and Interrupt Service routines, Interrupt cycle of 8086, NMI, INTR, Interrupt programming, Timing and Delays. (Chap. 4 of Text). **L1, L2, L3**

Module -4

8086 Bus Configuration and Timings:
Physical memory Organization, General Bus operation cycle, I/O addressing capability, Special processor activities, Minimum mode 8086 system and Timing diagrams, Maximum Mode 8086 system and Timing diagrams. (1.4 to 1.9 of Text).

Basic Peripherals and their Interfacing with 8086 (Part 1): Static RAM Interfacing with 8086 (5.1.1), Interfacing I/O ports, PIO 8255, Modes of operation – Mode-0 and BSR Mode, Interfacing simple switches and simple LEDs using 8255 (Refer 5.3, 5.4, 5.5 of Text). **L1, L2, L3**

Module 5
Basic Peripherals and their Interfacing with 8086 (Part 2): Interfacing ADC-0808/0809, DAC-0800, Stepper Motor using 8255 (5.6.1, 5.7.2, 5.8). Timer 8254 – Mode 0 & 3 and Interfacing programmes for these modes (refer 6.1 of Text). **INT 21H DOS Function calls** - for handling Keyboard and Display (refer Appendix-B of Text). Von-Neumann & Harvard CPU architecture and CISC & RISC CPU architecture (refer Reference Book 1). **L1, L2, L3**
Course Outcomes: At the end of the course students will be able to: • Explain the History of evaluation of Microprocessors, Architecture and instruction set of 8086, CISC & RISC, Von-Neumann & Harvard CPU Architecture, Configuration & Timing diagrams of 8086 and Instruction set of 8086. • Write 8086 Assembly level programs using the 8086 instruction set • Write modular programs using procedures. • Write 8086 Stack and Interrupts programming. • Interface 8086 to Static memory chips and 8255, 8254, 0808 ADC, 0800 DAC, Keyboard, Display and Stepper motors. • Use INT 21 DOS interrupt function calls to handle Keyboard and Display.
Text Book: **Advanced Microprocessors and Peripherals** - A.K. Ray and K.M. Bhurchandi, TMH, 3rd Edition, 2012, ISBN 978-1-25-900613-5.
Reference Books: 1. **Microprocessor and Interfacing**- Douglas V Hall, SSSP Rao, 3rd edition TMH, 2012. 2. **Microcomputer systems-The 8086 / 8088 Family** – Y.C. Liu and A. Gibson, 2nd edition, PHI -2003. 3. **The 8086 Microprocessor: Programming & Interfacing the PC** – Kenneth J Ayala, CENGAGE Learning, 2011. 4. **The Intel Microprocessor, Architecture, Programming and Interfacing** - Barry B. Brey, 6e, Pearson Education / PHI, 2003.

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