

| DIGITAL ELECTRONICS LAB SEMESTER – III (EC/TC) [As per Choice Based Credit System (CBCS) Scheme] | | | |
|---|---|-------------------|-----------|
| Laboratory Code | 17ECL38 | CIE Marks | 40 |
| Number of Lecture Hours/Week | 01Hr Tutorial (Instructions) + 02 Hours Laboratory | SEE Marks | 60 |
| RBT Level | L1, L2, L3 | Exam Hours | 03 |
| CREDITS – 02 | | | |
| Course objectives: This laboratory course enables students to get practical experience in design, realisation and verification of <ul style="list-style-type: none"> • Demorgan's Theorem, SOP, POS forms • Full/Parallel Adders, Subtractors and Magnitude Comparator • Demultiplexers and Decoders applications • Flip-Flops, Shift registers and Counters | | | |
| NOTE: <ol style="list-style-type: none"> 1. Use discrete components to test and verify the logic gates. The IC umbers given are suggestive. Any equivalent IC can be used. 2. For experiment No. 11 and 12 any open source or licensed simulation tool may be used. | | | |
| Laboratory Experiments: | | | |
| 1. Verify (a) Demorgan's Theorem for 2 variables. (b) The sum-of product and product-of-sum expressions using universal gates. | | | |
| 2. Design and implement (a) Full Adder using (i) basic logic gates and (ii) NAND gates. (b) Full subtractor using (i) basic logic gates and (ii) NANAD gates. | | | |
| 3. Design and implement 4-bit Parallel Adder/ Subtractor using IC 7483. | | | |
| 4. Design and Implementation of 5-bit Magnitude Comparator using IC 7485. | | | |
| 5. Realize (a) Adder & Subtractor using IC 74153. (b) 3-variable function using IC 74151(8:1MUX). | | | |
| 6. Realize a Boolean expression using decoder IC74139. | | | |
| 7. Realize Master-Slave JK, D & T Flip-Flops using NAND Gates. | | | |
| 8. Realize the following shift registers using IC7474/IC 7495 (a) SISO (b) SIPO (c) PISO (d) PIPO (e) Ring and (f) Johnson counter. | | | |
| 9. Realize (i) Mod-N Asynchronous Counter using IC7490 and (ii) Mod-N Synchronous counter using IC74192 | | | |
| 10. Design Pseudo Random Sequence generator using 7495. | | | |

11. Simulate Full- Adder using simulation tool.

12. Simulate Mod-8 Synchronous UP/DOWN Counter using simulation tool.

Course Outcomes: On the completion of this laboratory course, the students will be able to:

- Demonstrate the truth table of various expressions and combinational circuits using logic gates.
- Design and test various combinational circuits such as adders, subtractors, comparators, multiplexers.
- Realize Boolean expression using decoders.
- Construct and test flips-flops, counters and shift registers.
- Simulate full adder and up/down counters.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.



H. O. D.

Dept. Of Electronics & Communication
Alva' - Institute of Engg & Technology
Mijar, MOODBIDRI - 574 225