ADVANCED COMPUTER ARCHITECTURE

B.E., VII Semester, Electronics & Communication Engineering /Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC754	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Course Objectives: This course will enable students to:

- Understand the various parallel computer models and conditions of parallelism
- Explain the control flow, dataflow and demand driven machines
- Study CISC, RISC, superscalar, VLIW and multiprocessor architectures
- Understand the concept of pipelining and memory hierarchy design
- Explain cache coherence protocols.

Module-1	RBT Level
Parallel Computer Models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputer, Multivectors and SIMD computers. **Program and Network Properties:** Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency.	L1, L2
Module-2	
Program flow mechanisms: Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms. **Principles of Scalable Performance**: Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches.	L1, L2, L3
Module-3	
Speedup Performance Laws: Amdhal's law, Gustafson's law, Memory bounded speed up model, Scalability Analysis and Approaches. **Advanced Processors:** Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures.	L1, L2, L3
Module-4	
Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design. **Memory Hierarchy Design:** Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.	L1, L2, L3

Module-5	
Multiprocessor Architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols.	L1, L2, L3

Course Outcomes: At the end of the course, the students will be able to:

- Explain parallel computer models and conditions of parallelism
- Differentiate control flow, dataflow, demand driven mechanisms
- Explain the principle of scalable performance
- Discuss advanced processors architectures like CISC, RISC, superscalar and VLIW
- Understand the basics of instruction pipelining and memory technologies
- Explain the issues in multiprocessor architectures

Question paper pattern:

The question paper will have ten questions.

- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Kai Hwang, "Advanced computer architecture"; TMH.

Reference Books:

1. Kai Hwang and Zu, "Scalable Parallel Computers Architecture"; MGH.
2. M.J Flynn, "Computer Architecture, Pipelined and Parallel Processor Design"; Narosa Publishing.
3. D.A.Patterson, J.L.Hennessy, "Computer Architecture :A quantitative approach"; Morgan Kauffmann Feb, 2002.

D.V.

H.O.D.

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