DIGITAL SYSTEM DESIGN USING VERILOG

B.E., VI Semester (Open Elective)

[As per Choice Based Credit System (CBCS) scheme]

Subject Code:	15EC663	IA Marks: 20
Number of Lecture Hours/Week:	03	Exam Marks: 80
Total Number of Lecture Hours:	40 (08 Hrs per module)	Exam Hours: 03
CREDITS – 03		

Course objectives: Thiscourse will enable students to:

- Understand the concepts of Verilog Language.
- Design the digital systems as an activity in a larger systems design context.
- Study the design and operation of semiconductor memories frequently used in application specific digital system.
- Inspect how effectively IC's are embedded in package and assembled in PCB's for different application.
- Design and diagnosis of processors and I/O controllers used in embedded systems.

Module -1	RBT Level
Introduction and Methodology: Digital Systems and Embedded Systems, Real-World Circuits, Models, Design Methodology (1.1, 1.3 to 1.5 of Text). **Combinational Basics:**Combinational Components and Circuits, Verification of Combinational Circuits.(2.3 and 2.4 of Text) **Sequential Basics**:Sequential Datapaths and ControlClocked Synchronous Timing Methodology (4.3 up to 4.3.1,4.4 up to 4.4.1 of Text).	L1, L2, L3
Module -2	
Memories: Concepts, Memory Types, Error Detection and Correction (Chap 5 of Text).	L1, L2, L3
Module -3	
Implementation Fabrics: Integrated Circuits, Programmable Logic Devices, Packaging and Circuit boards, Interconnection and Signal integrity (Chap 6 of Text).	L1, L2, L3
Module -4	
I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software (Chap 8 of Text).	L1, L2, L3
Module -5	
Design Methodology: Design flow, Design optimization, Design for test, Nontechnical Issues (Chap 10 of Text).	L1, L2, L3, L4

Course outcomes: After studying this course, students will be able to:

- Construct the combinational circuits, using discrete gates and programmable logic devices.
- Describe Verilog model for sequential circuits and test pattern generation.
- Design a semiconductor memory for specific chip design.

- Design embedded systems using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores.
- Synthesize different types of processor and I/O controllers that are used in embedded system.

Question paper pattern:

- The question paper will have ten questions.
- Each full Question consisting of 16 marks. There will be 2 full questions (with a maximum of Three sub questions from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using VERILOG", Elesvier, 2010.

H. O. D.
Dept. Of Electronics & Communication
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225