

DIGITAL ELECTRONICS [As per Choice Based Credit System (CBCS) scheme] SEMESTER – III (EC/TC)			
Subject Code	15EC33	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03
CREDITS – 04			
Course objectives: This course will enable students to: <ul style="list-style-type: none"> • Illustrate simplification of Algebraic equations using Karnaugh Maps and Quine-McClusky Techniques. • Design combinational logic circuits. • Design Decoders, Encoders, Digital Multiplexer, Adders, Subtractors and Binary Comparators. • Describe Latches and Flip-flops, Registers and Counters. • Analyze Mealy and Moore Models. • Develop state diagrams Synchronous Sequential Circuits. 			
Modules			RBT Level
Module – 1			
Principles of combination logic: Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don't care terms) Simplifying Max term equations, Quine-McCluskey minimization technique, Quine-McCluskey using don't care terms, Reduced prime implicants Tables.(Text 1, Chapter 3)			L1, L2, L3
Module -2			
Analysis and design of combinational logic: General approach to combinational logic design, Decoders, BCD decoders, Encoders, digital multiplexers, Using multiplexers as Boolean function generators, Adders and subtractors, Cascading full adders, Look ahead carry, Binary comparators.(Text 1, Chapter 4)			L1, L2, L3
Module -3			
Flip-Flops: Basic Bistable elements, Latches, Timing considerations, The master-slave flip-flops (pulse-triggered flip-flops): SR flip-flops, JK flip-flops, Edge triggered flip-flops, Characteristic equations. (Text 2, Chapter 6)			L1,L2
Module -4			
Simple Flip-Flops Applications: Registers, binary ripple counters, synchronous binary counters, Counters based on shift registers, Design of a synchronous counters, Design of a synchronous mod-n counter using clocked T , JK , D and SR flip-flops. (Text 2, Chapter 6)			L1,L2, L3

Module -5	
Sequential Circuit Design: Mealy and Moore models, State machine notation, Synchronous Sequential circuit analysis, Construction of state diagrams, counter design. (Text 1, Chapter 6)	L1, L2, L3
<p>Course Outcomes: After studying this course, students will be able to:</p> <ul style="list-style-type: none"> • Develop simplified switching equation using Karnaugh Maps and Quine-McClusky techniques. • Explain the operation of decoders, encoders, multiplexers, demultiplexers, adders, subtractors and comparators. • Explain the working of Latches and Flip Flops (SR,D,T and JK). • Design Synchronous/Asynchronous Counters and Shift registers using Flip Flops. • Develop Mealy/Moore Models and state diagrams for the given clocked sequential circuits. • Apply the knowledge gained in the design of Counters and Registers. 	
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have ten questions. • Each full question consists of 16 marks. • There will be 2 full questions (with a maximum of Three sub questions) from each module. • Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module. 	
<p>Text Books:</p> <ol style="list-style-type: none"> 1. Digital Logic Applications and Design, John M Yarbrough, Thomson Learning, 2001. ISBN 981-240-062-1. 2. Donald D. Givone, "Digital Principles and Design", McGraw Hill, 2002. ISBN 978-0-07-052906-9. 	
<p>Reference Books:</p> <ol style="list-style-type: none"> 1. D. P. Kothari and J. S Dhillon, "Digital Circuits and Design", Pearson, 2016, ISBN:9789332543539. 2. Morris Mano, "Digital Design", Prentice Hall of India, Third Edition. 3. Charles H Roth, Jr., "Fundamentals of logic design", Cengage Learning. 4. K. A. Navas, "Electronics Lab Manual", Volume I, PHI, 5th Edition, 2015, ISBN: 9788120351424. 	



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