FUNDAMENTALS OF CMOS VLSI

Subject Code	: **10EC56**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

BASIC MOS TECHNOLOGY: Integrated circuit's era. Enhancement and depletion mode MOS transistors. nMOS fabrication. CMOS fabrication. Thermal aspects of processing. BiCMOS technology. Production of E-beam masks.

MOS TRANSISTOR THEORY: Introduction, MOS Device Design Equations, The Complementary CMOS Inverter – DC Characteristics, Static Load MOS Inverters, The Differential Inverter, The Transmission Gate, Tristate Inverter.

UNIT - 2

CIRCUIT DESIGN PROCESSES: MOS layers. Stick diagrams. Design rules and layout – lambda-based design and other rules. Examples. Layout diagrams. Symbolic diagrams. Tutorial exercises.

Basic Physical Design of Simple logic gates.

UNIT - 3

CMOS LOGIC STRUCTURES: CMOS Complementary Logic, Bi CMOS Logic, Pseudo-nMOS Logic, Dynamic CMOS Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS Domino Logic Cascaded Voltage Switch Logic (CVSL).

UNIT - 4

BASIC CIRCUIT CONCEPTS: Sheet resistance. Area capacitances. Capacitance calculations. The delay unit. Inverter delays. Driving capacitive loads. Propagation delays. Wiring capacitances.

SCALING OF MOS CIRCUITS: Scaling models and factors. Limits on scaling. Limits due to current density and noise.

UNIT - 5

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CMOS SUBSYSTEM DESIGN: Architectural issues. Switch logic. Gate logic. Design examples – combinational logic. Clocked circuits. Other system considerations.

Clocking Strategies

UNIT - 6

CMOS SUBSYSTEM DESIGN PROCESSES: General considerations. Process illustration. ALU subsystem. Adders. Multipliers.

UNIT - 7

MEMORY, REGISTERS AND CLOCK: Timing considerations. Memory elements. Memory cell arrays.

UNIT - 8

TESTABILITY: Performance parameters. Layout issues. I/O pads. Real estate. System delays. Ground rules for design. Test and testability.

TEXT BOOKS:

1. **CMOS VLSI Design – A Circuits and Systems Perspective. 3rd Edition. N.H. Weste and David Harris. Addison-Wesley, 2005.** (Refer to http://www.cmosvlsi.com)
2. **Principles of CMOS VLSI Design: A Systems Perspective,** Neil H. E. Weste, K. Eshragian, and ??? 3rd edition, Pearson Education (Asia) Pvt. Ltd., 200?. (Shift to the latest edition.)
3. **Basic VLSI Design** - Douglas A. Pucknell & Kamran Eshraghian, PHI 3rd Edition (original Edition – 1994), 2005.

REFERENCE BOOKS:

1. R. Jacob Baker. CMOS Circuit Design, Layout and Simulation. John Wiley India Pvt. Ltd, 2008
2. **Fundamentals of Semiconductor Devices,** M. K. Achuthan and K. N. Bhat, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2007.
3. **CMOS Digital Integrated Circuits: Analysis and Design,** Sung-Mo Kang & Yusuf Leblebici, 3rd Edition, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007.
4. **Analysis and Design of Digital Integrated Circuits** - D.A Hodges, H.G Jackson and R.A Saleh. 3rd Edition, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2007.

DIGITAL SIGNAL PROCESSING LABORATORY

Subject Code	: **10ECL57**	IA Marks	: 25
No. of Practical Hrs/Week: 03		Exam Hours	: 03
Total no. of Practical Hrs.	: 42	Exam Marks	: 50

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