Design Process, Identifying the Requirements, Formulating the Requirements Specification, The System Design Specification, System Specifications versus System Requirements, Partitioning and Decomposing a System, Functional Design, Architectural Design, Functional Model versus Architectural Model, Prototyping, Other Considerations, Archiving the Project.

UNIT 5 & 6:

Real-Time Kernels and Operating Systems: Tasks and Things, Programs and Processes, The CPU is a resource, Threads – Lightweight and heavyweight, Sharing Resources, Foreground/Background Systems, The operating System, The real time operating system (RTOS), OS architecture, Tasks and Task control blocks, memory management revisited

UNIT 7 & 8:

Performance Analysis and Optimization: Performance or Efficiency Measures, Complexity Analysis, The methodology, Analyzing code, Instructions in Detail, Time, etc. – A more detailed look, Response Time, Time Loading, Memory Loading, Evaluating Performance, Thoughts on Performance Optimization, Performance Optimization, Tricks of the Trade, Hardware Accelerators, Caches and Performance

Text Book:

1. **Embedded Systems – A contemporary Design Tool,** James K. Peckol, John Weily India Pvt. Ltd, 2008

Reference Books:

1. **Embedded Systems: Architecture and Programming,** Raj Kamal, TMH. 2008
2. **Embedded Systems Architecture – A Comprehensive Guide for Engineers and Programmers,** Tammy Noergaard, Elsevier Publication, 2005
3. **Programming for Embedded Systems,** Dreamtech Software Team, John Wiley India Pvt. Ltd, 2008

VLSI LAB

Subject Code	: **10ECL77**	IA Marks	: 25
No. of Practical Hrs/Week	: 03	Exam Hours	: 03
Total no. of Practical Hrs.	: 42	Exam Marks	: 50

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(Wherever necessary Cadence/Synopsis/Mentz Graphics tools must be used)

PART - A

DIGITAL DESIGN

ASIC-DIGITAL DESIGN FLOW

1. Write Verilog Code for the following circuits and their Test Bench for **verification**, observe the waveform and **synthesize** the code with technological library with given Constraints*. Do the initial timing verification with gate level simulation.

i. An inverter
ii. A Buffer
iii. Transmission Gate
iv. Basic/universal gates
v. Flip flop -RS, D, JK, MS, T
vi. Serial & Parallel adder
vii. 4-bit counter [Synchronous and Asynchronous counter]
viii. Successive approximation register [SAR]

* *An appropriate constraint should be given*

PART - B
ANALOG DESIGN

Analog Design Flow

1. Design an **Inverter** with given specifications*, completing the design flow mentioned below:

a. **Draw the schematic** and verify the following
   i) DC Analysis
   ii) Transient Analysis
b. **Draw the Layout** and verify the DRC, ERC
c. Check for LVS
d. Extract RC and back annotate the same and verify the Design
e. Verify & Optimize for Time, Power and Area to the given constraint***

2. Design the following circuits with given specifications*, completing the design flow mentioned below:

a. Draw the schematic and verify the following
   i) DC Analysis
   ii) AC Analysis

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iii) Transient Analysis

b. Draw the Layout and verify the DRC, ERC

c. Check for LVS

d. Extract RC and back annotate the same and verify the Design.

i) A Single Stage differential amplifier

ii) Common source and Common Drain amplifier

3. Design an **op-amp** with given specification* using given differential amplifier Common source and Common Drain amplifier in library** and completing the design flow mentioned below:

a. Draw the schematic and verify the following

i) DC Analysis

ii). AC Analysis

iii) Transient Analysis

b. Draw the Layout and verify the DRC, ERC

c. Check for LVS

d. Extract RC and back annotate the same and verify the Design.

4. Design a **4 bit R-2R based DAC** for the given specification and completing the design flow mentioned using given op-amp in the library**.

a. Draw the schematic and verify the following

i) DC Analysis

ii) AC Analysis

iii) Transient Analysis

b. Draw the Layout and verify the DRC, ERC

c. Check for LVS

d. Extract RC and back annotate the same and verify the Design.

5. For the **SAR based ADC** mentioned in the figure below draw the mixed signal schematic and verify the functionality by completing ASIC Design FLOW.

[Specifications to GDS-II]

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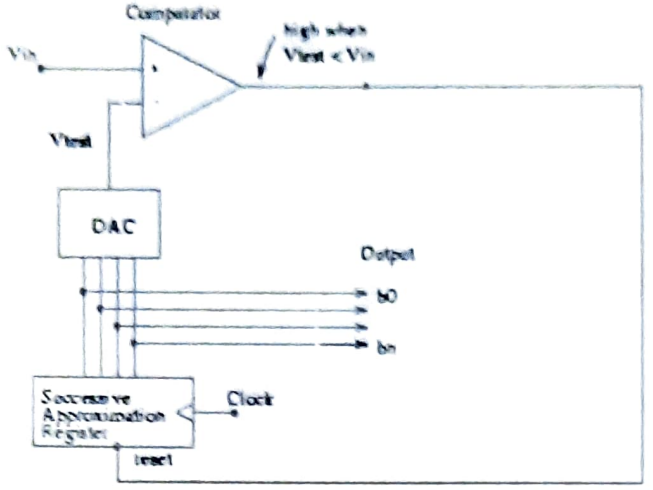

* Appropriate specification should be given.
** Applicable Library should be added & information should be given to the Designer.
*** An appropriate constraint should be given

POWER ELECTRONICS LAB

Subject Code	: **10ECL78**	IA Marks	: 25
No. of Practical Hrs/Week: 03		Exam Hours	: 03
Total no. of Practical Hrs. : 42		Exam Marks	: 50

Any five converter circuits experiment from the below list **must be** simulated using the **spice-simulator**.

1. Static characteristics of SCR and DIAC.
2. Static characteristics of MOSFET and IGBT.
3. Controlled HWR and FWR using RC triggering circuit
4. SCR turn off using i) LC circuit ii) Auxiliary Commutation
5. UJT firing circuit for HWR and FWR circuits.
6. Generation of firing signals for thyristors/ trials using digital circuits / microprocessor.
7. AC voltage controller using triac – diac combination.
8. Single phase Fully Controlled Bridge Converter with R and R-L loads.
9. Voltage (Impulse) commutated chopper both constant frequency and variable frequency operations.
10. Speed control of a separately exited DC motor.
11. Speed control of universal motor.

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