ARTIFICIAL NEURAL NETWORKS

Subject Code	: **10EC753**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

Introduction, history, structure and function of single neuron, neural net architectures, neural learning, use of neural networks.

UNIT - 2

Supervised learning, single layer networks, perceptions, linear separability, perceptions training algorithm, guarantees of success, modifications.

UNIT - 3

Multiclass networks-I, multilevel discrimination, preliminaries, back propagation, setting parameter values, theoretical results.

UNIT - 4

Accelerating learning process, application, mandaline, adaptive multilayer networks.

UNIT - 5

Prediction networks, radial basis functions, polynomial networks, regularization, unsupervised learning, winner take all networks.

UNIT - 6

Learning vector quantizing, counter propagation networks, adaptive resonance theorem, toplogically organized networks, distance based learning, neo-cognition.

UNIT - 7

Associative models, hop field networks, brain state networks, Boltzmann machines, hetero associations.

UNIT - 8

Optimization using hop filed networks, simulated annealing, random search, evolutionary computation.

D.V.

H.O.D.

Dept. Of Electronics & Communication

Sahyadri Institute of Engg. & Technology

TEXT BOOK:

1. **Elements of Artificial Neural Networks**, Kishan Mehrotra, C. K. Mohan, Sanjay Ranka, Penram, 1997.

REFERENCE BOOKS:

1. **Artificial Neural Networks**, R. Schalkoff, MGH, 1997.
2. **Introduction to Artificial Neural Systems**, J. Zurada, Jaico, 2003.
3. **Neural Networks,** Haykins, Pearson Edu., 1999.

CAD FOR VLSI

Subject Code	: **10EC754**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
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UNIT – 1&2

INTRODUCTION TO VLSI METHODOLOGIES: VLSI Physical Design Automation - Design and Fabrication of VLSI Devices - Fabrication process and its impact on Physical Design.

UNIT – 3&4

A QUICK TOUR OF VLSI DESIGN AUTOMATION TOOLS: Data structures and Basic Algorithms, Algorithmic Graph theory and computational complexity, Tractable and Intractable problems.

UNIT – 5&6

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: partitioning, floor planning and pin assignment, placement, routing.

UNIT – 7&8

SIMULATION-LOGIC SYNTHESIS: Verification-High level synthesis - Compaction. Physical Design Automation of FPGAs, MCMS-VHDL-Verilog-Implementation of Simple circuits using VHDL and Verilog.