REFERENCE BOOKS:

1. **Object Oriented Programming in C++** - Balaguruswamy. TMH, 1995.
2. **Programming in C++** - Balaguruswamy. TMH, 4th, 2010 .

DIGITAL SYSTEMS DESIGN USING VHDL

Subject Code	: **10EC666**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

INTRODUCTION: VHDL description of combinational networks, Modeling flip-flops using VHDL, VHDL models for a multiplexer, Compilation and simulation of VHDL code, Modeling a sequential machine, Variables, Signals and constants, Arrays, VHDL operators, VHDL functions, VHDL procedures, Packages and libraries, VHDL model for a counter.

UNIT - 2

DESIGNING WITH PROGRAMMABLE LOGIC DEVICES: Read-only memories, Programmable logic arrays (PLAs), Programmable array logic (PLAs), Other sequential programmable logic devices (PLDs), Design of a keypad scanner.

UNIT - 3

DESIGN OF NETWORKS FOR ARITHMETIC OPERATIONS: Design of a serial adder with accumulator, State graphs for control networks, Design of a binary multiplier, Multiplication of signed binary numbers, Design of a binary divider.

UNIT - 4

DIGITAL DESIGN WITH SM CHARTS: State machine charts, Derivation of SM charts, Realization of SM charts. Implementation of the dice game, Alternative realization for SM charts using microprogramming, Linked state machines.

UNIT - 5

DESIGNING WITH PROGRAMMABLE GATE ARRAYS AND COMPLEX PROGRAMMABLE LOGIC DEVICES: Xlinx 3000 series FPGAs, Designing with FPGAs, Xlinx 4000 series FPGAs, using a one-hot state assignment, Altera complex programmable logic devices (CPLDs), Altera FELX 10K series COLDs.

D.V.

H. O. D.
Dept. Of Electronics & Communication
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

UNIT - 6

FLOATING - POINT ARITHMETIC: Representation of floating-point numbers, Floating-point multiplication, Other floating-point operations.

UNIT - 7

ADDITIONAL TOPICS IN VHDL: Attributes, Transport and Inertial delays, Operator overloading, Multi-valued logic and signal resolution, IEEE-1164 standard logic, Generics, Generate statements, Synthesis of VHDL code, Synthesis examples, Files and Text IO.

UNIT - 8

VHDL MODELS FOR MEMORIES AND BUSES: Static RAM, A simplified 486 bus model, Interfacing memory to a microprocessor bus.

TEXT BOOK:

1. **Digital Systems Design using VHDL**, Charles H. Roth. Jr:, Thomson Learning, Inc, 9th reprint, 2006.

REFERENCE BOOKS:

1. **Fundamentals of Digital Logic Design with VHDL**, Stephen Brwon & Zvonko Vranesic, Tata McGrw-Hill, New Delhi, 2nd Ed., 2007
2. **Digital System Design with VHDL**, Mark Zwolinski, 2 Ed, Pearson Education., 2004
3. **Digital Electronics and Design with VHDL -** Volnei A Pedroni, Elsivier Science, 2009.

VIRTUAL INSTRUMENTATION

Subject Code	: **10EC668**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT 1

Review of Digital Instrumentation: Representation of analog signals in the digital domain – Review of quantization in amplifier and time areas, sample and hold, sampling theorem, ADC and DAC.

UNIT 2

Fundamentals of Virtual Instrumentation: Concept of Virtual Instrumentation – PC based data acquisition – Typical on board DAQ card –

D.V.

H.O.D.

Dept. Of Electronics & Communication
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI-574 225