Oscillators: Oscillator operation, Phase shift Oscillator, Wienbridge Oscillator, Tuned Oscillator circuits, Crystal Oscillator. (BJT Version Only) Simple design methods of Oscillators.

UNIT 8:

FET Amplifiers: FET small signal model, Biasing of FET, Common drain common gate configurations, MOSFETs, FET amplifier networks.

TEXT BOOK:

1. **"Electronic Devices and Circuit Theory",** Robert L. Boylestad and Louis Nashelsky, PHI/Pearson Eduication. 9TH Edition.

REFERENCE BOOKS:

1. **'Integrated Electronics',** Jacob Millman & Christos C. Halkias, Tata - McGraw Hill, 2nd Edition, 2010
2. **"Electronic Devices and Circuits",** David A. Bell, PHI, 4th Edition, 2004
3. **"Analog Electronics Circuits: A Simplified Approach",** U.B. Mahadevaswamy, Pearson/Saguine, 2007.

LOGIC DESIGN
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	**:**	**10ES33**	**IA Marks**	**:**	**25**
Hrs/ Week	**:**	**04**	**Exam Hours**	**:**	**03**
Total Hrs.	**:**	**52**	**Exam Marks**	**:**	**100**

UNIT 1:

Principles of combinational logic-1: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3, 4 and 5 variables, Incompletely specified functions (Don't Care terms), Simplifying Max term equations.

UNIT 2:

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Principles of combinational Logic-2: Quine-McCluskey minimization technique- Quine-McCluskey using don't care terms, Reduced Prime Implicant Tables, Map entered variables.

UNIT 3:

Analysis and design of combinational logic - I: General approach, Decoders-BCD decoders, Encoders.

UNIT 4:

Analysis and design of combinational logic - II: Digital multiplexers-Using multiplexers as Boolean function generators. Adders and subtractors-Cascading full adders, Look ahead carry, Binary comparators. Design methods of building blocks of combinational logics.

UNIT 5:

Sequential Circuits – 1: Basic Bistable Element, Latches, SR Latch, Application of SR Latch, A Switch Debouncer, The $\overline{S}\overline{R}$ Latch, The gated SR Latch, The gated D Latch, The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The Master-Slave SR Flip-Flops, The Master-Slave JK Flip-Flop. Edge Triggered Flip-Flop: The Positive Edge-Triggered D Flip-Flop, Negative-Edge Triggered D Flip-Flop.

UNIT 6:

Sequential Circuits – 2: Characteristic Equations, Registers, Counters - Binary Ripple Counters, Synchronous Binary counters, Counters based on Shift Registers, Design of a Synchronous counters, Design of a Synchronous Mod-6 Counter using clocked JK Flip-Flops Design of a Synchronous Mod-6 Counter using clocked D, T, or SR Flip-Flops

UNIT 7:

Sequential Design - I: Introduction, Mealy and Moore Models, State Machine Notation, Synchronous Sequential Circuit Analysis and Design.

UNIT 8:

Sequential Design - II: Construction of state Diagrams, Counter Design.

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TEXT BOOKS:

1. **"Digital Logic Applications and Design"**, John M Yarbrough, Thomson Learning, 2001.
2. **"Digital Principles and Design "**, Donald D Givone, Tata McGraw Hill Edition, 2002.

REFERENCE BOOKS:

1. **"Fundamentals of logic design"**, Charles H Roth, Jr; Thomson Learning, 2004.
2. **"Logic and computer design Fundamentals"**, Mono and Kim, Pearson, Second edition, 2001.
3. **"Logic Design"**, Sudhakar Samuel, Pearson/Saguine, 2007

NETWORK ANALYSIS
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	**:**	**10ES34**	**IA Marks**	**:**	**25**
Hrs/ Week	**:**	**04**	**Exam Hours**	**:**	**03**
Total Hrs.	**:**	**52**	**Exam Marks**	**:**	**100**

UNIT 1:

Basic Concepts: Practical sources, Source transformations, Network reduction using Star – Delta transformation, Loop and node analysis With linearly dependent and independent sources for DC and AC networks, Concepts of super node and super mesh.

UNIT 2:

Network Topology: Graph of a network, Concept of tree and co-tree, incidence matrix, tie-set, tie-set and cut-set schedules, Formulation of equilibrium equations in matrix form, Solution of resistive networks, Principle of duality.

UNIT 3:

Network Theorems – 1: Superposition, Reciprocity and Millman's theorems.

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