ANALOG ELECTRONICS LAB
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	:	**10ESL37**	**IA Marks**	:	**25**
Hrs/ Week	:	**03**	**Exam Hours**	:	**03**
Total Hrs.	:		**Exam Marks**	:	**50**

NOTE: Use the Discrete components to test the circuits. LabView can be used for the verification and testing along with the above.

1. Wiring of RC coupled Single stage FET & BJT amplifier and determination of the gain-frequency response, input and output impedances.

2. Wiring of BJT Darlington Emitter follower with and without bootstrapping and determination of the gain, input and output impedances (Single circuit) (One Experiment)

3. Wiring of a two stage BJT Voltage series feed back amplifier and determination of the gain, Frequency response, input and output impedances with and without feedback (One Experiment)

4. Wiring and Testing for the performance of BJT-RC Phase shift Oscillator for $f_0 \leq 10$ KHz

5. Testing for the performance of BJT – Hartley & Colpitts Oscillators for RF range $f_0 \geq 100$KHz.

6. Testing for the performance of BJT -Crystal Oscillator for $f_0 > 100$ KHz
7 Testing of Diode clipping (Single/Double ended) circuits for peak clipping, peak detection

8. Testing of Clamping circuits: positive clamping /negative clamping.
9. Testing of a transformer less Class – B push pull power amplifier and determination of its conversion efficiency.

10. Testing of Half wave, Full wave and Bridge Rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency

H. O. D.
Dept. Of Electronics & Communication
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

11. Verification of Thevinin's Theorem and Maximum Power Transfer theorem for DC Circuits.

12. Characteristics of Series and Parallel resonant circuits.

LOGIC DESIGN LAB
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	:	**10ESL38**	**IA Marks**	:	**25**
Hrs/ Week	:	**03**	**Exam Hours**	:	**03**
Total Hrs.	:		**Exam Marks**	:	**50**

NOTE: Use discrete components to test and verify the logic gates. LabView can be used for designing the gates along with the above.

1. Simplification, realization of Boolean expressions using logic gates/Universal gates.
2. Realization of Half/Full adder and Half/Full Subtractors using logic gates.
3. (i) Realization of parallel adder/Subtractors using 7483 chip
   (ii) BCD to Excess-3 code conversion and vice versa.
4. Realization of Binary to Gray code conversion and vice versa
5. MUX/DEMUX – use of 74153, 74139 for arithmetic circuits and code converter.
6. Realization of One/Two bit comparator and study of 7485 magnitude comparator.
7. Use of a) Decoder chip to drive LED display and b) Priority encoder.
8. Truth table verification of Flip-Flops: (i) JK Master slave (ii) T type and (iii) D type.
9. Realization of 3 bit counters as a sequential circuit and MOD – N counter design (7476, 7490, 74192, 74193).
10. Shift left; Shift right, SIPO, SISO, PISO, PIPO operations using 74S95.
11. Wiring and testing Ring counter/Johnson counter.
12. Wiring and testing of Sequence generator.

H. O. D.
Dept. Of Electronics & Communication
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225