iterative method. Definition of eigen values and eigen vectors of a square matrix. Computation of largest eigen value and the corresponding eigen vector by Rayleigh's power method.

UNIT 6:

Finite differences (Forward and Backward differences) Interpolation, Newton's forward and backward interpolation formulae. Divided differences – Newton's divided difference formula. Lagrange's interpolation and inverse interpolation formulae. Numerical differentiation using Newton's forward and backward interpolation formulae. Numerical Integration – Simpson's one third and three eighth's value, Weddle's rule.
(All formulae / rules without proof).

UNIT 7:

Calculus of Variations

Variation of a function and a functional Extremal of a functional, Variational problems, Euler's equation, Standard variational problems including geodesics, minimal surface of revolution, hanging chain and Brachistochrone problems.

UNIT 8:

Difference Equations and Z-transforms

Difference equations – Basic definitions. Z-transforms – Definition, Standard Z-transforms, Linearity property, Damping rule, Shifting rule, Initial value theorem, Final value theorem, Inverse Z-transforms. Application of Z-transforms to solve difference equations.

Reference Books:

1. **Higher Engineering Mathematics** by B.V. Ramana (Tata-Macgraw Hill).
2. **Advanced Modern Engineering Mathematics** by Glyn James – Pearson Education.

ANALOG ELECTRONIC CIRCUITS
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	:	**10ES32**	**IA Marks**	:	**25**
Hrs/ Week	:	**04**	**Exam Hours**	:	**03**
Total Hrs.	:	**52**	**Exam Marks**	:	**100**

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UNIT 1:

Diode Circuits: Diode Resistance, Diode equivalent circuits, Transition and diffusion capacitance, Reverse recovery time, Load line analysis, Rectifiers, Clippers and clampers.

UNIT 2:

Transistor Biasing: Operating point, Fixed bias circuits, Emitter stabilized biased circuits, Voltage divider biased, DC bias with voltage feedback, Miscellaneous bias configurations, Design operations, Transistor switching networks, PNP transistors, Bias stabilization.

UNIT 3:

Transistor at Low Frequencies: BJT transistor modeling, CE Fixed bias configuration, Voltage divider bias, Emitter follower, CB configuration, Collector feedback configuration, Analysis of circuits r_e model; analysis of CE configuration using h- parameter model; Relationship between h-parameter model of CE,CC and CE configuration.

UNIT 4:

Transistor Frequency Response: General frequency considerations, low frequency response, Miller effect capacitance, High frequency response, multistage frequency effects.

UNIT 5:

(a) General Amplifiers: Cascade connections, Cascode connections, Darlington connections.

(b) Feedback Amplifier: Feedback concept, Feedback connections type, Practical feedback circuits. Design procedures for the feedback amplifiers.

UNIT 6:

Power Amplifiers: Definitions and amplifier types, series fed class A amplifier, Transformer coupled Class A amplifiers, Class B amplifier operations, Class B amplifier circuits, Amplifier distortions. Designing of Power amplifiers.

UNIT 7:

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Oscillators: Oscillator operation, Phase shift Oscillator, Wienbridge Oscillator, Tuned Oscillator circuits, Crystal Oscillator. (BJT Version Only) Simple design methods of Oscillators.

UNIT 8:

FET Amplifiers: FET small signal model, Biasing of FET, Common drain common gate configurations, MOSFETs, FET amplifier networks.

TEXT BOOK:

1. **"Electronic Devices and Circuit Theory",** Robert L. Boylestad and Louis Nashelsky, PHI/Pearson Eduication. 9TH Edition.

REFERENCE BOOKS:

1. **'Integrated Electronics',** Jacob Millman & Christos C. Halkias, Tata - McGraw Hill, 2nd Edition, 2010
2. **"Electronic Devices and Circuits",** David A. Bell, PHI, 4th Edition, 2004
3. **"Analog Electronics Circuits: A Simplified Approach",** U.B. Mahadevaswamy, Pearson/Saguine, 2007.

LOGIC DESIGN
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	**:**	**10ES33**	**IA Marks**	**:**	**25**
Hrs/ Week	**:**	**04**	**Exam Hours**	**:**	**03**
Total Hrs.	**:**	**52**	**Exam Marks**	**:**	**100**

UNIT 1:

Principles of combinational logic-1: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3, 4 and 5 variables, Incompletely specified functions (Don't Care terms), Simplifying Max term equations.

UNIT 2:

D.V-T

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