## ENGINEERING MATHEMATICS – III

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | : | **10MAT31** | **IA Marks** | : | **25** |
| **Hrs/ Week** | : | **04** | **Exam Hours** | : | **03** |
| **Total Hrs.** | : | **52** | **Exam Marks** | : | **100** |

**UNIT 1:**

**Fourier Series**

Periodic functions, Fourier expansions, Half range expansions, Complex form of Fourier series, Practical harmonic analysis.

**UNIT 2:**

**Fourier Transforms**

Finite and Infinite Fourier transforms, Fourier sine and consine transforms, properties. Inverse transforms.

**UNIT 3:**

**Partial Differential Equations (P.D.E)**

Formation of P.D.E Solution of non homogeneous P.D.E by direct integration, Solution of homogeneous P.D.E involving derivative with respect to one independent variable only (Both types with given set of conditions) Method of separation of variables. (First and second order equations) Solution of Lagrange's linear P.D.E. of the type $P\,p + Q\,q = R$.

**UNIT 4:**

**Applications of P.D.E**

Derivation of one dimensional wave and heat equations. Various possible solutions of these by the method of separation of variables. D'Alembert's solution of wave equation. Two dimensional Laplace's equation – various possible solutions. Solution of all these equations with specified boundary conditions. (Boundary value problems).

**UNIT 5:**

**Numerical Methods**

Introduction, Numerical solutions of algebraic and transcendental equations:- Newton-Raphson and Regula-Falsi methods. Solution of linear simultaneous equations : - Gauss elimination and Gauss Jordon methods. Gauss - Seidel



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iterative method. Definition of eigen values and eigen vectors of a square matrix. Computation of largest eigen value and the corresponding eigen vector by Rayleigh's power method.

**UNIT 6:**

Finite differences (Forward and Backward differences) Interpolation, Newton's forward and backward interpolation formulae. Divided differences – Newton's divided difference formula. Lagrange's interpolation and inverse interpolation formulae. Numerical differentiation using Newton's forward and backward interpolation formulae. Numerical Integration – Simpson's one third and three eighth's value, Weddle's rule.
(All formulae / rules without proof).

**UNIT 7:**

**Calculus of Variations**

Variation of a function and a functional Extremal of a functional, Variational problems, Euler's equation, Standard variational problems including geodesics, minimal surface of revolution, hanging chain and Brachistochrone problems.

**UNIT 8:**

**Difference Equations and Z-transforms**

Difference equations – Basic definitions. Z-transforms – Definition, Standard Z-transforms, Linearity property, Damping rule, Shifting rule, Initial value theorem, Final value theorem, Inverse Z-transforms. Application of Z-transforms to solve difference equations.

**Reference Books:**


1. **Higher Engineering Mathematics** by B.V. Ramana (Tata-Macgraw Hill).
2. **Advanced Modern Engineering Mathematics** by Glyn James – Pearson Education.


## ANALOG ELECTRONIC CIRCUITS
## (Common to EC/TC/EE/IT/BM/ML)

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | : | **10ES32** | **IA Marks** | : | **25** |
| **Hrs/ Week** | : | **04** | **Exam Hours** | : | **03** |
| **Total Hrs.** | : | **52** | **Exam Marks** | : | **100** |



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iterative method. Definition of eigen values and eigen vectors of a square matrix. Computation of largest eigen value and the corresponding eigen vector by Rayleigh's power method.

**UNIT 6:**

Finite differences (Forward and Backward differences) Interpolation, Newton's forward and backward interpolation formulae. Divided differences – Newton's divided difference formula. Lagrange's interpolation and inverse interpolation formulae. Numerical differentiation using Newton's forward and backward interpolation formulae. Numerical Integration – Simpson's one third and three eighth's value, Weddle's rule.
(All formulae / rules without proof).

**UNIT 7:**

**Calculus of Variations**

Variation of a function and a functional Extremal of a functional, Variational problems, Euler's equation, Standard variational problems including geodesics, minimal surface of revolution, hanging chain and Brachistochrone problems.

**UNIT 8:**

**Difference Equations and Z-transforms**

Difference equations – Basic definitions. Z-transforms – Definition, Standard Z-transforms, Linearity property, Damping rule, Shifting rule, Initial value theorem, Final value theorem, Inverse Z-transforms. Application of Z-transforms to solve difference equations.

**Reference Books:**


1. **Higher Engineering Mathematics** by B.V. Ramana (Tata-Macgraw Hill).
2. **Advanced Modern Engineering Mathematics** by Glyn James – Pearson Education.


## ANALOG ELECTRONIC CIRCUITS
## (Common to EC/TC/EE/IT/BM/ML)

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | : | **10ES32** | **IA Marks** | : | **25** |
| **Hrs/ Week** | : | **04** | **Exam Hours** | : | **03** |
| **Total Hrs.** | : | **52** | **Exam Marks** | : | **100** |



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**UNIT 1:**

**Diode Circuits:** Diode Resistance, Diode equivalent circuits, Transition and diffusion capacitance, Reverse recovery time, Load line analysis, Rectifiers, Clippers and clampers.

**UNIT 2:**

**Transistor Biasing**: Operating point, Fixed bias circuits, Emitter stabilized biased circuits, Voltage divider biased, DC bias with voltage feedback, Miscellaneous bias configurations, Design operations, Transistor switching networks, PNP transistors, Bias stabilization.

**UNIT 3:**

**Transistor at Low Frequencies:** BJT transistor modeling, CE Fixed bias configuration, Voltage divider bias, Emitter follower, CB configuration, Collector feedback configuration, Analysis of circuits $r_e$ model; analysis of CE configuration using h- parameter model; Relationship between h-parameter model of CE,CC and CE configuration.

**UNIT 4:**

**Transistor Frequency Response**: General frequency considerations, low frequency response, Miller effect capacitance, High frequency response, multistage frequency effects.

**UNIT 5:**

**(a) General Amplifiers**: Cascade connections, Cascode connections, Darlington connections.

**(b) Feedback Amplifier:** Feedback concept, Feedback connections type, Practical feedback circuits. Design procedures for the feedback amplifiers.

**UNIT 6:**

**Power Amplifiers**: Definitions and amplifier types, series fed class A amplifier, Transformer coupled Class A amplifiers, Class B amplifier operations, Class B amplifier circuits, Amplifier distortions. Designing of Power amplifiers.

**UNIT 7:**



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**Oscillators:** Oscillator operation, Phase shift Oscillator, Wienbridge Oscillator, Tuned Oscillator circuits, Crystal Oscillator. (BJT Version Only) Simple design methods of Oscillators.

**UNIT 8:**

**FET Amplifiers:** FET small signal model, Biasing of FET, Common drain common gate configurations, MOSFETs, FET amplifier networks.

**TEXT BOOK:**

1. **"Electronic Devices and Circuit Theory",** Robert L. Boylestad and Louis Nashelsky, PHI/Pearson Eduication. 9TH Edition.

**REFERENCE BOOKS:**

1. **'Integrated Electronics',** Jacob Millman & Christos C. Halkias, Tata - McGraw Hill, 2nd Edition, 2010
2. **"Electronic Devices and Circuits",** David A. Bell, PHI, 4th Edition, 2004
3. **"Analog Electronics Circuits: A Simplified Approach",** U.B. Mahadevaswamy, Pearson/Saguine, 2007.

## LOGIC DESIGN
## (Common to EC/TC/EE/IT/BM/ML)

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | **:** | **10ES33** | **IA Marks** | **:** | **25** |
| **Hrs/ Week** | **:** | **04** | **Exam Hours** | **:** | **03** |
| **Total Hrs.** | **:** | **52** | **Exam Marks** | **:** | **100** |

**UNIT 1:**

**Principles of combinational logic-1:** Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3, 4 and 5 variables, Incompletely specified functions (Don't Care terms), Simplifying Max term equations.

**UNIT 2:**



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## ANALOG ELECTRONICS LAB
## (Common to EC/TC/EE/IT/BM/ML)

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | : | **10ESL37** | **IA Marks** | : | **25** |
| **Hrs/ Week** | : | **03** | **Exam Hours** | : | **03** |
| **Total Hrs.** | : | | **Exam Marks** | : | **50** |

**NOTE:** Use the Discrete components to test the circuits. LabView can be used for the verification and testing along with the above.

1. Wiring of RC coupled Single stage FET & BJT amplifier and determination of the gain-frequency response, input and output impedances.

2. Wiring of BJT Darlington Emitter follower with and without bootstrapping and determination of the gain, input and output impedances (Single circuit) (One Experiment)

3. Wiring of a two stage BJT Voltage series feed back amplifier and determination of the gain, Frequency response, input and output impedances with and without feedback (One Experiment)

4. Wiring and Testing for the performance of BJT-RC Phase shift Oscillator for $f_0 \leq 10$ KHz

5. Testing for the performance of BJT – Hartley & Colpitts Oscillators for RF range $f_0 \geq 100$KHz.

6. Testing for the performance of BJT -Crystal Oscillator for $f_0 > 100$ KHz
7 Testing of Diode clipping (Single/Double ended) circuits for peak clipping, peak detection

8. Testing of Clamping circuits: positive clamping /negative clamping.
9. Testing of a transformer less Class – B push pull power amplifier and determination of its conversion efficiency.

10. Testing of Half wave, Full wave and Bridge Rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency



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11. Verification of Thevinin's Theorem and Maximum Power Transfer theorem for DC Circuits.

12. Characteristics of Series and Parallel resonant circuits.

## LOGIC DESIGN LAB
## (Common to EC/TC/EE/IT/BM/ML)

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | : | **10ESL38** | **IA Marks** | : | **25** |
| **Hrs/ Week** | : | **03** | **Exam Hours** | : | **03** |
| **Total Hrs.** | : | | **Exam Marks** | : | **50** |

**NOTE:** Use discrete components to test and verify the logic gates. LabView can be used for designing the gates along with the above.

1. Simplification, realization of Boolean expressions using logic gates/Universal gates.
2. Realization of Half/Full adder and Half/Full Subtractors using logic gates.
3. (i) Realization of parallel adder/Subtractors using 7483 chip
   (ii) BCD to Excess-3 code conversion and vice versa.
4. Realization of Binary to Gray code conversion and vice versa
5. MUX/DEMUX – use of 74153, 74139 for arithmetic circuits and code converter.
6. Realization of One/Two bit comparator and study of 7485 magnitude comparator.
7. Use of a) Decoder chip to drive LED display and b) Priority encoder.
8. Truth table verification of Flip-Flops: (i) JK Master slave (ii) T type and (iii) D type.
9. Realization of 3 bit counters as a sequential circuit and MOD – N counter design (7476, 7490, 74192, 74193).
10. Shift left; Shift right, SIPO, SISO, PISO, PIPO operations using 74S95.
11. Wiring and testing Ring counter/Johnson counter.
12. Wiring and testing of Sequence generator.



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## ELECTRONIC INSTRUMENTATION
**(Common to EC/TC/IT/BM/ML)**

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | : | **10IT35** | **IA Marks** | : | **25** |
| **Hrs/ Week** | : | **04** | **Exam Hours** | : | **03** |
| **Total Hrs.** | : | **52** | **Exam Marks** | : | **100** |

**UNIT – 1:**
**Introduction**
**(a) Measurement Errors:** Gross errors and systematic errors, Absolute and relative errors, Accuracy, Precision, Resolution and Significant figures.
**(b) Voltmeters and Multimeters** Introduction, Multirange voltmeter, Extending voltmeter ranges, Loading, AC voltmeter using Rectifiers – Half wave and full wave, Peak responding and True RMS voltmeters.

**UNIT – 2:**
**Digital Instruments**
Digital Voltmeters – Introduction, DVM's based on V – T, V – F and Successive approximation principles, Resolution and sensitivity, General specifications, Digital Multi-meters, Digital frequency meters, Digital measurement of time.

**UNIT – 3:**
**Oscilloscopes**
Introduction, Basic principles, CRT features, Block diagram and working of each block, Typical CRT connections, Dual beam and dual trace CROs, Electronic switch.
**UNIT – 4:**
**Special Oscilloscopes**
Delayed time-base oscilloscopes, Analog storage, Sampling and Digital storage oscilloscopes.

**UNIT – 5:**
**Signal Generators**



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Introduction, Fixed and variable AF oscillator, Standard signal generator, Laboratory type signal generator, AF sine and Square wave generator, Function generator, Square and Pulse generator, Sweep frequency generator, Frequency synthesizer.

**UNIT – 6:**

**Measurement of resistance, inductance and capacitance**

Whetstone's bridge, Kelvin Bridge; AC bridges, Capacitance Comparison Bridge, Maxwell's bridge, Wein's bridge, Wagner's earth connection

**UNIT – 7:**

**Transducers - I**

Introduction, Electrical transducers, Selecting a transducer, Resistive transducer, Resistive position transducer, Strain gauges, Resistance thermometer, Thermistor, Inductive transducer, Differential output transducers and LVDT.

**UNIT – 8:**

**Miscellaneous Topics**

**(a) Transducers - II** –Piezoelectric transducer, Photoelectric transducer, Photovoltaic transducer, Semiconductor photo devices, Temperature transducers-RTD, Thermocouple .

**(b) Display devices:** Digital display system, classification of display, Display devices, LEDs, LCD displays.

**(c)** Bolometer and RF power measurement using Bolometer

**(d)** Introduction to Signal conditioning.

(e) Introduction to LabView.

**TEXT BOOKS:**


1. **"Electronic Instrumentation",** H. S. Kalsi, TMH, 3rd 2010
2. **"Electronic Instrumentation and Measurements",** David A Bell, PHI / Pearson Education, 2006.


**REFERENCE BOOKS:**


1. **"Principles of measurement systems",** John P. Beately, 3rd Edition, Pearson Education, 2000
2. **"Modern electronic instrumentation and measuring techniques",** Cooper D & A D Helfrick, PHI, 1998.
3. **Electronics & electrical measurements,** A K Sawhney, , Dhanpat Rai & sons, 9th edition.




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**Oscillators:** Oscillator operation, Phase shift Oscillator, Wienbridge Oscillator, Tuned Oscillator circuits, Crystal Oscillator. (BJT Version Only) Simple design methods of Oscillators.

**UNIT 8:**

**FET Amplifiers:** FET small signal model, Biasing of FET, Common drain common gate configurations, MOSFETs, FET amplifier networks.

**TEXT BOOK:**

1. **"Electronic Devices and Circuit Theory",** Robert L. Boylestad and Louis Nashelsky, PHI/Pearson Eduication. 9TH Edition.

**REFERENCE BOOKS:**

1. **'Integrated Electronics',** Jacob Millman & Christos C. Halkias, Tata - McGraw Hill, 2nd Edition, 2010
2. **"Electronic Devices and Circuits",** David A. Bell, PHI, 4th Edition, 2004
3. **"Analog Electronics Circuits: A Simplified Approach",** U.B. Mahadevaswamy, Pearson/Saguine, 2007.

## LOGIC DESIGN
## (Common to EC/TC/EE/IT/BM/ML)

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | **:** | **10ES33** | **IA Marks** | **:** | **25** |
| **Hrs/ Week** | **:** | **04** | **Exam Hours** | **:** | **03** |
| **Total Hrs.** | **:** | **52** | **Exam Marks** | **:** | **100** |

**UNIT 1:**

**Principles of combinational logic-1:** Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3, 4 and 5 variables, Incompletely specified functions (Don't Care terms), Simplifying Max term equations.

**UNIT 2:**



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**Principles of combinational Logic-2:** Quine-McCluskey minimization technique- Quine-McCluskey using don't care terms, Reduced Prime Implicant Tables, Map entered variables.

**UNIT 3:**

**Analysis and design of combinational logic - I:** General approach, Decoders-BCD decoders, Encoders.

**UNIT 4:**

**Analysis and design of combinational logic - II:** Digital multiplexers-Using multiplexers as Boolean function generators. Adders and subtractors-Cascading full adders, Look ahead carry, Binary comparators. Design methods of building blocks of combinational logics.

**UNIT 5:**

**Sequential Circuits – 1:** Basic Bistable Element, Latches, SR Latch, Application of SR Latch, A Switch Debouncer, The $\overline{S}\overline{R}$ Latch, The gated SR Latch, The gated D Latch, The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The Master-Slave SR Flip-Flops, The Master-Slave JK Flip-Flop. Edge Triggered Flip-Flop: The Positive Edge-Triggered D Flip-Flop, Negative-Edge Triggered D Flip-Flop.

**UNIT 6:**

**Sequential Circuits – 2:** Characteristic Equations, Registers, Counters - Binary Ripple Counters, Synchronous Binary counters, Counters based on Shift Registers, Design of a Synchronous counters, Design of a Synchronous Mod-6 Counter using clocked JK Flip-Flops Design of a Synchronous Mod-6 Counter using clocked D, T, or SR Flip-Flops

**UNIT 7:**

**Sequential Design - I:** Introduction, Mealy and Moore Models, State Machine Notation, Synchronous Sequential Circuit Analysis and Design.

**UNIT 8:**

**Sequential Design - II:** Construction of state Diagrams, Counter Design.



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**TEXT BOOKS:**

1. **"Digital Logic Applications and Design"**, John M Yarbrough, Thomson Learning, 2001.
2. **"Digital Principles and Design "**, Donald D Givone, Tata McGraw Hill Edition, 2002.

**REFERENCE BOOKS:**

1. **"Fundamentals of logic design"**, Charles H Roth, Jr; Thomson Learning, 2004.
2. **"Logic and computer design Fundamentals"**, Mono and Kim, Pearson, Second edition, 2001.
3. **"Logic Design"**, Sudhakar Samuel, Pearson/Saguine, 2007

## NETWORK ANALYSIS
## (Common to EC/TC/EE/IT/BM/ML)

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | **:** | **10ES34** | **IA Marks** | **:** | **25** |
| **Hrs/ Week** | **:** | **04** | **Exam Hours** | **:** | **03** |
| **Total Hrs.** | **:** | **52** | **Exam Marks** | **:** | **100** |

**UNIT 1:**

**Basic Concepts**: Practical sources, Source transformations, Network reduction using Star – Delta transformation, Loop and node analysis With linearly dependent and independent sources for DC and AC networks, Concepts of super node and super mesh.

**UNIT 2:**

**Network Topology:** Graph of a network, Concept of tree and co-tree, incidence matrix, tie-set, tie-set and cut-set schedules, Formulation of equilibrium equations in matrix form, Solution of resistive networks, Principle of duality.

**UNIT 3:**

**Network Theorems – 1:** Superposition, Reciprocity and Millman's theorems.



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11. Verification of Thevinin's Theorem and Maximum Power Transfer theorem for DC Circuits.

12. Characteristics of Series and Parallel resonant circuits.

## LOGIC DESIGN LAB
## (Common to EC/TC/EE/IT/BM/ML)

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | : | **10ESL38** | **IA Marks** | : | **25** |
| **Hrs/ Week** | : | **03** | **Exam Hours** | : | **03** |
| **Total Hrs.** | : | | **Exam Marks** | : | **50** |

**NOTE:** Use discrete components to test and verify the logic gates. LabView can be used for designing the gates along with the above.

1. Simplification, realization of Boolean expressions using logic gates/Universal gates.
2. Realization of Half/Full adder and Half/Full Subtractors using logic gates.
3. (i) Realization of parallel adder/Subtractors using 7483 chip
   (ii) BCD to Excess-3 code conversion and vice versa.
4. Realization of Binary to Gray code conversion and vice versa
5. MUX/DEMUX – use of 74153, 74139 for arithmetic circuits and code converter.
6. Realization of One/Two bit comparator and study of 7485 magnitude comparator.
7. Use of a) Decoder chip to drive LED display and b) Priority encoder.
8. Truth table verification of Flip-Flops: (i) JK Master slave (ii) T type and (iii) D type.
9. Realization of 3 bit counters as a sequential circuit and MOD – N counter design (7476, 7490, 74192, 74193).
10. Shift left; Shift right, SIPO, SISO, PISO, PIPO operations using 74S95.
11. Wiring and testing Ring counter/Johnson counter.
12. Wiring and testing of Sequence generator.



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**UNIT 6:**

**Applications of Fourier representations:** Introduction, Frequency response of LTI systems, Fourier transform representation of periodic signals, Fourier transform representation of discrete time signals. Sampling theorm and Nyquist rate.

**UNIT 7:**

**Z-Transforms – 1:** Introduction, Z – transform, properties of ROC, properties of Z – transforms, inversion of Z – transforms.

**UNIT 8:**

**Z-transforms – 2:** Transform analysis of LTI Systems, unilateral Z-Transform and its application to solve difference equations.

**TEXT BOOK**


1. **Simon Haykin,** "Signals and Systems", John Wiley India Pvt. Ltd., 2nd Edn, 2008.
2. **Michael Roberts,** "Fundamentals of Signals & Systems", 2nd ed, Tata McGraw-Hill, 2010


**REFERENCE BOOKS:**


1. **Alan V Oppenheim, Alan S, Willsky and A Hamid Nawab,** "Signals and Systems" Pearson Education Asia / PHI, 2nd edition, 1997. Indian Reprint 2002
2. **H. P Hsu, R. Ranjan,** "Signals and Systems", Scham's outlines, TMH, 2006
3. **B. P. Lathi,** "Linear Systems and Signals", Oxford University Press, 2005
4. **Ganesh Rao and Satish Tunga,** "Signals and Systems", Pearson/Sanguine Technical Publishers, 2004


## FUNDAMENTALS OF HDL
## (Common to EC/TC/IT/BM/ML)

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | : | **10EC45** | **IA Marks** | : | **25** |
| **Hrs/ Week** | : | **04** | **Exam Hours** | : | **03** |
| **Total Hrs.** | : | **52** | **Exam Marks** | : | **100** |

**UNIT 1:**



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**Introduction:** Why HDL? , A Brief History of HDL, Structure of HDL Module, Operators, Data types, Types of Descriptions, simulation and synthesis, Brief comparison of VHDL and Verilog

**UNIT 2:**
**Data –Flow Descriptions:** Highlights of Data-Flow Descriptions, Structure of Data-Flow Description, Data Type – Vectors.

**UNIT 3:**
**Behavioral Descriptions:** Behavioral Description highlights, structure of HDL behavioral Description, The VHDL variable –Assignment Statement, sequential statements.

**UNIT 4:**
**Structural Descriptions**: Highlights of structural Description, Organization of the structural Descriptions, Binding, state Machines, Generate, Generic, and Parameter statements.

**UNIT 5: Procedures, Tasks, and Functions:** Highlights of Procedures, tasks, and Functions, Procedures and tasks, Functions.
**Advanced HDL Descriptions:** File Processing, Examples of File Processing

**UNIT 6:**
**Mixed –Type Descriptions:** Why Mixed-Type Description? VHDL User-Defined Types, VHDL Packages, Mixed-Type Description examples

**UNIT 7:**
**Mixed –Language Descriptions:** Highlights of Mixed-Language Description, How to invoke One language from the Other, Mixed-language Description Examples, Limitations of Mixed-Language Description.
**UNIT 8:**
**Synthesis Basics:** Highlights of Synthesis, Synthesis information from Entity and Module, Mapping Process and Always in the Hardware Domain.

**TEXT BOOKS:**



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1. **HDL Programming (VHDL and Verilog)**- Nazeih M.Botros- John Weily India Pvt. Ltd. 2008.

**REFERENCE BOOKS:**

1. **Fundamentals of HDL** – Cyril P.R. Pearson/Sanguin 2010.
2. **VHDL** -Douglas perry-Tata McGraw-Hill
3. **A Verilog HDL Primer**- J.Bhaskar – BS Publications
4. **Circuit Design with VHDL**-Volnei A.Pedroni-PHI

## LINEAR IC's & APPLICATIONS
## (Common to EC/TC/IT/BM/ML)

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | : | **10EC46** | **IA Marks** | : | **25** |
| **Hrs/ Week** | : | **04** | **Exam Hours** | : | **03** |
| **Total Hrs.** | : | **52** | **Exam Marks** | : | **100** |

**UNIT 1:**

**Operational Amplifier Fundamentals**: Basic Op-Amp circuit, Op-Amp parameters – Input and output voltage, CMRR and PSRR, offset voltages and currents, Input and output impedances, Slew rate and Frequency limitations; Op-Amps as DC Amplifiers- Biasing Op-Amps, Direct coupled -Voltage Followers, Non-inverting Amplifiers, Inverting amplifiers, Summing amplifiers, Difference amplifier.

**UNIT 2:**

**Op-Amps as AC Amplifiers:** Capacitor coupled Voltage Follower, High input impedance - Capacitor coupled Voltage Follower, Capacitor coupled Non-inverting Amplifiers, High input impedance - Capacitor coupled Non-inverting Amplifiers, Capacitor coupled Inverting amplifiers, setting the upper cut-off frequency, Capacitor coupled Difference amplifier, Use of a single polarity power supply.

**UNIT 3:**

**Op-Amps frequency response and compensation:** Circuit stability, Frequency and phase response, Frequency compensating methods, Band width, Slew rate effects, $Z_{in}$ Mod compensation, and circuit stability precautions.

**UNIT 4:**



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**HDL LAB**
**(Common to EC/TC/IT/BM/ML)**

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | : | **10ECL48** | **IA Marks** | : | **25** |
| **Hrs/ Week** | : | **03** | **Exam Hours** | : | **03** |
| **Total Hrs.** | : | **42** | **Exam Marks** | : | **50** |

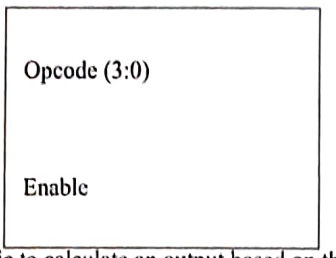
Note: Programming can be done using any compiler. Download the programs on a FPGA/CPLD boards such as Apex/Acex/Max/Spartan/Sinti/TK Base or equivalent and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

**PROGRAMMING (using VHDL /Verilog)**

1. Write HDL code to realize all the logic gates
2. Write a HDL program for the following combinational designs
   a. 2 to 4 decoder
   b. 8 to 3 (encoder without priority & with priority)
   c. 8 to 1 multiplexer
   d. 4 bit binary to gray converter
   e. Multiplexer, de-multiplexer, comparator.
2. Write a HDL code to describe the functions of a Full Adder Using three modeling styles.

3. Write a model for 32 bit ALU using the schematic diagram shown below

A (31:0) B (31:0)




- ALU should use combinational logic to calculate an output based on the four bit op-code input.
- ALU should pass the result to the out bus when enable line in high, and tri-state the out bus when the enable line is low.



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- ALU should decode the 4 bit op-code according to the given in example below.

| OPCODE | ALU OPERATION |
|---|---|
| 1. | A + B |
| 2. | A – B |
| 3. | A Complement |
| 4. | A * B |
| 5. | A AND B |
| 6. | A OR B |
| 7. | A NAND B |
| 8. | A XOR B |

4. Develop the HDL code for the following flip-flops, SR, D, JK, T.
5. Design 4 bit binary, BCD counters (Synchronous reset and Asynchronous reset) and "any sequence" counters

**INTERFACING** (at least four of the following must be covered using VHDL/Verilog)

1. Write HDL code to display messages on the given seven segment display and LCD and accepting Hex key pad input data.

2. Write HDL code to control speed, direction of DC and Stepper motor.

3. Write HDL code to accept 8 channel Analog signal, Temperature sensors and display the data on LCD panel or Seven segment display.

4. Write HDL code to generate different waveforms (Sine, Square, Triangle, Ramp etc.,) using DAC change the frequency and amplitude.

5. Write HDL code to simulate Elevator operations
6. Write HDL code to control external lights using relays.



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1. **HDL Programming (VHDL and Verilog)**- Nazeih M.Botros- John Weily India Pvt. Ltd. 2008.

**REFERENCE BOOKS:**

1. **Fundamentals of HDL** – Cyril P.R. Pearson/Sanguin 2010.
2. **VHDL** -Douglas perry-Tata McGraw-Hill
3. **A Verilog HDL Primer**- J.Bhaskar – BS Publications
4. **Circuit Design with VHDL**-Volnei A.Pedroni-PHI

## LINEAR IC's & APPLICATIONS
## (Common to EC/TC/IT/BM/ML)

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | : | **10EC46** | **IA Marks** | : | **25** |
| **Hrs/ Week** | : | **04** | **Exam Hours** | : | **03** |
| **Total Hrs.** | : | **52** | **Exam Marks** | : | **100** |

**UNIT 1:**

**Operational Amplifier Fundamentals**: Basic Op-Amp circuit, Op-Amp parameters – Input and output voltage, CMRR and PSRR, offset voltages and currents, Input and output impedances, Slew rate and Frequency limitations; Op-Amps as DC Amplifiers- Biasing Op-Amps, Direct coupled -Voltage Followers, Non-inverting Amplifiers, Inverting amplifiers, Summing amplifiers, Difference amplifier.

**UNIT 2:**

**Op-Amps as AC Amplifiers:** Capacitor coupled Voltage Follower, High input impedance - Capacitor coupled Voltage Follower, Capacitor coupled Non-inverting Amplifiers, High input impedance - Capacitor coupled Non-inverting Amplifiers, Capacitor coupled Inverting amplifiers, setting the upper cut-off frequency, Capacitor coupled Difference amplifier, Use of a single polarity power supply.

**UNIT 3:**

**Op-Amps frequency response and compensation:** Circuit stability, Frequency and phase response, Frequency compensating methods, Band width, Slew rate effects, $Z_{in}$ Mod compensation, and circuit stability precautions.

**UNIT 4:**



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**OP-AMP Applications:** Voltage sources, current sources and current sinks, Current amplifiers, instrumentation amplifier, precision rectifiers, Limiting circuits.

**UNIT 5:**

**More applications:** Clamping circuits, Peak detectors, sample and hold circuits, V to I and I to V converters, Log and antilog amplifiers, Multiplier and divider, Triangular / rectangular wave generators, Wave form generator design, phase shift oscillator, Wein bridge oscillator.

**UNIT 6:**

**Non-linear circuit applications:** crossing detectors, inverting Schmitt trigger circuits, Monostable & Astable multivibrator, Active Filters –First and second order Low pass & High pass filters.

**UNIT 7:**

**Voltage Regulators:** Introduction, Series Op-Amp regulator, IC Voltage regulators, 723 general purpose regulator, Switching regulator.

**UNIT 8:**

Other Linear IC applications: 555 timer - Basic timer circuit, 555 timer used as astable and monostable multivibrator, Schmitt trigger; PLL-operating principles, Phase detector / comparator, VCO; D/A and A/ D converters – Basic DAC Techniques, AD converters.

**TEXT BOOKS:**


1. **"Operational Amplifiers and Linear IC's",** David A. Bell, 2nd edition, PHI/Pearson, 2004
2. **"Linear Integrated Circuits",** D. Roy Choudhury and Shail B. Jain, 2nd edition, Reprint 2006, New Age International


**REFERENCE BOOKS:**


**1. "Opamps- Design, Applications and Trouble Shooting",** Terrell, Elsevier, 3rd ed. 2006.

**2. "Operational Amplifiers",** George Clayton and Steve Winder, Elsever 5th ed., 2008




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3. **"Operational Amplifiers and Linear Integrated Circuits"**, Robert. F. Coughlin & Fred.F. Driscoll, PHI/Pearson, 2006
4. **"Design with Operational Amplifiers and Analog Integrated Circuits"**, Sergio Franco, TMH, 3e, 2005

## MICROCONTROLLERS LAB
**(Common to EC/TC/EE/IT/BM/ML)**

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | : | **10ESL47** | **IA Marks** | : | **25** |
| **Hrs/ Week** | : | **03** | **Exam Hours** | : | **03** |
| **Total Hrs.** | : | **42** | **Exam Marks** | : | **50** |

### I. PROGRAMMING

1. Data Transfer - Block move, Exchange, Sorting, Finding largest element in an array.
2. Arithmetic Instructions - Addition/subtraction, multiplication and division, square, Cube – (16 bits Arithmetic operations – bit addressable).
3. Counters.
4. Boolean & Logical Instructions (Bit manipulations).
5. Conditional CALL & RETURN.
6. Code conversion: BCD – ASCII; ASCII – Decimal; Decimal - ASCII; HEX - Decimal and Decimal - HEX .
7. Programs to generate delay, Programs using serial port and on-Chip timer / counter.

**Note: Programming exercise is to be done on both 8051 & MSP430.**

### II. INTERFACING:

Write C programs to interface 8051 chip to Interfacing modules to develop single chip solutions.

8. Simple Calculator using 6 digit seven segment displays and Hex Keyboard interface to 8051.
9. Alphanumeric LCD panel and Hex keypad input interface to 8051.
10. External ADC and Temperature control interface to 8051.
11. Generate different waveforms Sine, Square, Triangular, Ramp etc. using DAC interface to 8051; change the frequency and amplitude.
12. Stepper and DC motor control interface to 8051.
13. Elevator interface to 8051.



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## ENGINEERING MATHEMATICS - IV

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | : | **10MAT41** | **IA Marks** | : | **25** |
| **Hrs/ Week** | : | **04** | **Exam Hours** | : | **03** |
| **Total Hrs.** | : | **52** | **Exam Marks** | : | **100** |

**UNIT 1:**

**Numerical Methods**

Numerical solutions of first order and first degree ordinary differential equations – Taylor's series method, Modified Euler's method, Runge – Kutta method of fourth order, Milne's and Adams-Bashforth predictor and corrector methods (All formulae without Proof).

**UNIT 2:**

**Complex Variables**

Function of a complex variable, Limit, Continuity Differentiability – Definitions. Analytic functions, Cauchy – Riemann equations in cartesian and polar forms, Properties of analytic functions. Conformal Transformation – Definition. Discussion of transformations: $W = z^2$, $W = e^z$, $W = z + (I/z)$, $z \neq 0$ Bilinear transformations.

**UNIT 3:**

**Complex Integration**

Complex line integrals, Cauchy's theorem, Cauchy's integral formula. Taylor's and Laurent's series (Statements only) Singularities, Poles, Residues, Cauchy's residue theorem (statement only).

**UNIT 4:**

**Series solution of Ordinary Differential Equations and Special Functions**

Series solution – Frobenius method, Series solution of Bessel's D.E. leading to Bessel function of fist kind. Equations reducible to Bessel's D.E., Series solution of Legendre's D.E. leading to Legendre Polynomials. Rodirgue's formula.

**UNIT 5:**



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**Statistical Methods**

Curve fitting by the method of least squares: $y = a + bx$, $y = a + bx + cx^2$, $y = ax^b$ $y = ab^x$, $y = ae^{bx}$, Correlation and Regression.

Probability: Addition rule, Conditional probability, Multiplication rule, Baye's theorem.

**UNIT 6:**

Random Variables (Discrete and Continuous) p.d.f., c.d.f. Binomial, Poisson, Normal and Exponential distributions.

**UNIT 7:**

Sampling, Sampling distribution, Standard error. Testing of hypothesis for means. Confidence limits for means, Student's t distribution, Chi-square distribution as a test of goodness of fit.

**UNIT 8:**

Concept of joint probability – Joint probability distribution, Discrete and Independent random variables. Expectation, Covariance, Correlation coefficient.

Probability vectors, Stochastic matrices, Fixed points, Regular stochastic matrices. Markov chains, Higher transition probabilities. Stationary distribution of regular Markov chains and absorbing states.

**Text book:**

1. **Higher Engineering Mathematics** by Dr. B.S. Grewal, 36th Edn. Kanna Publications.
2. **Probability** by Seymour Lipschutz (Schaum's series)

**Reference Books:**

1. **Higher Engineering Mathematics** by B.V. Ramana (Tata-Macgraw Hill).
2. **Advanced Modern Engineering Mathematics** by Glyn James – Pearson Education.



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## MICROCONTROLLERS
## (Common to EC/TC/EE/IT/BM/ML)

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | : | **10ES42** | **IA Marks** | : | **25** |
| **Hrs/ Week** | : | **04** | **Exam Hours** | : | **03** |
| **Total Hrs.** | : | **52** | **Exam Marks** | : | **100** |

**UNIT 1:**
Microprocessors and microcontroller. Introduction, Microprocessors and Microcontrollers, RISC & CISC CPU Architectures, Harvard & Von-Neumann CPU architecture, Computer software.
The 8051 Architecture: Introduction, Architecture of 8051, Pin diagram of 8051, Memory organization, External Memory interfacing, Stacks.

**UNIT 2:**
Addressing Modes: Introduction, Instruction syntax, Data types, Subroutines, Addressing modes: Immediate addressing , Register addressing, Direct addressing, Indirect addressing, relative addressing, Absolute addressing, Long addressing, Indexed addressing, Bit inherent addressing, bit direct addressing.
Instruction set: Instruction timings, 8051 instructions: Data transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Subroutine instructions, Bit manipulation instruction.

**UNIT 3:**
8051 programming: Assembler directives, Assembly language programs and Time delay calculations.

**UNIT 4:**
8051 Interfacing and Applications: Basics of I/O concepts, I/O Port Operation, Interfacing 8051 to LCD, Keyboard, parallel and serial ADC, DAC, Stepper motor interfacing and DC motor interfacing and programming

**UNIT 5:**
8051 Interrupts and Timers/counters: Basics of interrupts, 8051 interrupt structure, Timers and Counters, 8051 timers/counters, programming 8051 timers in assembly and C .

**UNIT 6:**



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8051 Serial Communication: Data communication, Basics of Serial Data Communication, 8051 Serial Communication, connections to RS-232, Serial communication Programming in assembly and C.
8255A Programmable Peripheral Interface., Architecture of 8255A, I/O addressing., I/O devices interfacing with 8051 using 8255A.

Course Aim – The MSP430 microcontroller is ideally suited for development of low-power embedded systems that must run on batteries for many years. There are also applications where MSP430 microcontroller must operate on energy harvested from the environment. This is possible due to the ultra-low power operation of MSP430 and the fact that it provides a complete system solution including a RISC CPU, flash memory, on-chip data converters and on-chip peripherals.

UNIT 7:

**Motivation for MSP430microcontrollers** – Low Power embedded systems, On-chip peripherals (analog and digital), low-power RF capabilities. Target applications (Single-chip, low cost, low power, high performance system design).
**MSP430 RISC CPU architecture,** Compiler-friendly features, Instruction set, Clock system, Memory subsystem. Key differentiating factors between different MSP430 families.
**Introduction to Code Composer Studio** (CCS v4). Understanding how to use CCS for Assembly, C, Assembly+C projects for MSP430 microcontrollers. Interrupt programming.
**Digital I/O – I/O ports** programming using C and assembly, Understanding the muxing scheme of the MSP430 pins.

UNIT 8:
**On-chip peripherals. Watchdog Timer, Comparator,** Op-Amp, Basic Timer, Real Time Clock (RTC), ADC, DAC, SD16, LCD, DMA.
**Using the Low-power features of MSP430.** Clock system, low-power modes, Clock request feature, Low-power programming and Interrupt.
**Interfacing LED, LCD, External memory.** Seven segment LED modules interfacing. Example – Real-time clock.
**Case Studies of applications of MSP430** - Data acquisition system, Wired Sensor network, Wireless sensor network with Chipcon RF interfaces.



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**TEXT BOOKS:**

1. **"The 8051 Microcontroller and Embedded Systems – using assembly and C "-**, Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay, PHI, 2006 / Pearson, 2006
2. **"MSP430 Microcontroller Basics"**, John Davies, Elsevier, 2008.

**REFERENCE BOOKS:**

1. **"The 8051 Microcontroller Architecture, Programming & Applications"**, 2e Kenneth J. Ayala ;, Penram International, 1996 / Thomson Learning 2005.
2. **"The 8051 Microcontroller"**, V.Udayashankar and MalikarjunaSwamy, TMH, 2009
3. **MSP430 Teaching CD-ROM,** Texas Instruments, 2008 (can be requested **http://www.uniti.in** )
4. **Microcontrollers: Architecture, Programming, Interfacing and System Design"**,Raj Kamal, "Pearson Education, 2005

## CONTROL SYSTEMS
## (Common to EC/TC/EE/IT/BM/ML)

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | **:** | **10ES43** | **IA Marks** | **:** | **25** |
| **Hrs/ Week** | **:** | **04** | **Exam Hours** | **:** | **03** |
| **Total Hrs.** | **:** | **52** | **Exam Marks** | **:** | **100** |

**UNIT 1:**

**Modeling of Systems:** Introduction to Control Systems, Types of Control Systems, Effect of Feedback Systems, Differential equation of Physical Systems -Mechanical systems, Friction, Translational systems (Mechanical accelerometer, systems excluded), Rotational systems, Gear trains, Electrical systems, Analogous systems

**UNIT 2:**

**Block diagrams and signal flow graphs:** Transfer functions, Block diagram algebra, Signal Flow graphs (State variable formulation excluded),



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3. **"Operational Amplifiers and Linear Integrated Circuits"**, Robert. F. Coughlin & Fred.F. Driscoll, PHI/Pearson, 2006
4. **"Design with Operational Amplifiers and Analog Integrated Circuits"**, Sergio Franco, TMH, 3e, 2005

## MICROCONTROLLERS LAB
**(Common to EC/TC/EE/IT/BM/ML)**

| | | | | | |
|---|---|---|---|---|---|
| **Sub Code** | : | **10ESL47** | **IA Marks** | : | **25** |
| **Hrs/ Week** | : | **03** | **Exam Hours** | : | **03** |
| **Total Hrs.** | : | **42** | **Exam Marks** | : | **50** |

### I. PROGRAMMING

1. Data Transfer - Block move, Exchange, Sorting, Finding largest element in an array.
2. Arithmetic Instructions - Addition/subtraction, multiplication and division, square, Cube – (16 bits Arithmetic operations – bit addressable).
3. Counters.
4. Boolean & Logical Instructions (Bit manipulations).
5. Conditional CALL & RETURN.
6. Code conversion: BCD – ASCII; ASCII – Decimal; Decimal - ASCII; HEX - Decimal and Decimal - HEX .
7. Programs to generate delay, Programs using serial port and on-Chip timer / counter.

**Note: Programming exercise is to be done on both 8051 & MSP430.**

### II. INTERFACING:

Write C programs to interface 8051 chip to Interfacing modules to develop single chip solutions.

8. Simple Calculator using 6 digit seven segment displays and Hex Keyboard interface to 8051.
9. Alphanumeric LCD panel and Hex keypad input interface to 8051.
10. External ADC and Temperature control interface to 8051.
11. Generate different waveforms Sine, Square, Triangular, Ramp etc. using DAC interface to 8051; change the frequency and amplitude.
12. Stepper and DC motor control interface to 8051.
13. Elevator interface to 8051.



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## DIGITAL SIGNAL PROCESSING

| | | | |
|---|---|---|---|
| Subject Code | : **10EC52** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

Discrete Fourier Transforms (DFT): Frequency domain sampling and reconstruction of discrete time signals. DFT as a linear transformation, its relationship with other transforms.

**UNIT - 2**

Properties of DFT, multiplication of two DFTs- the circular convolution, additional DFT properties.

**UNIT - 3**

Use of DFT in linear filtering, overlap-save and overlap-add method.
Direct computation of DFT, need for efficient computation of the DFT (FFT algorithms).

**UNIT - 4**

Radix-2 FFT algorithm for the computation of DFT and IDFT–decimation-in-time and decimation-in-frequency algorithms. Goertzel algorithm, and chirp-z transform

**UNIT - 5**

IIR filter design: Characteristics of commonly used analog filters – Butterworth and Chebysheve filters, analog to analog frequency transformations.

**UNIT - 6**

Implementation of discrete-time systems: Structures for IIR and FIR systems-direct form I and direct form II systems, cascade, lattice and parallel realization.

**UNIT - 7**

FIR filter design: Introduction to FIR filters, design of FIR filters using - Rectangular, Hamming, Bartlet and Kaiser windows, FIR filter design using frequency sampling technique.

**UNIT - 8**

Design of IIR filters from analog filters (Butterworth and Chebyshev) - impulse invariance method. Mapping of transfer functions: Approximation of derivative (backward difference and bilinear transformation) method, Matched z transforms, Verification for stability and linearity during mapping

**TEXT BOOK:**

1. **Digital signal processing – Principles Algorithms & Applications**, Proakis & Monalakis, Pearson education, 4th Edition, New Delhi, 2007.

**REFERENCE BOOKS:**

1. **Discrete Time Signal Processing**, Oppenheim & Schaffer, PHI, 2003.
2. **Digital Signal Processing**, S. K. Mitra, Tata Mc-Graw Hill, 3rd Edition, 2010.
3. **Digital Signal Processing**, Lee Tan: Elsivier publications, 2007

## ANALOG COMMUNICATION

| | | | |
|---|---|---|---|
| Subject Code | : **10EC53** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

**RANDOM PROCESS:** Random variables: Several random variables. Statistical averages: Function of Random variables, moments, Mean, Correlation and Covariance function: Principles of autocorrelation function, cross – correlation functions. Central limit theorem, Properties of Gaussian process.

**UNIT - 2**

**AMPLITUDE MODULATION:** Introduction, AM: Time-Domain description, Frequency – Domain description. Generation of AM wave: square law modulator, switching modulator. Detection of AM waves: square law detector, envelop detector. Double side band suppressed carrier modulation (DSBSC): Time-Domain description, Frequency-Domain representation, Generation of DSBSC waves: balanced modulator, ring modulator. Coherent detection of DSBSC modulated waves. Costas loop.

**UNIT - 3**

V SEMESTER

## MANAGEMENT & ENTREPRENEURSHIP

| | | | |
|---|---|---|---|
| Subject Code | : **10AL51** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

### MANAGEMENT

**UNIT - 1**

**MANAGEMENT:** Introduction - Meaning - nature and characteristics of Management, Scope and functional areas of Management - Management as a Science, Art or Profession Management & Administration - Roles of Management, Levels of Management, Development of Management Thought-Early Management Approaches-Modern Management Approaches.

**UNIT - 2**

**PLANNING:** Nature, importance and purpose of planning process - Objectives - Types of plans (Meaning only) - Decision making - Importance of planning - steps in planning & planning premises - Hierarchy of plans.

**UNIT - 3**

**ORGANISING AND STAFFING:** Nature and purpose of organization - Principles of organization - Types of organization - Departmentation - Committees – Centralisation Vs Decentralisation of authority and responsibility - Span of control - MBO and MBE (Meaning only) Nature and importance of Staffing - Process of Selection & Recruitment (in brief).

**UNIT - 4**

**DIRECTING & CONTROLLING:** Meaning and nature of directing - Leadership styles, Motivation Theories, Communication - Meaning and importance – Coordination, meaning and importance and Techniques of Co - ordination. Meaning and steps in controlling - Essentials of a sound control system - Methods of establishing control.

### ENTREPRENEURSHIP

**UNIT - 5**

**ENTREPRENEUR:** Meaning of Entrepreneur; Evolution of the Concept, Functions of an Entrepreneur, Types of Entrepreneur, Intrapreneur - an emerging Class. Concept of Entrepreneurship - Evolution of

Entrepreneurship, Development of Entrepreneurship; Stages in entrepreneurial process; Role of entrepreneurs in Economic Development; Entrepreneurship in India; Entrepreneurship – its Barriers.

**UNIT - 6**

**SMALL SCALE INDUSTRY:** Definition; Characteristics; Need and rationale: Objectives; Scope; role of SSI in Economic Development. Advantages of SSI Steps to start an SSI - Government policy towards SSI; Different Policies of S.S.I.; Government Support for S.S.I. during 5 year plans, Impact of Liberalization, Privatization, Globalization on S.S.I., Effect of WTO/GATT Supporting Agencies of Government for S.S.I Meaning; Nature of Support; Objectives; Functions; Types of Help; Ancillary Industry and Tiny Industry (Definition only).

**UNIT - 7**

**INSTITUTIONAL SUPPORT:** Different Schemes; TECKSOK; KIADB; KSSIDC; KSIMC; DIC Single Window Agency: SISI; NSIC; SIDBI; KSFC.

**UNIT - 8**

**PREPARATION OF PROJECT:** Meaning of Project; Project Identification; Project Selection; Project Report; Need and Significance of Report; Contents; formulation; Guidelines by Planning Commission for Project report; Network Analysis; Errors of Project Report; Project Appraisal. Identification of Business Opportunities - Market Feasibility Study; Technical Feasibility Study; Financial Feasibility Study & Social Feasibility Study.

**TEXT BOOKS:**


1. **Principles of Management** - P. C. Tripathi, P. N. Reddy; Tata McGraw Hill, 4th Edition, 2010
2. **Dynamics of Entrepreneurial Development & Management** - Vasant Desai Himalaya Publishing House.
3. **Entrepreneurship Development** - Small Business Enterprises - Poornima M Charantimath - Pearson Education – 2006.


**REFERENCE BOOKS:**


1. **Management Fundamentals** - Concepts, Application, Skill Development Robert Lusier – Thomson.
2. **Entrepreneurship Development** - S S Khanka - S Chand & Co.
3. **Management** - Stephen Robbins - Pearson Education /PHI -17th Edition, 2003.




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## FUNDAMENTALS OF CMOS VLSI

| | | | |
|---|---|---|---|
| Subject Code | : **10EC56** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

**BASIC MOS TECHNOLOGY:** Integrated circuit's era. Enhancement and depletion mode MOS transistors. nMOS fabrication. CMOS fabrication. Thermal aspects of processing. BiCMOS technology. Production of E-beam masks.

**MOS TRANSISTOR THEORY:** Introduction, MOS Device Design Equations, The Complementary CMOS Inverter – DC Characteristics, Static Load MOS Inverters, The Differential Inverter, The Transmission Gate, Tristate Inverter.

**UNIT - 2**

**CIRCUIT DESIGN PROCESSES:** MOS layers. Stick diagrams. Design rules and layout – lambda-based design and other rules. Examples. Layout diagrams. Symbolic diagrams. Tutorial exercises.

Basic Physical Design of Simple logic gates.

**UNIT - 3**

**CMOS LOGIC STRUCTURES:** CMOS Complementary Logic, Bi CMOS Logic, Pseudo-nMOS Logic, Dynamic CMOS Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS Domino Logic Cascaded Voltage Switch Logic (CVSL).

**UNIT - 4**

**BASIC CIRCUIT CONCEPTS:** Sheet resistance. Area capacitances. Capacitance calculations. The delay unit. Inverter delays. Driving capacitive loads. Propagation delays. Wiring capacitances.

**SCALING OF MOS CIRCUITS:** Scaling models and factors. Limits on scaling. Limits due to current density and noise.

**UNIT - 5**



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**CMOS SUBSYSTEM DESIGN:** Architectural issues. Switch logic. Gate logic. Design examples – combinational logic. Clocked circuits. Other system considerations.

Clocking Strategies

**UNIT - 6**

**CMOS SUBSYSTEM DESIGN PROCESSES:** General considerations. Process illustration. ALU subsystem. Adders. Multipliers.

**UNIT - 7**

**MEMORY, REGISTERS AND CLOCK:** Timing considerations. Memory elements. Memory cell arrays.

**UNIT - 8**

**TESTABILITY:** Performance parameters. Layout issues. I/O pads. Real estate. System delays. Ground rules for design. Test and testability.

**TEXT BOOKS:**

1. **CMOS VLSI Design – A Circuits and Systems Perspective. 3rd Edition. N.H. Weste and David Harris. Addison-Wesley, 2005.** (Refer to http://www.cmosvlsi.com)
2. **Principles of CMOS VLSI Design: A Systems Perspective,** Neil H. E. Weste, K. Eshragian, and ??? 3rd edition, Pearson Education (Asia) Pvt. Ltd., 200?. (Shift to the latest edition.)
3. **Basic VLSI Design** - Douglas A. Pucknell & Kamran Eshraghian, PHI 3rd Edition (original Edition – 1994), 2005.

**REFERENCE BOOKS:**

1. R. Jacob Baker. CMOS Circuit Design, Layout and Simulation. John Wiley India Pvt. Ltd, 2008
2. **Fundamentals of Semiconductor Devices,** M. K. Achuthan and K. N. Bhat, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2007.
3. **CMOS Digital Integrated Circuits: Analysis and Design,** Sung-Mo Kang & Yusuf Leblebici, 3rd Edition, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007.
4. **Analysis and Design of Digital Integrated Circuits** - D.A Hodges, H.G Jackson and R.A Saleh. 3rd Edition, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2007.

## DIGITAL SIGNAL PROCESSING LABORATORY

| | | | |
|---|---|---|---|
| Subject Code | : **10ECL57** | IA Marks | : 25 |
| No. of Practical Hrs/Week: 03 | | Exam Hours | : 03 |
| Total no. of Practical Hrs. | : 42 | Exam Marks | : 50 |



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**CMOS SUBSYSTEM DESIGN:** Architectural issues. Switch logic. Gate logic. Design examples – combinational logic. Clocked circuits. Other system considerations.

Clocking Strategies

**UNIT - 6**

**CMOS SUBSYSTEM DESIGN PROCESSES:** General considerations. Process illustration. ALU subsystem. Adders. Multipliers.

**UNIT - 7**

**MEMORY, REGISTERS AND CLOCK:** Timing considerations. Memory elements. Memory cell arrays.

**UNIT - 8**

**TESTABILITY:** Performance parameters. Layout issues. I/O pads. Real estate. System delays. Ground rules for design. Test and testability.

**TEXT BOOKS:**

1. **CMOS VLSI Design – A Circuits and Systems Perspective. 3rd Edition. N.H. Weste and David Harris. Addison-Wesley, 2005.** (Refer to http://www.cmosvlsi.com)
2. **Principles of CMOS VLSI Design: A Systems Perspective**, Neil H. E. Weste, K. Eshragian, and ??? 3rd edition, Pearson Education (Asia) Pvt. Ltd., 200?. (Shift to the latest edition.)
3. **Basic VLSI Design** - Douglas A. Pucknell & Kamran Eshraghian, PHI 3rd Edition (original Edition – 1994), 2005.

**REFERENCE BOOKS:**

1. R. Jacob Baker. CMOS Circuit Design, Layout and Simulation. John Wiley India Pvt. Ltd, 2008
2. **Fundamentals of Semiconductor Devices**, M. K. Achuthan and K. N. Bhat, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2007.
3. **CMOS Digital Integrated Circuits: Analysis and Design**, Sung-Mo Kang & Yusuf Leblebici, 3rd Edition, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007.
4. **Analysis and Design of Digital Integrated Circuits** - D.A Hodges, H.G Jackson and R.A Saleh. 3rd Edition, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2007.

## DIGITAL SIGNAL PROCESSING LABORATORY

| | | | |
|---|---|---|---|
| Subject Code | : **10ECL57** | IA Marks | : 25 |
| No. of Practical Hrs/Week: 03 | | Exam Hours | : 03 |
| Total no. of Practical Hrs. | : 42 | Exam Marks | : 50 |



DNT

## A LIST OF EXPERIMENTS USING MATLAB / SCILAB / OCTAVE / WAB

1. Verification of Sampling theorem.
2. Impulse response of a given system
3. Linear convolution of two given sequences.
4. Circular convolution of two given sequences
5. Autocorrelation of a given sequence and verification of its properties.
6. Cross correlation of given sequences and verification of its properties.
7. Solving a given difference equation.
8. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum.
9. Linear convolution of two sequences using DFT and IDFT.
10. Circular convolution of two given sequences using DFT and IDFT
11. Design and implementation of FIR filter to meet given specifications.
12. Design and implementation of IIR filter to meet given specifications.

## B. LIST OF EXPERIMENTS USING DSP PROCESSOR

1.Linear convolution of two given sequences.
2.Circular convolution of two given sequences.
3.Computation of N- Point DFT of a given sequence
4.Realization of an FIR filter (any type) to meet given specifications .The input can be a signal from function generator / speech signal.
5.Audio applications such as to plot time and frequency (Spectrum) display of Microphone output plus a cosine using DSP. Read a wav file and match with their respective spectrograms
6.Noise: Add noise above 3kHz and then remove; Interference suppression using 400 Hz tone.
7.Impulse response of first order and second order system

## REFERENCE BOOKS:


1.**Digital signal processing using MATLAB** - Sanjeet Mitra, TMH, 2001

2.**Digital signal processing using MATLAB** - J. G. Proakis & Ingale, MGH, 2000

3.**Digital Signal Processors**, B. Venkataramani and Bhaskar, TMH,2002


## ANALOG COMMUNICATION LAB + LIC LAB

| | | | |
|---|---|---|---|
| Subject Code | : **10ECL58** | IA Marks | : 25 |
| No. of Practical Hrs/Week | : 03 | Exam Hours | : 03 |
| Total no. of Practical Hrs. | : 42 | Exam Marks | : 50 |



D.N.

## A LIST OF EXPERIMENTS USING MATLAB / SCILAB / OCTAVE / WAB

1. Verification of Sampling theorem.
2. Impulse response of a given system
3. Linear convolution of two given sequences.
4. Circular convolution of two given sequences
5. Autocorrelation of a given sequence and verification of its properties.
6. Cross correlation of given sequences and verification of its properties.
7. Solving a given difference equation.
8. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum.
9. Linear convolution of two sequences using DFT and IDFT.
10. Circular convolution of two given sequences using DFT and IDFT
11. Design and implementation of FIR filter to meet given specifications.
12. Design and implementation of IIR filter to meet given specifications.

## B. LIST OF EXPERIMENTS USING DSP PROCESSOR

1.Linear convolution of two given sequences.
2.Circular convolution of two given sequences.
3.Computation of N- Point DFT of a given sequence
4.Realization of an FIR filter (any type) to meet given specifications .The input can be a signal from function generator / speech signal.
5.Audio applications such as to plot time and frequency (Spectrum) display of Microphone output plus a cosine using DSP. Read a wav file and match with their respective spectrograms
6.Noise: Add noise above 3kHz and then remove; Interference suppression using 400 Hz tone.
7.Impulse response of first order and second order system

## REFERENCE BOOKS:


1.**Digital signal processing using MATLAB** - Sanjeet Mitra, TMH, 2001

2.**Digital signal processing using MATLAB** - J. G. Proakis & Ingale, MGH, 2000

3.**Digital Signal Processors**, B. Venkataramani and Bhaskar, TMH,2002


## ANALOG COMMUNICATION LAB + LIC LAB

| | | | |
|---|---|---|---|
| Subject Code | : **10ECL58** | IA Marks | : 25 |
| No. of Practical Hrs/Week | : 03 | Exam Hours | : 03 |
| Total no. of Practical Hrs. | : 42 | Exam Marks | : 50 |



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**EXPERIMENTS USING DESCERTE COMPONENTS and LABVIEW - 2009 CAN BE USED FOR VERIFICATION AND TESTING.**

1. Second order active LPF and HPF
2. Second order active BPF and BE
3. Schmitt Trigger Design and test a Schmitt trigger circuit for the given values of UTP and LTP
4. Frequency synthesis using PLL.
5. Design and test R-2R DAC using op-amp
6. Design and test the following circuits using IC 555
    a. Astable multivibrator for given frequency and duty cycle
    b. Monostable multivibrator for given pulse width W
7. IF amplifier design
8. Amplitude modulation using transistor/FET (Generation and detection)
9. Pulse amplitude modulation and detection
10. PWM and PPM
11. Frequency modulation using 8038/2206
12. Precision rectifiers – both Full Wave and Half Wave.

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VI SEMESTER

## DIGITAL COMMUNICATION

| | | | |
|---|---|---|---|
| Subject Code | : **10EC61** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

Basic signal processing operations in digital communication. Sampling Principles: Sampling Theorem, Quadrature sampling of Band pass signal, Practical aspects of sampling and signal recovery.

**UNIT - 2**

PAM, TDM. Waveform Coding Techniques, PCM, Quantization noise and SNR, robust quantization.

**UNIT - 3**

DPCM, DM, applications. Base-Band Shaping for Data Transmission, Discrete PAM signals, power spectra of discrete PAM signals.

**UNIT - 4**

ISI, Nyquist's criterion for distortion less base-band binary transmission, correlative coding, eye pattern, base-band M-ary PAM systems, adaptive equalization for data transmission.

**UNIT - 5**

**DIGITAL MODULATION TECHNIQUES:** Digital Modulation formats, Coherent binary modulation techniques, Coherent quadrature modulation techniques. Non-coherent binary modulation techniques.

**UNIT - 6**

Detection and estimation, Model of DCS, Gram-Schmidt Orthogonalization procedure, geometric interpretation of signals, response of bank of correlators to noisy input.

**UNIT - 7**

Detection of known signals in noise, correlation receiver, matched filter receiver, detection of signals with unknown phase in noise.

**UNIT - 8**

Spread Spectrum Modulation: Pseudo noise sequences, notion of spread spectrum, direct sequence spread spectrum, coherent binary PSK, frequency



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hop spread spectrum, applications.

**TEXT BOOK:**

1. **Digital communications**, Simon Haykin, John Wiley India Pvt. Ltd, 2008.

**REFERENCE BOOKS:**

1. **Digital and Analog communication systems,** Simon Haykin, John Wildy India Lts, 2008
2. **An introduction to Analog and Digital Communication,** K. Sam Shanmugam, John Wiley India Pvt. Ltd, 2008.
3. **Digital communications** - Bernard Sklar: Pearson education 2007

## MICROPROCESSOR

| | | | |
|---|---|---|---|
| Subject Code | : **10EC62** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

**8086 PROCESSORS:** Historical background, The microprocessor-based personal computer system, 8086 CPU Architecture, Machine language instructions, Instruction execution timing, The 8086

**UNIT - 2**

**INSTRUCTION SET OF 8086:** Assembler instruction format, data transfer and arithmetic, branch type, loop, NOP & HALT, flag manipulation, logical and shift and rotate instructions. Illustration of these instructions with example programs, Directives and operators

**UNIT - 3**

**BYTE AND STRING MANIPULATION:** String instructions, REP Prefix, Table translation, Number format conversions, Procedures, Macros, Programming using keyboard and video display

**UNIT - 4**

**8086 INTERRUPTS:** 8086 Interrupts and interrupt responses, Hardware interrupt applications, Software interrupt applications, Interrupt examples

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**UNIT - 5**

**8086 INTERFACING**: Interfacing microprocessor to keyboard (keyboard types, keyboard circuit connections and interfacing, software keyboard interfacing, keyboard interfacing with hardware), Interfacing to alphanumeric displays (interfacing LED displays to microcomputer), Interfacing a microcomputer to a stepper motor

**UNIT - 6**

**8086 BASED MULTIPROCESSING SYSTEMS:** Coprocessor configurations, The 8087 numeric data processor: data types, processor architecture, instruction set and examples

**UNIT - 7**

**SYSTEM BUS STRUCTURE:** Basic 8086 configurations: minimum mode, maximum mode, Bus Interface: peripheral component interconnect (PCI) bus, the parallel printer interface (LPT), the universal serial bus (USB)

**UNIT - 8**

**80386, 80486 AND PENTIUM PROCESSORS:** Introduction to the 80386 microprocessor, Special 80386 registers, Introduction to the 80486 microprocessor, Introduction to the Pentium microprocessor.

**TEXT BOOKS:**

1. **Microcomputer systems-The 8086 / 8088** Family – Y.C. Liu and G. A. Gibson, 2E PHI -2003
2. **The Intel Microprocessor, Architecture, Programming and Interfacing**-Barry B. Brey, 6e, Pearson Education / PHI, 2003

**REFERENCE BOOKS:**

1. **Microprocessor and Interfacing- Programming & Hardware**, Douglas hall, 2nd , TMH, 2006.
2. **Advanced Microprocessors and Peripherals** - A.K. Ray and K.M. Bhurchandi, TMH, 2nd , 2006.
3. **8088 and 8086 Microprocessors - Programming, Interfacing, Software, Hardware & Applications** - Triebel and Avtar Singh, 4e, Pearson Education, 2003

## MICROELECTRONICS CIRCUITS

| | | | |
|---|---|---|---|
| Subject Code | : **10EC63** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |



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**UNIT – 1**

**MOSFETS:** Device Structure and Physical Operation, V-I Characteristics, MOSFET Circuits at DC, Biasing in MOS amplifier Circuits, Small Signal Operation and Models, MOSFET as an amplifier and as a switch, biasing in MOS amplifier circuits, small signal operation modes, single stage MOS amplifiers. MOSFET internal capacitances and high frequency modes, Frequency response of CS amplifiers, CMOS digital logic inverter, detection type MOSFET.

**UNIT -2**

**Single Stage IC Amplifier:** IC Design philiosophy, CoUmparison of MOSFET and BJT, Current sources, Current mirrors and Current steering circuits, high frequency response.

**UNIT – 3**

**Single Stage IC amplifiers** (continued): CS and CF amplifiers with loads, high frequency response of CS and CF amplifiers, CG and CB amplifiers with active loads, high frequency response of CG and CB amplifiers, Cascade amplifiers. CS and CE amplifiers with source ( emitter) degeneration source and emitter followers, some useful transfer parings, current mirrors with improved performance. SPICE examples.

**UNIT – 4**

**Differences and Multistage Amplifiers:** The MOS differential pair, small signal operation of MOS differential pair, the BJT differences pair, other non-ideal characteristics and differential pair, Differential amplifier with active loads, frequency response and differential amplifiers. Multistage amplifier. SPICE examples.

**UNIT – 5**

**Feedback**. General Feedback structure. Properties of negative feedback. Four basic feedback topologies. Series-Shunt feedback. Determining the loop gain. Stability problem. Effect of feedback an amplifier poles. Stability study using Bode plots. Frequency compensation. SPICE examples.

**UNIT - 6**

**Operational Amplifiers:** The two stage CMOS Op-amp, folded cascade CMOS op-amp, 741 op-amp circuit, DC analysis of the 741, small signal analysis of 741, gain, frequency response and slew rate of 741. Data Converters. A-D and D-A converters.

**UNIT – 7 & 8**

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**Digital CMOS circuits**. Overview. Design and performance analysis of CMOS inverter. Logic Gate Circuits. Pass-transistor logic. Dynamic Logic Circuits. SPICE examples.

**Text Book:**

1. **"Microelectronic Circuits"**, Adel Sedra and K.C. Smith, 5th Edition, Oxford University Press, Interantional Version, 2009.

**Reference Book:**

1. "**Fundamentals of Microelectronics**" , Behzad Razavi, John Wiley India Pvt. Ltd, 2008.
2. **"Microelectronics – Analysis and Design"**, Sundaram Natarajan, Tata McGraw-Hill, 2007

## ANTENNAS AND PROPAGATION

| | | | |
|---|---|---|---|
| Subject Code | : **10EC64** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

**ANTENNA BASICS:** Introduction, basic Antenna parameters, patterns, beam area, radiation intensity, beam efficiency, diversity and gain, antenna apertures, effective height, bandwidth, radiation, efficiency, antenna temperature and antenna filed zones.

**UNIT - 2**

**POINT SOURCES AND ARRAYS:** Introduction, point sources, power patterns, power theorem, radiation intensity, filed patterns, phase patterns. Array of two isotropic point sources. Endfire array and Broadside array.

**UNIT - 3**

**ELECTRIC DIPOLES AND THIN LINEAR ANTENNAS:** Introduction, short electric dipole, fields of a short dipole(no derivation of field components), radiation resistance of short dipole, radiation resistances of lambda/2 Antenna, thin linear antenna, micro strip arrays, low side lobe arrays, long wire antenna, folded dipole antennas.

**UNIT - 4 & 5**

**LOOP, SLOT, PATCH AND HORN ANTENNA:** Introduction, small loop, comparison of far fields of small loop and short dipole, loop antenna general case, far field patterns of circular loop, radiation resistance, directivity, slot antenna, Babinet's principle and complementary antennas,



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hop spread spectrum, applications

**TEXT BOOK:**

1. **Digital communications**, Simon Haykin, John Wiley India Pvt. Ltd. 2008.

**REFERENCE BOOKS:**

1. **Digital and Analog communication systems**, Simon Haykin, John Wildy India Lts, 2008
2. **An introduction to Analog and Digital Communication**, K. Sam Shanmugam, John Wiley India Pvt. Ltd, 2008.
3. **Digital communications** - Bernard Sklar Pearson education 2007

## MICROPROCESSOR

| | | | |
|---|---|---|---|
| Subject Code | : **10EC62** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

**8086 PROCESSORS:** Historical background, The microprocessor-based personal computer system, 8086 CPU Architecture, Machine language instructions, Instruction execution timing, The 8086

**UNIT - 2**

**INSTRUCTION SET OF 8086:** Assembler instruction format, data transfer and arithmetic, branch type, loop, NOP & HALT, flag manipulation, logical and shift and rotate instructions. Illustration of these instructions with example programs, Directives and operators

**UNIT - 3**

**BYTE AND STRING MANIPULATION:** String instructions, REP Prefix, Table translation, Number format conversions, Procedures, Macros, Programming using keyboard and video display

**UNIT - 4**

**8086 INTERRUPTS:** 8086 Interrupts and interrupt responses, Hardware interrupt applications, Software interrupt applications, Interrupt examples

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**UNIT - 5**

**8086 INTERFACING**: Interfacing microprocessor to keyboard (keyboard types, keyboard circuit connections and interfacing, software keyboard interfacing, keyboard interfacing with hardware), Interfacing to alphanumeric displays (interfacing LED displays to microcomputer), Interfacing a microcomputer to a stepper motor

**UNIT - 6**

**8086 BASED MULTIPROCESSING SYSTEMS:** Coprocessor configurations, The 8087 numeric data processor: data types, processor architecture, instruction set and examples

**UNIT - 7**

**SYSTEM BUS STRUCTURE:** Basic 8086 configurations: minimum mode, maximum mode, Bus Interface: peripheral component interconnect (PCI) bus, the parallel printer interface (LPT), the universal serial bus (USB)

**UNIT - 8**

**80386, 80486 AND PENTIUM PROCESSORS:** Introduction to the 80386 microprocessor, Special 80386 registers, Introduction to the 80486 microprocessor, Introduction to the Pentium microprocessor.

**TEXT BOOKS:**

1. **Microcomputer systems-The 8086 / 8088** Family – Y.C. Liu and G. A. Gibson, 2E PHI -2003
2. **The Intel Microprocessor, Architecture, Programming and Interfacing**-Barry B. Brey, 6e, Pearson Education / PHI, 2003

**REFERENCE BOOKS:**

1. **Microprocessor and Interfacing- Programming & Hardware**, Douglas hall, 2nd , TMH, 2006.
2. **Advanced Microprocessors and Peripherals** - A.K. Ray and K.M. Bhurchandi, TMH, 2nd , 2006.
3. **8088 and 8086 Microprocessors - Programming, Interfacing, Software, Hardware & Applications** - Triebel and Avtar Singh, 4e, Pearson Education, 2003

## MICROELECTRONICS CIRCUITS

| | | | |
|---|---|---|---|
| Subject Code | : **10EC63** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |



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impedance of complementary and slot antennas, patch antennas, horn antennas, rectangular horn antennas.

**UNIT - 6**

**ANTENNA TYPES:** Helical Antenna, Yagi-Uda array, corner reflectors, parabolic reflectors, log periodic antenna, lens antenna, antenna for special applications – sleeve antenna, turnstile antenna, omni directional antennas, antennas for satellite antennas for ground penetrating radars, embedded antennas, ultra wide band antennas, plasma antenna, high-resolution data, intelligent antennas, antenna for remote sensing.

**UNIT - 7 & 8**

**RADIO WAVE PROPAGATION:** Introduction, Ground wave propagation, free space propagation, ground reflection, surface wave, diffraction.
**TROPOSPHERE WAVE PROPAGATION:** Troposcopic scatter, Ionosphere propagation, electrical properties of the ionosphere, effects of earth's magnetic field.

**TEXT BOOKS:**

1. **Antennas and Wave Propagation**, John D. Krauss, 4th Edn,McGraw-Hill International edition, 2010.
2. **Antennas and Wave Propagation** - Harish and Sachidananda: Oxford Press 2007

**REFERENCE BOOKS:**

1. **Antenna Theory Analysis and Design** - C A Balanis, 3rd Edn, John Wiley India Pvt. Ltd, 2008
2. **Antennas and Propagation for Wireless Communication Systems** - Sineon R Saunders, John Wiley, 2003.
3. **Antennas and wave propagation** - G S N Raju: Pearson Education 2005

## OPERATING SYSTEMS

| | | | |
|---|---|---|---|
| Subject Code | : **10EC65** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

**INTRODUCTION AND OVERVIEW OF OPERATING SYSTEMS:** Operating system, Goals of an O.S, Operation of an O.S, Resource allocation and related functions, User interface related functions, Classes of operating



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systems, O.S and the computer system, Batch processing system, Multi programming systems, Time sharing systems, Real time operating systems, distributed operating systems.

**UNIT - 2**

**STRUCTURE OF THE OPERATING SYSTEMS:** Operation of an O.S, Structure of the supervisor, Configuring and installing of the supervisor, Operating system with monolithic structure, layered design, Virtual machine operating systems, Kernel based operating systems, and Microkernel based operating systems.

**UNIT - 3**

**PROCESS MANAGEMENT:** Process concept, Programmer view of processes, OS view of processes, Interacting processes, Threads, Processes in UNIX, Threads in Solaris.

**UNIT - 4**

**MEMORY MANAGEMENT:** Memory allocation to programs, Memory allocation preliminaries, Contiguous and noncontiguous allocation to programs, Memory allocation for program controlled data, kernel memory allocation.

**UNIT - 5**

**VIRTUAL MEMORY:** Virtual memory basics, Virtual memory using paging, Demand paging, Page replacement, Page replacement policies, Memory allocation to programs, Page sharing, UNIX virtual memory.

**UNIT - 6**

**FILE SYSTEMS:** File system and IOCS, Files and directories, Overview of I/O organization, Fundamental file organizations, Interface between file system and IOCS, Allocation of disk space, Implementing file access, UNIX file system.

**UNIT - 7**

**SCHEDULING:** Fundamentals of scheduling, Long-term scheduling, Medium and short term scheduling, Real time scheduling, Process scheduling in UNIX.

**UNIT - 8**

**MESSAGE PASSING:** Implementing message passing, Mailboxes, Inter process communication in UNIX.

**TEXT BOOK:**

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1. **"Operating Systems - A Concept based Approach"**, D. M. Dhamdhare, TMH, 3rd Ed, 2010.

**REFERENCE BOOK:**

1. **Operating Systems Concepts**, Silberschatz and Galvin, John Wiley India Pvt. Ltd, 5th Edition, 2001.
2. **Operating System – Internals and Design Systems**, Willaim Stalling, Pearson Education, 4th Ed, 2006.
3. **Design of Operating Systems,** Tennambhaum, TMH, 2001.

## ADVANCED COMMUNICATION LAB

| | | | |
|---|---|---|---|
| Subject Code | : **10ECL67** | IA Marks | : 25 |
| No. of Practical Hrs/Week: 03 | | Exam Hours | : 03 |
| Total no. of Practical Hrs. : 42 | | Exam Marks | : 50 |

**LIST OF EXPERIMENTS USING DESCERTE COMPONENTS and LABVIEW – 2009 can be used for verification and testing.**

1. TDM of two band limited signals.
2. ASK and FSK generation and detection
3. PSK generation and detection
4. DPSK generation and detection
5. QPSK generation and detection
6. PCM generation and detection using a CODEC Chip
7. Measurement of losses in a given optical fiber ( propagation loss, bending loss) and numerical aperture
8. Analog and Digital (with TDM) communication link using optical fiber.
9. Measurement of frequency, guide wavelength, power, VSWR and attenuation in a microwave test bench
10. Measurement of directivity and gain of antennas: Standard dipole (or printed dipole), microstrip patch antenna and Yagi antenna (printed).
11. Determination of coupling and isolation characteristics of a stripline (or microstrip) directional coupler
12. (a) Measurement of resonance characteristics of a microstrip ring resonator and determination of dielectric constant of the substrate.



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(b) Measurement of power division and isolation characteristics of a microstrip 3 dB power divider.

## MICROPROCESSOR LAB

| | | | |
|---|---|---|---|
| Subject Code | : **10ECL68** | IA Marks | : 25 |
| No. of Practical Hrs/Week: 03 | | Exam Hours | : 03 |
| Total no. of Practical Hrs. : 42 | | Exam Marks | : 50 |

I) **Programs involving**

1) Data transfer instructions like:
   - i] Byte and word data transfer in different addressing modes.
   - ii] Block move (with and without overlap)
   - iii] Block interchange

2) Arithmetic & logical operations like:
   - i] Addition and Subtraction of multi precision nos.
   - ii] Multiplication and Division of signed and unsigned Hexadecimal nos.
   - iii] ASCII adjustment instructions
   - iv] Code conversions
   - v] Arithmetic programs to find square cube, LCM, GCD, factorial

3) Bit manipulation instructions like checking:
   - i] Whether given data is positive or negative
   - ii] Whether given data is odd or even
   - iii] Logical 1's and 0's in a given data
   - iv] 2 out 5 code
   - v] Bit wise and nibble wise palindrome

4) Branch/Loop instructions like:
   - i] Arrays: addition/subtraction of N nos.
     Finding largest and smallest nos.
     Ascending and descending order
   - ii] Near and Far Conditional and Unconditional jumps, Calls and Returns

5) Programs on String manipulation like string transfer, string reversing, searching for a string, etc.

6) Programs involving Software interrupts
Programs to use DOS interrupt INT 21h Function calls for Reading a Character from keyboard, Buffered Keyboard input, Display of character/ String on console

II) Experiments on interfacing 8086 with the following interfacing modules through DIO (Digital Input/Output-PCI bus compatible) card
a) Matrix keyboard interfacing
b) Seven segment display interface
c) Logical controller interface
d) Stepper motor interface

III) Other Interfacing Programs
a) Interfacing a printer to an X86 microcomputer
b) PC to PC Communication

## ELECTIVE – GROUP A
## ANALOG AND MIXED MODE VLSI DESIGN

| | | | |
|---|---|---|---|
| Subject Code | : **10EC661** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

(Text Book 1)

**UNIT 1**
Data converter fundamentals: Analog versus Digital Discrete Time Signals, Converting Analog Signals to Data Signals, Sample and Hold Characteristics, DAC Specifications, ADC Specifications, Mixed-Signal Layout Issues.

**UNIT 2**
Data Converters Architectures: DAC Architectures, Digital Input Code, Resistors String, R-2R Ladder Networks, Current Steering, Charge Scaling DACs, Cyclic DAC, Pipeline DAC, ADC Architectures, Flash, 2-Step Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC.

**UNIT 3**
Non-Linear Analog Circuits: Basic CMOS Comparator Design (Excluding Characterization), Analog Multipliers, Multiplying Quad (Excluding Stimulation), Level Shifting (Excluding Input Level Shifting For Multiplier).

(Text Book 2)

**UNIT 4:**
Data Converter SNR: Improving SNR Using Averaging (Excluding Jitter & Averaging onwards), Decimating Filters for ADCs (Excluding Decimating



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without Averaging onwards), Interpolating Filters for DAC, Band pass and High pass Sync filters.

**UNIT 5**

Su-Microns CMOS circuit design: Process Flow, Capacitors and Resistors, MOSFET Switch (upto Bidirectional Switches), Delay and adder Elements, Analog Circuits MOSFET Biasing (upto MOSFET Transition Frequency).

**UNIT 6**

OPAmp Design (Excluding Circuits Noise onwards)

**TEXT BOOK:**

1. **Design, Layout, Stimulation ,**R. Jacob Baker, Harry W Li, David E Boyce, CMOS Circuit, PHI Education, 2005

2. **CMOS- Mixed Signal Circuit Design ,**R. Jacob Baker, (Vol II of CMOS: Circuit Design, Layout and Stimulation), John Wiley India Pvt. Ltd, 2008.

**REFERENCE BOOKS:**

1. **Design of Analog CMOS Integrated Circuits**, B Razavi, First Edition, McGraw Hill,2001.

2. **CMOS Analog Circuit Design**, P e Allen and D R Holberg, 2nd Edition, Oxford University Press,2002.

## SATELLITE COMMUNICATION

| | | | |
|---|---|---|---|
| Subject Code | : **10EC662** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |



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without Averaging onwards), Interpolating Filters for DAC, Band pass and High pass Sync filters.

**UNIT 5**

Su-Microns CMOS circuit design: Process Flow, Capacitors and Resistors, MOSFET Switch (upto Bidirectional Switches), Delay and adder Elements, Analog Circuits MOSFET Biasing (upto MOSFET Transition Frequency).

**UNIT 6**

OPAmp Design (Excluding Circuits Noise onwards)

**TEXT BOOK:**

1. **Design, Layout, Stimulation ,**R. Jacob Baker, Harry W Li, David E Boyce, CMOS Circuit, PHI Education, 2005

2. **CMOS- Mixed Signal Circuit Design ,**R. Jacob Baker, (Vol II of CMOS: Circuit Design, Layout and Stimulation), John Wiley India Pvt. Ltd, 2008.

**REFERENCE BOOKS:**

1. **Design of Analog CMOS Integrated Circuits**, B Razavi, First Edition, McGraw Hill,2001.

2. **CMOS Analog Circuit Design**, P e Allen and D R Holberg, 2nd Edition, Oxford University Press,2002.

## SATELLITE COMMUNICATION

| | | | |
|---|---|---|---|
| Subject Code | : **10EC662** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |



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Total no. of Lecture Hrs. : 52 Exam Marks : 100

**UNIT - 1**

**OVER VIEW OF SATELLITE SYSTEMS:** Introduction, frequency allocation, INTEL Sat.

**UNIT - 2**

**ORBITS:** Introduction, Kepler laws, definitions, orbital element, apogee and perigee heights, orbit perturbations, inclined orbits, calendars, universal time, sidereal time, orbital plane, local mean time and sun synchronous orbits, Geostationary orbit: Introduction, antenna, look angles, polar mix antenna, limits of visibility, earth eclipse of satellite, sun transit outage, leandiag orbits.

**UNIT - 3**

**PROPAGATION IMPAIRMENTS AND SPACE LINK:** Introduction, atmospheric loss, ionospheric effects, rain attenuation, other impairments.
**SPACE LINK:** Introduction, EIRP, transmission losses, link power budget, system noise, CNR, uplink, down link, effects of rain, combined CNR.

**UNIT - 4**

**SPACE SEGMENT:** Introduction, power supply units, altitude control, station keeping, thermal control, TT&C, transponders, antenna subsystem.

**UNIT - 5 & 6**

**EARTH SEGEMENT:** Introduction, receive only home TV system, out door unit, indoor unit, MATV, CATV, Tx – Rx earth station.

**INTERFERENCE AND SATELLITE ACCESS:** Introduction, interference between satellite circuits, satellite access, single access, pre-assigned FDMA, SCPC (spade system), TDMA, pre-assigned TDMA, demand assigned TDMA, down link analysis, comparison of uplink power requirements for TDMA & FDMA, on board signal processing satellite switched TDMA.

**UNIT - 7 & 8**

**DBS, SATELLITE MOBILE AND SPECIALIZED SERVICES:** Introduction, orbital spacing, power ratio, frequency and polarization, transponder capacity, bit rates for digital TV, satellite mobile services, USAT, RadarSat, GPS, orb communication and Indian Satellite systems.



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**TEXT BOOK:**

1. **Satellite Communications**, Dennis Roddy, 4th Edition, McGraw-Hill International edition, 2006.

**REFERENCES BOOKS:**

1. **Satellite Communications**, Timothy Pratt, Charles Bostian and Jeremy Allnutt, 2nd Edition, John Wiley Pvt. Ltd & Sons, 2008.
2. **Satellite Communication Systems Engineering**, W. L. Pitchand, H. L. Suyderhoud, R. A. Nelson, 2nd Ed., Pearson Education., 2007.

## RANDOM PROCESSES

| | | | |
|---|---|---|---|
| Subject Code | : **10EC663** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

**INTRODUCTION TO PROBABILITY THEORY:** Experiments, sample space, Events, Axioms, Assigning probabilities, Joint and conditional probabilities, Baye's Theorem, Independence, Discrete Random Variables, Engg Example.

**UNIT - 2**

**Random Variables, Distributions, Density Functions:** CDF, PDF, Gaussian random variable, Uniform Exponential, Laplace, Gamma, Erlang, Chi-Square, Raleigh, Rician and Cauchy types of random variables

**UNIT - 3**

**OPERATIONS ON A SINGLE R V:** Expected value, EV of Random variables, EV of functions of Random variables, Central Moments, Conditional expected values.

**UNIT - 4**

Characteristic functions, Probability generating functions, Moment generating functions, Engg applications, Scalar quantization, entropy and source coding.

**UNIT - 5**

Pairs of Random variables, Joint CDF, joint PDF, Joint probability mass functions, Conditional Distribution, density and mass functions, EV



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(b) Measurement of power division and isolation characteristics of a microstrip 3 dB power divider.

## MICROPROCESSOR LAB

| | | | |
|---|---|---|---|
| Subject Code | : **10ECL68** | IA Marks | : 25 |
| No. of Practical Hrs/Week: 03 | | Exam Hours | : 03 |
| Total no. of Practical Hrs. : 42 | | Exam Marks | : 50 |

I) **Programs involving**

1) Data transfer instructions like:
   - i] Byte and word data transfer in different addressing modes.
   - ii] Block move (with and without overlap)
   - iii] Block interchange

2) Arithmetic & logical operations like:
   - i] Addition and Subtraction of multi precision nos.
   - ii] Multiplication and Division of signed and unsigned Hexadecimal nos.
   - iii] ASCII adjustment instructions
   - iv] Code conversions
   - v] Arithmetic programs to find square cube, LCM, GCD, factorial

3) Bit manipulation instructions like checking:
   - i] Whether given data is positive or negative
   - ii] Whether given data is odd or even
   - iii] Logical 1's and 0's in a given data
   - iv] 2 out 5 code
   - v] Bit wise and nibble wise palindrome

4) Branch/Loop instructions like:
   - i] Arrays: addition/subtraction of N nos.
     Finding largest and smallest nos.
     Ascending and descending order
   - ii] Near and Far Conditional and Unconditional jumps, Calls and Returns

5) Programs on String manipulation like string transfer, string reversing, searching for a string, etc.



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6) Programs involving Software interrupts
Programs to use DOS interrupt INT 21h Function calls for Reading a Character from keyboard, Buffered Keyboard input, Display of character/ String on console

II) Experiments on interfacing 8086 with the following interfacing modules through DIO (Digital Input/Output-PCI bus compatible) card
   a) Matrix keyboard interfacing
   b) Seven segment display interface
   c) Logical controller interface
   d) Stepper motor interface

III) Other Interfacing Programs
   a) Interfacing a printer to an X86 microcomputer
   b) PC to PC Communication

## ELECTIVE – GROUP A
## ANALOG AND MIXED MODE VLSI DESIGN

| | | | |
|---|---|---|---|
| Subject Code | : 10EC661 | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

(Text Book 1)

**UNIT 1**

Data converter fundamentals: Analog versus Digital Discrete Time Signals, Converting Analog Signals to Data Signals, Sample and Hold Characteristics, DAC Specifications, ADC Specifications, Mixed-Signal Layout Issues.

**UNIT 2**

Data Converters Architectures: DAC Architectures, Digital Input Code, Resistors String, R-2R Ladder Networks, Current Steering, Charge Scaling DACs, Cyclic DAC, Pipeline DAC, ADC Architectures, Flash, 2-Step Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC.

**UNIT 3**

Non-Linear Analog Circuits: Basic CMOS Comparator Design (Excluding Characterization), Analog Multipliers, Multiplying Quad (Excluding Stimulation), Level Shifting (Excluding Input Level Shifting For Multiplier).

(Text Book 2)

**UNIT 4:**

Data Converter SNR: Improving SNR Using Averaging (Excluding Jitter & Averaging onwards), Decimating Filters for ADCs (Excluding Decimating



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Resolution and sampling frequency – Multiplexing of analog inputs – Single-ended and differential inputs – Different strategies for sampling of multi channel analog inputs. Concept of universal DAQ card – Use of timer-counter and analog outputs on the universal DAQ card.

**UNIT 3**

**Cluster of Instruments in System:** Interfacing of external instruments to a PC – RS 232C, RS – 422, RS 485 and USB standards – IEEE 488 standard – ISO –OSI model for series bus – introduction to bus protocols of MOD bus and CAN bus.

**UNIT 4**

**Graphical Programming Environment in VI:** Concepts of graphical programming – Lab-view software – Concept of VIs and sub VIs – Display types – Digital – Analog – Chart – Oscilloscope types – Loops – Case and sequence structures – Types of data – Arrays – Formulate nodes – Local and Global variables – String and file I/O.

**UNIT 5**

**Analysis Tools and Simple Application in VI:** Fourier transform – Power spectrum – Correlation – Windowing and filtering tools – Simple temperature indicator – ON/OFF controller – PID controller – CRO emulation – Simulation of a simple second order system – Generation of HTML page.

**Reference Books:**


1. S. Gupta and J P Gupta,"**PC Interfacing for Data Acquisition and Process Control"**, Instrument Society of America, 1994
2. Peter W Gofton , "**Understanding Serial Communication**", Sybes International, 2000
3. Robert H. Bishop, "**Learning with Lab-View**" Preticee Hall, 2009
4. Sanjay Gupta, "**Virtual Instrumentation, LABVIEW"**, TMH, New Delhi, 2003
5. Ernest O. Doeblin and Dhanesh N Manik, " **Measrement Systems – Application and Design"**, 5th Edn, TMH, 2007.


## VII SEMESTER

## COMPUTER COMMUNICATION NETWORKS

| | | | |
|---|---|---|---|
| Subject Code | : **10EC71** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |



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**UNIT - 1**

Layered tasks, OSI Model, Layers in OSI model, TCP?IP Suite, Addressing, Telephone and cable networks for data transmission, Telephone networks, Dial up modem, DSL, Cable TV for data transmission.

**UNIT - 2**

**DATA LINK CONTROL:** Framing, Flow and error control, Protocols, Noiseless channels and noisy channels, HDLC.

**UNIT - 3**

**MULTIPLE ACCESSES:** Random access, Controlled access, Channelisation.

**UNIT - 4**

Wired LAN, Ethernet, IEEE standards, Standard Ethernet. Changes in the standards, Fast Ethernet, Gigabit Ethernet, Wireless LAN IEEE 802.11

**UNIT - 5**

Connecting LANs, Backbone and Virtual LANs, Connecting devices, Back bone Networks, Virtual LANs

**UNIT - 6**

Network Layer, Logical addressing, Ipv4 addresses, Ipv6 addresses, Ipv4 and Ipv6 Transition from Ipv4 to Ipv6.

**UNIT - 7**

Delivery, Forwarding, Unicast Routing Protocols, Multicast Routing protocols

**UNIT - 8**

Transport layer Process to process Delivery, UDP, TCP, Domain name system, Resolution

**TEXT BOOK:**

1. **Data Communication and Networking**, B Forouzan, 4th Ed, TMH 2006

**REFERENCE BOOKS:**



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1. **Computer Networks**, James F. Kurose, Keith W. Ross: Pearson education, 2nd Edition, 2003
2. **Introduction to Data communication and Networking**, Wayne Tomasi: Pearson education 2007

## OPTICAL FIBER COMMUNICATION

| | | | |
|---|---|---|---|
| Subject Code | : **10EC72** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

**OVERVIEW OF OPTICAL FIBER COMMUNICATION:** Introduction, Historical development, general system, advantages, disadvantages, and applications of optical fiber communication, optical fiber waveguides, Ray theory, cylindrical fiber (no derivations in article 2.4.4), single mode fiber, cutoff wave length, mode filed diameter. Optical Fibers: fiber materials, photonic crystal, fiber optic cables specialty fibers.

**UNIT - 2**

**TRANSMISSION CHARACTERISTICS OF OPTICAL FIBERS:** Introduction, Attenuation, absorption, scattering losses, bending loss, dispersion, Intra model dispersion, Inter model dispersion.

**UNIT - 3**

**OPTICAL SOURCES AND DETECTORS:** Introduction, LED's, LASER diodes, Photo detectors, Photo detector noise, Response time, double hetero junction structure, Photo diodes, comparison of photo detectors.

**UNIT - 4**

**FIBER COUPLERS AND CONNECTORS:** Introduction, fiber alignment and joint loss, single mode fiber joints, fiber splices, fiber connectors and fiber couplers.

**UNIT - 5**

**OPTICAL RECEIVER:** Introduction, Optical Receiver Operation, receiver sensitivity, quantum limit, eye diagrams, coherent detection, burst mode receiver, operation, Analog receivers

**UNIT - 6**



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**ANALOG AND DIGITAL LINKS:** Analog links – Introduction, overview of analog links, CNR, multichannel transmission techniques, RF over fiber, key link parameters, Radio over fiber links, microwave photonics.
Digital links – Introduction, point–to–point links, System considerations, link power budget, resistive budget, short wave length band, transmission distance for single mode fibers, Power penalties, nodal noise and chirping.

**UNIT - 7**

**WDM CONCEPTS AND COMPONENTS:** WDM concepts, overview of WDM operation principles, WDM standards, Mach-Zehender interferometer, multiplexer, Isolators and circulators, direct thin film filters, active optical components, MEMS technology, variable optical attenuators, tunable optical fibers, dynamic gain equalizers, optical drop multiplexers, polarization controllers, chromatic dispersion compensators, tunable light sources.

**UNIT - 8**

Optical Amplifiers and Networks – optical amplifiers, basic applications and types, semiconductor optical amplifiers, EDFA.
**OPTICAL NETWORKS:** Introduction, SONET / SDH, Optical Interfaces, SONET/SDH rings, High – speed light – waveguides.

**TEXT BOOKS:**

1. **"Optical Fiber Communication"**, Gerd Keiser, 4th Ed., MGH, 2008.
2. **"Optical Fiber Communications"**, John M. Senior, Pearson Education. 3rd Impression, 2007.

**REFERENCE BOOK:**

1. **Fiber Optic Communication** - Joseph C Palais: 4th Edition, Pearson Education.

## POWER ELECTRONICS

| | | | |
|---|---|---|---|
| Subject Code | : **10EC73** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

Introduction, Applications of power electronics, Power semiconductor devices, Control characteristics, Types of power electronics circuits, Peripheral effects.



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**UNIT - 2**

**POWER TRANSISTOR:** Power BJT's, Switching characteristics, Switching limits, Base derive control, Power MOSFET's, Switching characteristics, Gate drive, IGBT's, Isolation of gate and base drives.

**UNIT - 3**

**INTRODUCTION TO THYRISTORS:** Principle of operation states anode-cathode characteristics, Two transistor model. Turn-on Methods, Dynamic Turn-on and turn-off characteristics, Gate characteristics, Gate trigger circuits, di / dt and dv / dt protection, Thyristor firing circuits.

**UNIT - 4**

**CONTROLLED RECTIFIERS:** Introduction, Principles of phase controlled converter operation, 1φ fully controlled converters, Duel converters, 1 φ semi converters (all converters with R & RL load).

**UNIT - 5**

Thyristor turn off methods, natural and forced commutation, self commutation, class A and class B types, Complementary commutation, auxiliary commutation, external pulse commutation, AC line commutation, numerical problems.

**UNIT - 6**

**AC VOLTAGE CONTROLLERS:** Introduction, Principles of on and off control, Principles of phase control, Single phase controllers with restive loads and Inductive loads, numerical problems.

**UNIT - 7**

**DC CHOPPERS:** Introduction, Principles of step down and step up choppers, Step down chopper with RL loads, Chopper classification, Switch mode regulators – buck, boost and buck – boost regulators.

**UNIT - 8**

**INVERTORS:** Introduction, Principles of operation, Performance parameters, 1φ bridge inverter, voltage control of 1φ invertors, current source invertors, Variable DC link inverter.

**TEXT BOOKS:**



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1. **"Power Electronics"** - M. H. Rashid 3rd edition, PHI / Pearson publisher 2004.
2. **"Power Electronics"** - M. D. Singh and Kanchandani K.B. TMH publisher, 2nd Ed. 2007.

**REFERENCE BOOKS:**

1. **"Power Electronics, Essentials and Applications", L Umanand,** John Wiley India Pvt. Ltd, 2009.
2. **"Power Electronics"** , Daniel W. Hart, McGraw Hill, 2010.
3. **"Power Electronics"**, V Nattarasu and R.S. Anandamurhty, Pearson/Sanguine Pub. 2006.

## EMBEDDED SYSTEM DESIGN

| | | | |
|---|---|---|---|
| Subject Code | : **10EC74** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT 1:**

**Introduction to Embedded System:** Introducing Embedded Systems, Philosophy, Embedded Systems, Embedded Design and Development Process.

**UNIT 2:**

**The Hardware Side**: An Introduction, The Core Level, Representing Information, Understanding Numbers, Addresses, Instructions, Registers-A First Look, Embedded Systems-An Instruction Set View, Embedded Systems-A Register View, Register View of a Microprocessor
The Hardware Side: Storage Elements and Finite-State Machines (2 hour) The concepts of State and Time, The State Diagram, Finite State Machines-A Theoretical Model.

**UNIT 3:**

**Memories and the Memory Subsystem**: Classifying Memory, A General Memory Interface, ROM Overview, Static RAM Overview, Dynamic RAM Overview, Chip Organization, Terminology, A Memory Interface in Detail, SRAM Design, DRAM Design, DRAM Memory Interface, The Memory Map, Memory Subsystem Architecture, Basic Concepts of Caching, Designing a Cache System, Dynamic Memory Allocation.

**UNIT 4:**

**Embedded Systems Design and Development** : System Design and Development, Life-cycle Models, Problem Solving-Five Steps to Design, The



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1. **"Power Electronics"** - M. H. Rashid 3rd edition, PHI / Pearson publisher 2004.
2. **"Power Electronics"** - M. D. Singh and Kanchandani K.B. TMH publisher, 2nd Ed. 2007.

**REFERENCE BOOKS:**

1. **"Power Electronics, Essentials and Applications", L Umanand,** John Wiley India Pvt. Ltd, 2009.
2. **"Power Electronics"** , Daniel W. Hart, McGraw Hill, 2010.
3. **"Power Electronics"**, V Nattarasu and R.S. Anandamurhty, Pearson/Sanguine Pub. 2006.

## EMBEDDED SYSTEM DESIGN

| | | | |
|---|---|---|---|
| Subject Code | : **10EC74** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT 1:**

**Introduction to Embedded System:** Introducing Embedded Systems, Philosophy, Embedded Systems, Embedded Design and Development Process.

**UNIT 2:**

**The Hardware Side**: An Introduction, The Core Level, Representing Information, Understanding Numbers, Addresses, Instructions, Registers-A First Look, Embedded Systems-An Instruction Set View, Embedded Systems-A Register View, Register View of a Microprocessor
The Hardware Side: Storage Elements and Finite-State Machines (2 hour) The concepts of State and Time, The State Diagram, Finite State Machines-A Theoretical Model.

**UNIT 3**:

**Memories and the Memory Subsystem**: Classifying Memory, A General Memory Interface, ROM Overview, Static RAM Overview, Dynamic RAM Overview, Chip Organization, Terminology, A Memory Interface in Detail, SRAM Design, DRAM Design, DRAM Memory Interface, The Memory Map, Memory Subsystem Architecture, Basic Concepts of Caching, Designing a Cache System, Dynamic Memory Allocation.

**UNIT 4:**

**Embedded Systems Design and Development** : System Design and Development, Life-cycle Models, Problem Solving-Five Steps to Design, The

Design Process, Identifying the Requirements, Formulating the Requirements Specification, The System Design Specification, System Specifications versus System Requirements, Partitioning and Decomposing a System, Functional Design, Architectural Design, Functional Model versus Architectural Model, Prototyping, Other Considerations, Archiving the Project.

**UNIT 5 & 6:**

**Real-Time Kernels and Operating Systems**: Tasks and Things, Programs and Processes, The CPU is a resource, Threads – Lightweight and heavyweight, Sharing Resources, Foreground/Background Systems, The operating System, The real time operating system (RTOS), OS architecture, Tasks and Task control blocks, memory management revisited

**UNIT 7 & 8:**

**Performance Analysis and Optimization**: Performance or Efficiency Measures, Complexity Analysis, The methodology, Analyzing code, Instructions in Detail, Time, etc. – A more detailed look, Response Time, Time Loading, Memory Loading, Evaluating Performance, Thoughts on Performance Optimization, Performance Optimization, Tricks of the Trade, Hardware Accelerators, Caches and Performance

**Text Book**:

1. **Embedded Systems – A contemporary Design Tool,** James K. Peckol, John Weily India Pvt. Ltd, 2008

**Reference Books**:

1. **Embedded Systems: Architecture and Programming,** Raj Kamal, TMH. 2008
2. **Embedded Systems Architecture – A Comprehensive Guide for Engineers and Programmers,** Tammy Noergaard, Elsevier Publication, 2005
3. **Programming for Embedded Systems,** Dreamtech Software Team, John Wiley India Pvt. Ltd, 2008

## VLSI LAB

| | | | |
|---|---|---|---|
| Subject Code | : **10ECL77** | IA Marks | : 25 |
| No. of Practical Hrs/Week | : 03 | Exam Hours | : 03 |
| Total no. of Practical Hrs. | : 42 | Exam Marks | : 50 |

12. Speed control of stepper motor.
13. Parallel / series inverter.

Note: Experiments to be conducted with isolation transformer and low voltage.

## DSP ALGORITHMS AND ARCHITECTURE

| | | | |
|---|---|---|---|
| Subject Code | : 10EC751 | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

**INTRODUCTION TO DIGITAL SIGNAL PROCESSING:** Introduction, A Digital Signal-Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation.

**UNIT - 2**

**ARCHITECTURES FOR PROGRAMMABLE DIGITAL SIGNAL-PROCESSORS:** Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Features for External Interfacing.

**UNIT - 3**

**PROGRAMMABLE DIGITAL SIGNAL PROCESSORS:** Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54xx., Memory Space of TMS32OC54xx Processors, Program Control.

**UNIT - 4**

Detail Study of TMS320C54X & 54xx Instructions and Programming, On-Chip peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor.

**UNIT - 5**

**IMPLEMENTATION OF BASIC DSP ALGORITHMS:** Introduction, The Q-notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case).



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**UNIT - 6**

**IMPLEMENTATION OF FFT ALGORITHMS:** Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit-Reversed Index Generation & Implementation on the TMS32OC54xx.

**UNIT - 7**

**INTERFACING MEMORY AND PARALLEL I/O PERIPHERALS TO DSP DEVICES:** Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I / O Direct Memory Access (DMA).

**UNIT - 8**

**INTERFACING AND APPLICATIONS OF DSP PROCESSOR:** Introduction, Synchronous Serial Interface, A CODEC Interface Circuit. DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System.

**TEXT BOOK:**

1. **"Digital Signal Processing"**, Avatar Singh and S. Srinivasan, Thomson Learning, 2004.

**REFERENCE BOOKS:**

1. **Digital Signal Processing: A practical approach,** Ifeachor E. C., Jervis B. W Pearson-Education, PHI/ 2002
2. **"Digital Signal Processors"**, B Venkataramani and M Bhaskar TMH, 2nd, 2010
3. **"Architectures for Digital Signal Processing"**, Peter Pirsch John Weily, 2008

## MICRO AND SMART SYSTEMS TECHNOLOGY

| | | | | | |
|---|---|---|---|---|---|
| Subject Code | : | **10MS752** | IA Marks | : | 25 |
| No. of Lecture Hrs./ Week | : | 04 | Exam Hours | : | 03 |
| Total No. of Lecture Hrs. | : | 52 | Exam Marks | : | 100 |

**UNIT - 1**

**INTRODUCTION TO MICRO AND SMART SYSTEMS:**

a) What are smart-material systems? Evolution of smart materials, structures and systems. Components of a smart system. Application areas. Commercial products.



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# IMAGE PROCESSING

| | | | |
|---|---|---|---|
| Subject Code | : 10EC763 | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

**DIGITAL IMAGE FUNDAMENTALS:** What is Digital Image Processing. fundamental Steps in Digital Image Processing, Components of an Image processing system, elements of Visual Perception.

**UNIT - 2**

Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships between Pixels, Linear and Nonlinear Operations.

**UNIT - 3**

**IMAGE TRANSFORMS:** Two-dimensional orthogonal & unitary transforms, properties of unitary transforms, two dimensional discrete Fourier transform.

**UNIT - 4**

Discrete cosine transform, sine transform, Hadamard transform, Haar transform, Slant transform, KL transform.

**UNIT - 5**

**IMAGE ENHANCEMENT:** Image Enhancement in Spatial domain, Some Basic Gray Level Trans -formations, Histogram Processing, Enhancement Using Arithmetic/Logic Operations.

**UNIT - 6**

Basics of Spatial Filtering Image enhancement in the Frequency Domain filters, Smoothing Frequency Domain filters, Sharpening Frequency Domain filters, homomorphic filtering.

**UNIT - 7**

Model of image degradation/restoration process, noise models, Restoration in the Presence of Noise, Only-Spatial Filtering Periodic Noise Reduction by Frequency Domain Filtering, Linear Position-Invariant Degradations, inverse filtering, minimum mean square error (Weiner) Filtering

**UNIT - 8**



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Color Fundamentals. Color Models, Pseudo color Image Processing., processing basics of full color image processing

**TEXT BOOK:**

1. **"Digital Image Processing"**, Rafael C.Gonzalez, Richard E. Woods, etl , TMH , 2nd Edition 2010.

**REFERENCE BOOKS:**

1. **"Fundamentals of Digital Image Processing"**, Anil K. Jain, Pearson Education, 2001.
2. **"Digital Image Processing and Analysis"**, B. Chanda and D. Dutta Majumdar, PHI, 2003.

## RADIO FREQUENCY INTEGRATED CIRCUITS

| | | | |
|---|---|---|---|
| Subject Code | : **10EC764** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

**OVERVIEW OF WIRELESS PRINCIPLES:** A brief history of wireless systems, Noncellular wireless applications, Shannon, Modulations & Alphabet Soup, Propagation.

**PASSIVE RLC NETWORKS:** Introduction, Parallel RLC Tank, Series RLC Networks, Other RLC networks, RLC Networks as impedance Transformers.

**UNIT - 2**

**CHARACTERISTICS OF PASSIVE IC COMPONENTS:** Introduction, Interconnect at radio frequencies: Skin effect, resisters, Capacitors, Inductors, Transformers, Interconnect options at high frequency.

**UNIT - 3**

**A REVIEW OF MOS DEVICE PHYSICS:** Introduction, A little history, FETs, MOSFET physics, The long – channels approximation, operation in weak inversion (sub threshold), MOS device physics in the short – channel regime, Other effects.

**DISTRIBUTED SYSTEMS:** Introduction, Link between lumped and distributed regimes driving-point impedance of iterated structures,



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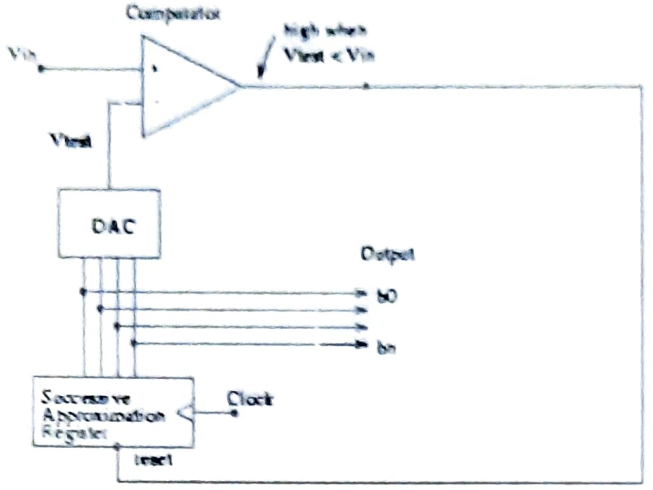


* Appropriate specification should be given.
** Applicable Library should be added & information should be given to the Designer.
*** An appropriate constraint should be given

## POWER ELECTRONICS LAB

| | | | |
|---|---|---|---|
| Subject Code | : **10ECL78** | IA Marks | : 25 |
| No. of Practical Hrs/Week: 03 | | Exam Hours | : 03 |
| Total no. of Practical Hrs. : 42 | | Exam Marks | : 50 |

Any five converter circuits experiment from the below list **must be** simulated using the **spice-simulator**.

1. Static characteristics of SCR and DIAC.
2. Static characteristics of MOSFET and IGBT.
3. Controlled HWR and FWR using RC triggering circuit
4. SCR turn off using i) LC circuit ii) Auxiliary Commutation
5. UJT firing circuit for HWR and FWR circuits.
6. Generation of firing signals for thyristors/ trials using digital circuits / microprocessor.
7. AC voltage controller using triac – diac combination.
8. Single phase Fully Controlled Bridge Converter with R and R-L loads.
9. Voltage (Impulse) commutated chopper both constant frequency and variable frequency operations.
10. Speed control of a separately exited DC motor.
11. Speed control of universal motor.



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12. Speed control of stepper motor.
13. Parallel / series inverter.

Note: Experiments to be conducted with isolation transformer and low voltage.

## DSP ALGORITHMS AND ARCHITECTURE

| | | | |
|---|---|---|---|
| Subject Code | : **10EC751** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

**INTRODUCTION TO DIGITAL SIGNAL PROCESSING:** Introduction, A Digital Signal-Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation.

**UNIT - 2**

**ARCHITECTURES FOR PROGRAMMABLE DIGITAL SIGNAL-PROCESSORS:** Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Features for External Interfacing.

**UNIT - 3**

**PROGRAMMABLE DIGITAL SIGNAL PROCESSORS:** Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54xx., Memory Space of TMS32OC54xx Processors, Program Control.

**UNIT - 4**

Detail Study of TMS320C54X & 54xx Instructions and Programming, On-Chip peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor.

**UNIT - 5**

**IMPLEMENTATION OF BASIC DSP ALGORITHMS:** Introduction, The Q-notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case).

Design Process, Identifying the Requirements, Formulating the Requirements Specification, The System Design Specification, System Specifications versus System Requirements, Partitioning and Decomposing a System, Functional Design, Architectural Design, Functional Model versus Architectural Model, Prototyping, Other Considerations, Archiving the Project.

**UNIT 5 & 6:**

**Real-Time Kernels and Operating Systems**: Tasks and Things, Programs and Processes, The CPU is a resource, Threads – Lightweight and heavyweight, Sharing Resources, Foreground/Background Systems, The operating System, The real time operating system (RTOS), OS architecture, Tasks and Task control blocks, memory management revisited

**UNIT 7 & 8:**

**Performance Analysis and Optimization**: Performance or Efficiency Measures, Complexity Analysis, The methodology, Analyzing code, Instructions in Detail, Time, etc. – A more detailed look, Response Time, Time Loading, Memory Loading, Evaluating Performance, Thoughts on Performance Optimization, Performance Optimization, Tricks of the Trade, Hardware Accelerators, Caches and Performance

**Text Book**:

1. **Embedded Systems – A contemporary Design Tool,** James K. Peckol, John Weily India Pvt. Ltd, 2008

**Reference Books**:

1. **Embedded Systems: Architecture and Programming,** Raj Kamal, TMH. 2008
2. **Embedded Systems Architecture – A Comprehensive Guide for Engineers and Programmers,** Tammy Noergaard, Elsevier Publication, 2005
3. **Programming for Embedded Systems,** Dreamtech Software Team, John Wiley India Pvt. Ltd, 2008

## VLSI LAB

| | | | |
|---|---|---|---|
| Subject Code | : **10ECL77** | IA Marks | : 25 |
| No. of Practical Hrs/Week | : 03 | Exam Hours | : 03 |
| Total no. of Practical Hrs. | : 42 | Exam Marks | : 50 |

(Wherever necessary Cadence/Synopsis/Mentz Graphics tools must be used)

## PART - A

## DIGITAL DESIGN

### ASIC-DIGITAL DESIGN FLOW

1. Write Verilog Code for the following circuits and their Test Bench for **verification**, observe the waveform and **synthesize** the code with technological library with given Constraints*. Do the initial timing verification with gate level simulation.

i. An inverter
ii. A Buffer
iii. Transmission Gate
iv. Basic/universal gates
v. Flip flop -RS, D, JK, MS, T
vi. Serial & Parallel adder
vii. 4-bit counter [Synchronous and Asynchronous counter]
viii. Successive approximation register [SAR]

* *An appropriate constraint should be given*

## PART - B
## ANALOG DESIGN

**Analog Design Flow**

1. Design an **Inverter** with given specifications*, completing the design flow mentioned below:

a. **Draw the schematic** and verify the following
   i) DC Analysis
   ii) Transient Analysis
b. **Draw the Layout** and verify the DRC, ERC
c. Check for LVS
d. Extract RC and back annotate the same and verify the Design
e. Verify & Optimize for Time, Power and Area to the given constraint***

2. Design the following circuits with given specifications*, completing the design flow mentioned below:

a. Draw the schematic and verify the following
   i) DC Analysis
   ii) AC Analysis



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iii) Transient Analysis

b. Draw the Layout and verify the DRC, ERC

c. Check for LVS

d. Extract RC and back annotate the same and verify the Design.

i) A Single Stage differential amplifier

ii) Common source and Common Drain amplifier

3. Design an **op-amp** with given specification* using given differential amplifier Common source and Common Drain amplifier in library** and completing the design flow mentioned below:

a. Draw the schematic and verify the following

i) DC Analysis

ii). AC Analysis

iii) Transient Analysis

b. Draw the Layout and verify the DRC, ERC

c. Check for LVS

d. Extract RC and back annotate the same and verify the Design.

4. Design a **4 bit R-2R based DAC** for the given specification and completing the design flow mentioned using given op-amp in the library**.

a. Draw the schematic and verify the following

i) DC Analysis

ii) AC Analysis

iii) Transient Analysis

b. Draw the Layout and verify the DRC, ERC

c. Check for LVS

d. Extract RC and back annotate the same and verify the Design.

5. For the **SAR based ADC** mentioned in the figure below draw the mixed signal schematic and verify the functionality by completing ASIC Design FLOW.

**[Specifications to GDS-II]**



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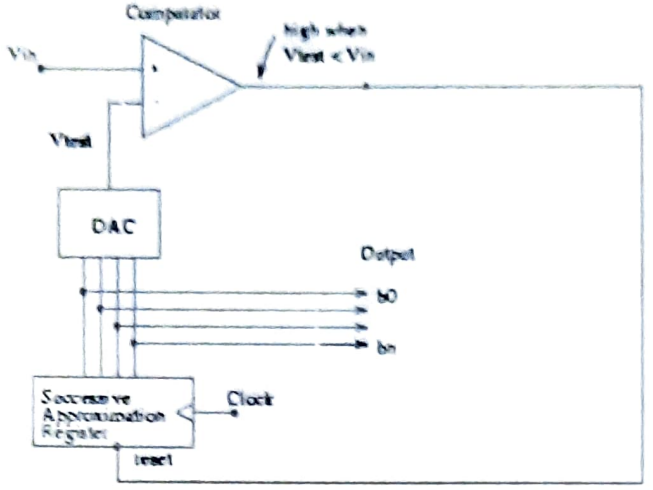


* Appropriate specification should be given.
** Applicable Library should be added & information should be given to the Designer.
*** An appropriate constraint should be given

## POWER ELECTRONICS LAB

| | | | |
|---|---|---|---|
| Subject Code | : **10ECL78** | IA Marks | : 25 |
| No. of Practical Hrs/Week: 03 | | Exam Hours | : 03 |
| Total no. of Practical Hrs. : 42 | | Exam Marks | : 50 |

Any five converter circuits experiment from the below list **must be** simulated using the **spice-simulator**.

1. Static characteristics of SCR and DIAC.
2. Static characteristics of MOSFET and IGBT.
3. Controlled HWR and FWR using RC triggering circuit
4. SCR turn off using i) LC circuit ii) Auxiliary Commutation
5. UJT firing circuit for HWR and FWR circuits.
6. Generation of firing signals for thyristors/ trials using digital circuits / microprocessor.
7. AC voltage controller using triac – diac combination.
8. Single phase Fully Controlled Bridge Converter with R and R-L loads.
9. Voltage (Impulse) commutated chopper both constant frequency and variable frequency operations.
10. Speed control of a separately exited DC motor.
11. Speed control of universal motor.



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VIII SEMESTER

## WIRELESS COMMUNICATION

| | | | |
|---|---|---|---|
| Subject Code | : **10EC81** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

Introduction to wireless telecommunication systems and Networks, History and Evolution Different generations of wireless cellular networks 1G, 2g,3G and 4G networks.

**UNIT - 2**

Common Cellular System components, Common cellular network components, Hardware and software, views of cellular networks, 3G cellular systems components, Cellular component identification Call establishment.

**UNIT - 3**

Wireless network architecture and operation, Cellular concept Cell fundamentals, Capacity expansion techniques, Cellular backbone networks, Mobility management, Radio resources and power management Wireless network security

**UNIT - 4**

GSM and TDMA techniques, GSM system overview, GSM Network and system Architecture, GSM channel concepts, GSM identifiers

**UNIT - 5**

GSM system operation, Traffic cases, Cal handoff, Roaming, GSM protocol architecture. TDMA systems

**UNIT - 6**

CDMA technology, CDMA overview, CDMA channel concept CDMA operations.

**UNIT - 7**

Wireless Modulation techniques and Hardware, Characteristics of air interface, Path loss models, wireless coding techniques, Digital modulation techniques, OFDM, UWB radio techniques, Diversity techniques, Typical GSM Hardware.



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**UNIT - 8**

Introduction to wireless LAN 802.11X technologies, Evolution of Wireless LAN Introduction to 802.15X technologies in PAN Application and architecture Bluetooth Introduction to Broadband wireless MAN, 802.16X technologies.

**TEXT BOOK:**

1. **Wireless Telecom Systems and networks**, Mullet: Thomson Learning 2006.

**REFERENCE BOOKS:**

1. **Mobile Cellular Telecommunication**, Lee W.C.Y, MGH, 2nd, 2009.
2. **Wireless communication** - D P Agrawal: 2nd Edition Thomson learning 2007.
3. **Fundamentals of Wireless Communication**, David Tse, Pramod Viswanath, Cambridge 2005.
4. S. S. Manvi, M. S. Kakkasageri, "**Wireles and Mobile Network concepts and protocols**", John Wiley India Pvt. Ltd, 1st edition, 2010.
5. "**Wireless Communication – Principles & Practice**" , T.S. Rappaport, PHI 2001.

## DIGITAL SWITCHING SYSTEMS

| | | | |
|---|---|---|---|
| Subject Code | : **10EC82** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

Developments of telecommunications, Network structure, Network services, terminology, Regulation, Standards. Introduction to telecommunications transmission, Power levels, Four wire circuits, Digital transmission, FDM, TDM, PDH and SDH, Transmission performance.

**UNIT - 2**

**EVOLUTION OF SWITCHING SYSTEMS:** Introduction, Message switching, Circuit switching, Functions of switching systems, Distribution systems, Basics of crossbar systems, Electronic switching, Digital switching systems.

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**UNIT - 8**

Introduction to wireless LAN 802.11X technologies, Evolution of Wireless LAN Introduction to 802.15X technologies in PAN Application and architecture Bluetooth Introduction to Broadband wireless MAN, 802.16X technologies.

**TEXT BOOK:**

1. **Wireless Telecom Systems and networks**, Mullet: Thomson Learning 2006.

**REFERENCE BOOKS:**

1. **Mobile Cellular Telecommunication**, Lee W.C.Y, MGH, 2nd, 2009.
2. **Wireless communication** - D P Agrawal: 2nd Edition Thomson learning 2007.
3. **Fundamentals of Wireless Communication**, David Tse, Pramod Viswanath, Cambridge 2005.
4. S. S. Manvi, M. S. Kakkasageri, "**Wireles and Mobile Network concepts and protocols**", John Wiley India Pvt. Ltd, 1st edition, 2010.
5. "**Wireless Communication – Principles & Practice**" , T.S. Rappaport, PHI 2001.

## DIGITAL SWITCHING SYSTEMS

| | | | |
|---|---|---|---|
| Subject Code | : **10EC82** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

Developments of telecommunications, Network structure, Network services, terminology, Regulation, Standards. Introduction to telecommunications transmission, Power levels, Four wire circuits, Digital transmission, FDM, TDM, PDH and SDH, Transmission performance.

**UNIT - 2**

**EVOLUTION OF SWITCHING SYSTEMS:** Introduction, Message switching, Circuit switching, Functions of switching systems, Distribution systems, Basics of crossbar systems, Electronic switching, Digital switching systems.

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**DIGITAL SWITCHING SYSTEMS:** Fundamentals : Purpose of analysis, Basic central office linkages, Outside plant versus inside plant, Switching system hierarchy, Evolution of digital switching systems, Stored program control switching systems, Digital switching system fundamentals, Building blocks of a digital switching system, Basic call processing.

**UNIT - 3**

**TELECOMMUNICATIONS TRAFFIC:** Introduction, Unit of traffic, Congestion, Traffic measurement, Mathematical model, lost call systems, Queuing systems.

**UNIT - 4**

**SWITCHING SYSTEMS:** Introduction, Single stage networks, Gradings, Link Systems, GOS of Linked systems.

**UNIT - 5**

**TIME DIVISION SWITCHING:** Introduction, space and time switching, Time switching networks, Synchronisation.

**UNIT - 6**

**SWITCHING SYSTEM SOFTWARE:** Introduction, Scope, Basic software architecture, Operating systems, Database Management, Concept of generic program, Software architecture for level 1 control, Software architecture for level 2 control, Software architecture for level 3 control, Digital switching system software classification, Call models, Connect sequence, Software linkages during call, Call features, Feature flow diagram, Feature interaction.

**UNIT - 7**

**MAINTENANCE OF DIGITAL SWITCHING SYSTEM:** Introduction, Scope, Software maintenance, Interface of a typical digital switching system central office, System outage and its impact on digital switching system reliability, Impact of software patches on digital switching system maintainability, Embedded patcher concept, Growth of digital switching system central office, Generic program upgrade, A methodology for proper maintenance of digital switching system, Effect of firmware deployment on digital switching system, Firmware-software coupling, Switching system maintainability metrics, Upgrade process success rate, Number of patches applied per year, Diagnostic resolution rate, Reported critical and major faults corrected, A strategy improving software quality, Program for software process improvement, Software processes improvement, Software processes, Metrics, Defect analysis, Defect analysis.



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**UNIT - 8**

**A GENERIC DIGITAL SWITCHING SYSTEM MODEL:** Introduction, Scope, Hardware architecture, Software architecture, Recovery strategy, Simple call through a digital system, Common characteristics of digital switching systems. Analysis report. Reliability analysis.

**TEXT BOOKS:**

1. **Telecommunication and Switching, Traffic and Networks** - J E Flood: Pearson Education, 2002.
2. **Digital Switching Systems**, Syed R. Ali, TMH Ed 2002.

**REFERENCE BOOK:**

1. **Digital Telephony** - John C Bellamy: Wiley India India Pvt. Ltd, 3rd Ed, 2008.

## ELECTIVE –4 (GROUP D)

## DISTRIBUTED SYSTEM

| | | | |
|---|---|---|---|
| Subject Code | : **10EC831** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

**CHARACTERIZATION OF DISTRIBUTED SYSTEMS:** Introduction, Examples of distributed systems, Resource sharing and the web, Challenges.

**UNIT - 2**

**SYSTEM MODELS:** Introduction, Architectural models, Fundamental mode.

**UNIT - 3**

**INTERPROCESS COMMUNICATION:** Introduction, The API for the internet protocols, External data representation and marshalling, Clint-server communication, Group communication.

**UNIT - 4**

**DISTRIBUTED OBJECTS AND REMOTE INVOCATION:** Introduction, Communication between distributed objects, Remote procedure call, Events and notifications.



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**UNIT - 5**

**SECURITY:** Introduction, Overview of security technique cryptographic algorithms, Digital signature, Cryptography progrmatics.

**UNIT - 6**

**TIME & GLOBAL STATES:** Introduction, Clocks, Events, Process states, Synchronizing physical clocks, Global states, Distributed debugging.

**UNIT - 7**

**COORDINATION AND AGREEMENT:** Distributed mutual exclusion, Elections, Multicast communication.

**UNIT - 8**

**CORBA CASE STUDY:** Introduction, CORBA RMI, CORBA Services.

**TEXT BOOK:**

1. **"Distributed Systems, Concepts & Design"**, George Coulouris, Jeam Dollimore, Tim Kindberg, fourth edition, 2006. Pearson education.

**REFERENCE BOOK:**

1. **"Distributed System Architecture, a Middleware Approach"** Arno puder, Kay Romer, Frank Pilhofer, Morgan Kaufmann publishers.

## NETWORK SECURITY

| | | | |
|---|---|---|---|
| Subject Code | : **10EC832** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

Services, mechanisms and attacks, The OSI security architecture, A model for network security.



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**UNIT - 2**
**SYMMETRIC CIPHERS:** Symmetric Cipher Model, Substitution Techniques, Transposition Techniques, Simplified DES, Data encryption standard (DES), The strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of Operation, Evaluation Criteria for Advanced Encryption Standard, The AES Cipher.

**UNIT - 3**
Principles of Public-Key Cryptasystems, The RSA algorithm, Key Management, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Authentication functions, Hash Functions.

**UNIT - 4**
Digital signatures, Authentication Protocols, Digital Signature Standard.

**UNIT - 5**
Web Security Consideration, Security socket layer (SSL) and Transport layer security, Secure Electronic Transaction.

**UNIT - 6**
Intruders, Intrusion Detection, Password Management.

**UNIT - 7**
**MALICIOUS SOFTWARE:** Viruses and Related Threats, Virus Countermeasures.

**UNIT - 8**
Firewalls Design Principles, Trusted Systems.

**TEXT BOOK:**

1. **Cryptography and Network Security**, William Stalling, Pearson Education, 2003.

**REFERENCE BOOKS:**

1. **Cryptography and Network Security**, Behrouz A. Forouzan, TMH, 2007.
2. **Cryptography and Network Security**, Atul Kahate, TMH, 2003.

## OPTICAL NETWORKS

Subject Code : **10EC833** IA Marks : 25



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## GSM

| | | | |
|---|---|---|---|
| Subject Code | : **10EC843** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

**GSM ARCHITECTURE AND INTERFACES:** Introduction, GSM frequency bands, GSM PLMN, Objectives of a GSM PLMN, GSM PLMN Services, GSM Subsystems, GSM Subsystems entities, GSM interfaces, The radio interface (MS to BSC), $A_{bits}$ interface (BTS to BSC), A interface (BSC to MSC), Interfaces between other GSM entities, Mapping of GSM layers onto OSI layers.

**UNIT - 2**

**RADIO LINK FEATURES IN GSM SYSTEMS:** Introduction, Radio link measurements, Radio link features of GSM, Dynamic power control, Discontinuous transmission (DTX), SFH, Future techniques to reduce interface in GSM, Channel borrowing, Smart antenna.

**UNIT - 3**

**GSM LOGICAL CHANNELS AND FRAME STRUCTURE:** Introduction, GSM logical channels, Allowed logical channel combinations, TCH multi frame for TCH/H, CCH multi frame, GSM frame structure, GSM bursts, Normal burst, Synchronization burst, Frequency correction channel burst, Access burst, Data encryption in GSM, Mobility management, Location registration, Mobile identification.

**UNIT - 4**

**SPEECH CODING IN GSM:** Introduction, Speech coding methods, Speech code attributes, Transmission bit rate, Delay, Complexity, Quality, LPAS, ITU-T standards, Bit rate, Waveform coding, Time domain waveform coding, Frequency domain waveform coding, Vocoders, Full-rate vocoder, Half-rate vocoder. MESSAGES, SERVICES, AND CALL FLOWS IN GSM: Introduction, GSM PLMN services.

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**UNIT - 5**

GSM messages, MS-BS interface, BS to MSC messages on the A interface, MSC to VLR and HLR, GSM call setup by an MS, Mobile-Terminated call, Call release, Handover, Data services, Introduction, Data interworking, GSM data services, Interconnection for switched data, Group 3 fax, Packet data on the signaling channel, User-to-user signaling, SMS, GSM GPRS.

**UNIT - 6**

**PRIVACY AND SECURITY IN GSM:** Introduction, Wireless security requirements, Privacy of communications, Authentication requirements, System lifetime requirements, Physical requirements, SIM cards, Security algorithms for GSM, Token-based authentication, Token-based registration, Token-based challenge.

**UNIT - 7**

**PLANNING AND DESIGN OF A GSM WIRELESS NETWORK:** Introduction, Tele traffic models, Call model, Topology model, Mobility in cellular / PCS networks, Application of a fluid flow model, Planning of a wireless network, Radio design for a cellular / PCS network, Radio link design, Coverage planning, Design of a wireless system, Service requirements, Constraints for hardware implementation, Propagation path loss, System requirements, Spectral efficiency of a wireless system, Receiver sensitivity and link budget, Selection of modulation scheme, Design of TDMA frame, Relationship between delay spread and symbol rate, Design example for a GSM system.

**UNIT - 8**

**MANAGEMENT OF GSM NETWORKS:** Introduction, Traditional approaches to NM, TMN, TMN layers, TMN nodes, TMN interface, TMN management services, Management requirements for wireless networks, Management of radio resources, Personal mobility management, Terminal mobility, Service mobility management, Platform-centered management, SNMP, OSI systems management, NM interface and functionality, NMS functionality, OMC functionality, Management of GSM network, TMN applications, GSM information model, GSM containment tree, Future work items.

**TEXT BOOK:**

1. **"Principles of Applications of GSM"**, Vijay K. Garg & Joseph E. Wilkes, Pearson education/ PHI, 1999.

**REFERENCE BOOKS:**


1. **GSM: Evolution towards 3rd Generation Systems**, (Editor), Z. Zvonar Peter Jung, Karl Kammerlander Springer; 1st edition 1998
2. **GSM & UMTS: The Creation of Global Mobile Communication**, Friedhelm Hillebrand, John Wiley & Sons; 2001.


## ADHOC WIRELESS NETWORKS

| | | | |
|---|---|---|---|
| Subject Code | : **10EC844** | IA Marks | : 25 |
| No. of Lecture Hrs/Week | : 04 | Exam Hours | : 03 |
| Total no. of Lecture Hrs. | : 52 | Exam Marks | : 100 |

**UNIT - 1**

**AD HOC NETWORKS:** Introduction, Issues in Ad hoc wireless networks, Ad hoc wireless internet.

**UNIT - 2**

**MAC PROTOCOLS FOR AD HOC WIRELESS NETWORKS:** Introduction, Issues in designing a MAC protocol for Ad hoc wireless Networks, Design goals of a MAC protocol for Ad hoc wireless Networks, Classification of MAC protocols.

**UNIT - 3**

Contention - based MAC protocols with scheduling mechanism, MAC protocols that use directional antennas, Other MAC protocols.

**UNIT - 4**

**ROUTING PROTOCOLS FOR AD HOC WIRELESS NETWORKS:** Introduction, Issues in designing a routing protocol for Ad hoc wireless Networks, Classification of routing protocols, Table drive routing protocol, On-demand routing protocol.

**UNIT - 5**

Hybrid routing protocol, Routing protocols with effective flooding mechanisms, Hierarchical routing protocols, Power aware routing protocols.

**UNIT - 6**

**TRANSPORT LAYER PROTOCOLS FOR AD HOC WIRELESS NETWORKS:** Introduction, Issues in designing a transport layer protocol



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