

## ANALOG AND DIGITAL ELECTRONICS

[As per Choice Based Credit System (CBCS) scheme]

(Effective from the academic year 2015 -2016)

### SEMESTER - III

Subject Code	15CS32	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50	Exam Hours	03

CREDITS – 04

**Course objectives:** This course will enable the students to

- Recall and Recognize construction and characteristics of JFETs and MOSFETs and differentiate with BJT
- Evolve and Analyze Operational Amplifier circuits and their applications
- Describe, Illustrate and Analyze Combinational Logic circuits, Simplification of Algebraic Equations using Karnaugh Maps and Quine McClusky Techniques.
- Describe and Design Decoders, Encoders, Digital multiplexers, Adders and Subtractors, Binary comparators, Latches and Master-Slave Flip-Flops.
- Describe, Design and Analyze Synchronous and Asynchronous Sequential
- Explain and design registers and Counters, A/D and D/A converters.

#### Module -1

**Teaching Hours**

**Field Effect Transistors:** Junction Field Effect Transistors, MOSFETs, Differences between JFETs and MOSFETs, Biasing MOSFETs, FET Applications, CMOS Devices. Wave-Shaping Circuits: Integrated Circuit(IC) Multivibrators. **Introduction to Operational Amplifier:** Ideal v/s practical Opamp, Performance Parameters, **Operational Amplifier Application Circuits:** Peak Detector Circuit, Comparator, Active Filters, Non-Linear Amplifier, Relaxation Oscillator, Current-To-Voltage Converter, Voltage-To-Current Converter.

**10 Hours**

**Text book 1:-** Ch5: 5.2, 5.3, 5.5, 5.8, 5.9, 5.1.Ch13: 13.10.Ch 16: 16.3, 16.4. Ch 17: 7.12, 17.14, 17.15, 17.18, 17.19, 17.20, 17.21.)

#### Module -2

**The Basic Gates:** Review of Basic Logic gates, Positive and Negative Logic, Introduction to HDL. **Combinational Logic Circuits:** Sum-of-Products Method, Truth Table to Karnaugh Map, Pairs Quads, and Octets, Karnaugh Simplifications, Don't-care Conditions, Product-of-sums Method, Product-of-sums simplifications, Simplification by Quine-McClusky Method, Hazards and Hazard covers, HDL Implementation Models.

**10 Hours**

**Text book 2:-** Ch2: 2.4, 2.5. Ch3: 3.2 to 3.11.

#### Module – 3



<p><b>Data-Processing Circuits:</b> Multiplexers, Demultiplexers, 1-of-16 Decoder, BCD to Decimal Decoders, Seven Segment Decoders, Encoders, Exclusive-OR Gates, Parity Generators and Checkers, Magnitude Comparator, Programmable Array Logic, Programmable Logic Arrays, HDL Implementation of Data Processing Circuits. Arithmetic Building Blocks, Arithmetic Logic Unit <b>Flip- Flops:</b> RS Flip-Flops, Gated Flip-Flops, Edge-triggered RS FLIP-FLOP, Edge-triggered D FLIP-FLOPs, Edge-triggered JK FLIP-FLOPs.</p> <p><b>Text book 2:-</b> Ch 4:- 4.1 to 4.9, 4.11, 4.12, 4.14.Ch6:-6.7, 6.10.Ch8:- 8.1 to 8.5.</p>	<p><b>10 Hours</b></p>
<p><b>Module-4</b></p>	
<p><b>Flip- Flops:</b> FLIP-FLOP Timing, JK Master-slave FLIP-FLOP, Switch Contact Bounce Circuits, Various Representation of FLIP-FLOPs, HDL Implementation of FLIP-FLOP. <b>Registers:</b> Types of Registers, Serial In - Serial Out, Serial In - Parallel out, Parallel In - Serial Out, Parallel In - Parallel Out, Universal Shift Register, Applications of Shift Registers, Register implementation in HDL. <b>Counters:</b> Asynchronous Counters, Decoding Gates, Synchronous Counters, Changing the Counter Modulus.</p> <p><b>(Text book 2:-</b> Ch 8: 8.6, 8.8, 8.9, 8.10, 8.13. Ch 9: 9.1 to 9.8. Ch 10: 10.1 to 10.4)</p>	<p><b>10 Hours</b></p>
<p><b>Module-5</b></p>	
<p><b>Counters:</b> Decade Counters, Presetable Counters, Counter Design as a Synthesis problem, A Digital Clock, Counter Design using HDL. <b>D/A Conversion and A/D Conversion:</b> Variable, Resistor Networks, Binary Ladders, D/A Converters, D/A Accuracy and Resolution, A/D Converter-Simultaneous Conversion, A/D Converter-Counter Method, Continuous A/D Conversion, A/D Techniques, Dual-slope A/D Conversion, A/D Accuracy and Resolution.</p> <p><b>Text book 2:-</b> Ch 10: 10.5 to 10.9. Ch 12: 12.1 to 12.10</p>	<p><b>10 Hours</b></p>
<p><b>Course outcomes:</b> After Studying this course, students will be able to</p>	
<ul style="list-style-type: none"> <li>• Explain the operation of JFETs and MOSFETs , Operational Amplifier circuits and their application</li> <li>• Explain Combinational Logic, Simplification Techniques using Karnaugh Maps, Quine McClusky technique.</li> <li>• Demonstrate Operation of Decoders, Encoders, Multiplexers, Adders and Subtractors, working of Latches, Flip-Flops, Designing Registers, Counters, A/D and D/A Converters</li> <li>• Design of Counters, Registers and A/D &amp; D/A converters</li> </ul>	
<p><b>Graduate Attributes (as per NBA)</b></p> <ol style="list-style-type: none"> <li>1. Engineering Knowledge</li> <li>2. Design/Development of Solutions(partly)</li> <li>3. Modern Tool Usage</li> <li>4. Problem Analysis</li> </ol>	
<p><b>Question paper pattern:</b></p> <p>The question paper will have ten questions. There will be 2 questions from each module. Each question will have questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.</p>	
<p><b>Text Books:</b></p>	

1. Anil K Maini, Varsha Agarwal: Electronic Devices and Circuits, Wiley, 2012.
2. Donald P Leach, Albert Paul Malvino & Goutam Saha: Digital Principles and Applications, 8<sup>th</sup> Edition, Tata McGraw Hill, 2015

**Reference Books:**

1. Stephen Brown, Zvonko Vranesic: Fundamentals of Digital Logic Design with VHDL, 2<sup>nd</sup> Edition, Tata McGraw Hill, 2005.
2. R D Sudhaker Samuel: Illustrative Approach to Logic Design, Sanguine-Pearson, 2010.
3. M Morris Mano: Digital Logic and Computer Design, 10<sup>th</sup> Edition, Pearson, 2008.



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