Setting Event Handlers, Using Action Scripts to Define States, Managing Object Creation Policies, Handling State Events, Understanding State Life Cycles, When To Use States.Using Effects and Transitions: Using Effects, Creating Custom Effects, Using Transitions, Creating Custom Transitions.

UNIT – 8 **6 Hours**

Flex – 5: Working with Data: Using Data Models, Data Binding, Enabling Data Binding for Custom Classes, Data Binding Examples, Building data binding proxies.Validating and Formatting Data: Validating user input, Formatting Data.

Text Books:

1. Steven Holzner: Ajax: A Beginner's Guide, Tata McGraw Hill, 2009.
   (Listed topics from Chapters 3, 4, 6, 7, 11, 12)
2. Chafic Kazon and Joey Lott: Programming Flex 3, O'Reilly, June 2009.
   (Listed topics from Chapters 1 to 8, 12 to 15)

Reference Books:

1. Jack Herrington and Emily Kim: Getting Started with Flex 3, O'Reilly, 1st Edition, 2008.
2. Michele E. Davis and John A. Phillips: Flex 3 - A Beginner's Guide, Tata McGraw-Hill, 2008.
3. Colin Moock: Essential Actionscript 3.0, O'Reilly Publications, 2007.
4. Nicholas C Zakas et al : Professional Ajax, 2nd Edition, Wrox/Wiley India, 2008.

VLSI DESIGN AND ALGORITHMS

Sub Code: 10CS833 **IA Marks : 25**
Hrs/Week: 04 **Exam Hours : 03**
Total Hrs: 52 **Exam Marks : 100**

PART - A

UNIT 1 **6 Hours**

Digital Systems and VLSI: Why design Integrated Circuits? Integrated Circuits manufacturing, CMOS Technology, Integrated Circuit Design Techniques, IP-based Design.

UNIT 2 **8 Hours**

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Fabrication and Devices: Fabrication Processes, Transistors, Wires and vias, SCMOS Design Rules, Layout design and tools.

UNIT 3 **6 Hours**

Logic Gates – 1: Combinatorial logic functions, Static Complementary gates, Switch Logic.

UNIT 4 **6 Hours**

Logic Gates – 2: Alternative gate Circuits, Low Power gates, Delay through resistive interconnect; Delay through inductive interconnect, Design for yield, Gates as IP.

PART - B

UNIT 5 **6 Hours**

Combinational Logic Networks: Standard cell-based layout, Combinatorial network delay, Logic and interconnect design, Power Optimization, Switch logic networks, Combinational logic testing.

UNIT 6 **6 Hours**

Sequential Machines: Latches and Flip-flops, Sequential systems and clocking disciplines, Clock generators, Sequential systems design, Power optimization, Design validation, Sequential testing.

UNIT 7 **6 Hours**

Architecture Design: Register Transfer design, High Level Synthesis, Architecture for Low Power, Architecture testing.

UNIT 8 **8 Hours**

Design Problems and Algorithms : Placement and Partitioning: Circuit Representation, Wire-length Estimation, Types of Placement Problems, Placement Algorithms, Constructive Placement, Iterative Improvement, Partitioning, The Kernighan-Lin Partitioning Algorithm. Floor Planning: Concepts, Shape functions and floor plan sizing.Routing: Types of Local Routing Problems, Area Routing, Channel Routing, Introduction to Global Routing, Algorithms for Global Routing

Text Books:

1. Wayne Wolf: Modern VLSI Design - IP-Based Design, 4th Edition, PHI Learning, 2009.
   (Listed topics only from Chapters 1 to 5, and 8)
2. Sabih H. Gerez: Algorithms for VLSI Design Automation, Wiley India, 2007.
   (Listed topics only from Chapters 7, 8, and 9)

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