

Implement the following operations by writing an appropriate constructor and an overloaded operator +.

- i. OCTAL $h = x$; where x is an integer
- ii. $\text{int } y = h + k$; where h is an OCTAL object and k is an integer.

Display the OCTAL result by overloading the operator <<. Also display the values of h and y.

14. Design, develop, and execute a program in C++ to create a class called BIN_TREE that represents a Binary Tree, with member functions to perform inorder, preorder and postorder traversals. Create a BIN_TREE object and demonstrate the traversals.

Note: In the examination each student picks one question from a lot of all the 14 questions.

ELECTRONIC CIRCUITS & LOGIC DESIGN LABORATORY
(Common to CSE & ISE)

Subject Code: 10CSL38
Hours/Week : 03
Total Hours : 42

L.A. Marks : 25
Exam Hours: 03
Exam Marks : 50

PART-A

1. a) Design and construct a suitable circuit and demonstrate the working of positive clipper, double-ended clipper and positive clamper using diodes.
b) Demonstrate the working of the above circuits using a simulation package.
2. a) Design and construct a suitable circuit and determine the frequency response, input impedance, output impedance, and bandwidth of a CE amplifier.
b) Design and build the CE amplifier circuit using a simulation package and determine the voltage gain for two different values of supply voltage and for two different values of emitter resistance.
3. a) Design and construct a suitable circuit and determine the drain characteristics and transconductance characteristics of an enhancement-mode MOSFET.
b) Design and build CMOS inverter using a simulation package and verify its truth table.

15



H.O.D.

Dept. Of Computer Science & Engineering
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

4. a) Design and construct a Schmitt trigger using Op-Amp for given UTP and LTP values and demonstrate its working.
b) Design and implement a Schmitt trigger using Op-Amp using a simulation package for two sets of UTP and LTP values and demonstrate its working.
5. a) Design and construct a rectangular waveform generator (Op-Amp relaxation oscillator) for given frequency and demonstrate its working.
b) Design and implement a rectangular waveform generator (Op-Amp relaxation oscillator) using a simulation package and demonstrate the change in frequency when all resistor values are doubled.
6. Design and implement an astable multivibrator circuit using 555 timer for a given frequency and duty cycle.

PART - B

7. a) Given a 4-variable logic expression, simplify it using Entered Variable Map and realize the simplified logic expression using 8:1 multiplexer IC.
b) Design and develop the Verilog /VHDL code for an 8:1 multiplexer. Simulate and verify its working.
8. a) Realize a J-K Master / Slave Flip-Flop using NAND gates and verify its truth table.
b) Design and develop the Verilog / VHDL code for D Flip-Flop with positive-edge triggering. Simulate and verify its working.
9. a) Design and implement a mod-n ($n < 8$) synchronous up counter using J-K Flip-Flop ICs and demonstrate its working.
b) Design and develop the Verilog / VHDL code for mod-8 up counter. Simulate and verify its working.
10. a) Design and implement a ring counter using 4-bit shift register and demonstrate its working.
b) Design and develop the Verilog / VHDL code for switched tail counter. Simulate and verify its working.
11. Design and implement an asynchronous counter using decade counter IC to count up from 0 to n ($n \leq 9$) and demonstrate its working.



H. O. D.
Dept. Of Computer Science & Engineering
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

12. Design and construct a 4-bit R-2R ladder D/A converter using Op-Amp. Determine its accuracy and resolution.

Notes:

1. In the examination, each student picks one question from the lot of questions, either from Part-A or from Part-B. About half the students in the batch are to get a question from Part-A while the rest are to get the question from Part-B.
2. Any simulation package like MultiSim / Pspice etc may be used.

IV SEMESTER

ENGINEERING MATHEMATICS – IV

CODE: 10 MAT 41
Hrs/Week: 04
Total Hrs: 52

IA Marks: 25
Exam Hrs: 03
Exam Marks:100

PART-A

Unit-I: NUMERICAL METHODS - 1

Numerical solution of ordinary differential equations of first order and first degree; Picard's method, Taylor's series method, modified Euler's method, Runge-kutta method of fourth-order, Milne's and Adams - Bashforth predictor and corrector methods (No derivations of formulae).

[6 hours]

Unit-II: NUMERICAL METHODS – 2

Numerical solution of simultaneous first order ordinary differential equations: Picard's method, Runge-Kutta method of fourth-order. Numerical solution of second order ordinary differential equations: Picard's method, Runge-Kutta method and Milne's method.

[6 hours]

Unit-III: Complex variables – 1

Function of a complex variable, Analytic functions-Cauchy-Riemann equations in cartesian and polar forms. Properties of analytic functions.



H. O. D.
Dept. Of Computer Science & Engineering
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225