UNIT - 6

Hardware Specifications, Memory Interface - 1: Pin-Outs and the Pin Functions, Clock Generator, Bus Buffering and Latching, Bus Timings, Ready and Wait State, Minimum versus Maximum Mode.

Memory Interfacing: Memory Devices

UNIT - 7

Memory Interface - 2, I/O Interface - 1: Memory Interfacing (continued):
Address Decoding, 8088 Memory Interface, 8086 Memory Interface.
Basic I/O Interface: Introduction to I/O Interface, I/O Port Address Decoding.

UNIT 8

1/O Interface – 2, Interrupts, and DMA: I/O Interface (continued): The Programmable Peripheral Interface 82C55, Programmable Interval Timer 8254.

Interrupts: Basic Interrupt Processing, Hardware Interrupts: INTR and INTA/; Direct Memory Access: Basic DMA Operation and Definition.

### Text Book:

 Barry B Brey: The Intel Microprocessors, 8<sup>th</sup> Edition, Pearson Education, 2009.
 (Listed topics only from the Chapters 1 to 13)

#### Reference Books:

- Douglas V. Hall: Microprocessors and Interfacing, Revised 2<sup>nd</sup> Edition, TMH, 2006.
- K. Udaya Kumar & B.S. Umashankar: Advanced Microprocessors & IBM-PC Assembly Language Programming, TMH 2003.
- James L. Antonakos: The Intel Microprocessor Family: Hardware and Software Principles and Applications, Cengage Learning, 2007.

## COMPUTER ORGANIZATION (Common to CSE & ISE)

Subject Code: 10CS46 I.A. Marks : 25 Hours/Week : 04 Exam Hours: 03 Total Hours : 52 Exam Marks: 100

#### PART-A

Basic Structure of Computers: Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Performance – Processor Clock, Basic

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Dept. Of Computer Science & Engineering Alva's Institute of Engg. & Technology Mijar, MOODBIDRI - 574 225 Performance Equation, Clock Rate, Performance Measurement, Historical Perspective

Machine Instructions and Programs: Numbers, Arithmetic Operations and Characters, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing,

UNIT - 2

Machine Instructions and Programs contd.: Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions, Encoding of Machine Instructions

UNIT - 3
Input/Output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Exceptions, Direct Memory Access, Buses

UNIT - 4
Input/Output Organization contd.: Interface Circuits, Standard I/O
Interfaces - PCI Bus, SCSI Bus, USB

#### PART - B

UNIT - 5

Memory System: Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, Cache Memories – Mapping Functions, Replacement Algorithms, Performance Considerations, Virtual Memories, Secondary Storage

UNIT - 6
7 Hours
Arithmetic: Addition and Subtraction of Signed Numbers, Design of Fast
Adders, Multiplication of Positive Numbers, Signed Operand Multiplication,
Fast Multiplication, Integer Division, Floating-point Numbers and Operations

UNIT - 7

Basic Processing Unit: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hard-wired Control, Microprogrammed Control

UNIT - 8

Multicores, Multiprocessors, and Clusters: Performance, The Power Wall, The Switch from Uniprocessors to Multiprocessors, Amdahl's Law, Shared Memory Multiprocessors, Clusters and other Message Passing Multiprocessors, Hardware Multithreading, SISD, IMD, SIMD, SPMD, and Vector.

**Text Books:** 

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- Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5<sup>th</sup> Edition, Tata McGraw Hill, 2002. (Listed topics only from Chapters 1, 2, 4, 5, 6, 7)
- David A. Patterson, John L. Hennessy: Computer Organization and Design - The Hardware / Software Interface ARM Edition, 4<sup>th</sup> Edition, Elsevier, 2009. (Listed topics only)

#### Reference Books:

- William Stallings: Computer Organization & Architecture, 7<sup>th</sup> Edition, PHI, 2006.
- Vincent P. Heuring & Harry F. Jordan: Computer Systems Design and Architecture, 2<sup>nd</sup> Edition, Pearson Education, 2004.

# DESIGN AND ANALYSIS OF ALGORITHMS LABORATORY (Common to CSE & ISE)

Subject Code: 10CSL47
Hours/Week: 03
Total Hours: 42

LA. Marks: 25
Exam Hours: 03
Exam Marks: 50

Design, develop and implement the specified algorithms for the following problems using C/C++ Language in LINUX / Windows environment.

- Sort a given set of elements using the Quicksort method and determine the time required to sort the elements. Repeat the experiment for different values of n, the number of elements in the list to be sorted and plot a graph of the time taken versus n. The elements can be read from a file or can be generated using the random number generator.
- 2. Using OpenMP, implement a parallelized Merge Sort algorithm to sort a given set of elements and determine the time required to sort the elements. Repeat the experiment for different values of n, the number of elements in the list to be sorted and plot a graph of the time taken versus n. The elements can be read from a file or can be generated using the random number generator.
- 3. a. Obtain the Topological ordering of vertices in a given digraph.
  - b. Compute the transitive closure of a given directed graph using Warshall's algorithm.

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