ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY
(A Unit of Alva's Education Foundation)
Shobhavana Campus, Mijar-574225, Moodbidri, D.K
Phone: 08258-262725, Fax: 08258-262726
Affiliated to VTU Belagavi and Approved by AICTE, New Delhi, Recognized by Govt. of Karnataka

ATTENDANCE BOOK

Academic Year : 2020 – 21

Semester : 7th Section B.

Period of the Semester : From 1st Sep, 2020 to 16th Jan, 2021

Subject with Code : ADVANCED COMPUTER ARCHITECTURES (17CS72)

Name of the Faculty : Dr ADHUSUDHAN. S.

Department : CSE

VISION OF THE INSTITUTE
"Transformative education by pursuing excellence in Engineering and Management through enhancing skills to meet the evolving needs of the community"

MISSION OF THE INSTITUTE
• To bestow quality technical education to imbibe knowledge, creativity and ethos to students community. • To inculcate the best engineering practices through transformative education. • To develop a knowledgeable individual for a dynamic industrial scenario. • To inculcate research, entrepreneurial skills and human values in order to cater the needs of the society.

AIET	Lesson Plan & Execution	Format No.	ACD 08
		Issue No.	01
		Rev. No.	00

Name of the faculty	Mr ADHUSUDHAN. S.
Semester and Section	7th Sem B-Sec.
Date of Commencement	1st Sept, 2020
Last Working Day of the Semester	16th Jan, 2021
Source Materials List	
1.	Advanced Computer Architectures Kai Hwang, Naresh Jotwani
2.	Computer Architecture: A quantitative approach. John L. Hennessy & D.A. Patterson
3.	
4.	
5.	
Subject Name	

Period	Plan			Execution		
	Date	Topics to be covered	Source Material needed	Topics Covered	Date	Source Material Referred
1	1/9	Theory of parallelism: parallel Computer models	1	Theory of parallelism: parallel Computer models.	1/9/20	1
2	5/9	The State of Computing	1	The State of Computing	5/9/20	1
3	7/9	Multiprocessors and Multicomputer	1	Multiprocessors and Multicomputer	7/9	1
4	10/9	Multivector and SIMD Computers PRAM and VLSI Models	1	Multivector and SIMD Computers	10/9	1

Period	Plan			Execution		
	Date	Topics to be covered	Source Material needed	Topics Covered	Date	Source Material Referred
5	12/9	Program and N/W properties Conditions of Parallelism	1	PRAM & VLSI Models	12/9	1
6	14/9	Program partitioning and Scheduling	1	Program and Network properties	14/9	1
7	17/9	Program flow mechanisms S/m interconnect architectures	1	Conditions of parallelism	17/9	1
8	19/9	Principles of Scalable Performance Performance metrics and measures	1	Program partitioning and Scheduling	19/9	1
9	21/9	Parallel Processing applications speed up performance laws.	1	Program flow mechanisms	21/9	1
10	24/9	Scalability analysis and approaches.	1	System Interconnect architectures	24/9	1
11	26/9	module-2 Advanced Processor Technology	1	Principles of Scalable Performance	26/9	1
12	28/9	Advanced Processor Technology	1	Performance metrics and measures	28/9	1
13	1/10	Superscalar and vector processors	1	Parallel Processing Applications	1/10	1
14	3/10	Superscalar and vector processors	1	Speed-up Performance laws.	3/10	1
15	5/10	Superscalar and vector processors	1	Scalability analysis and approaches	5/10	1
16	8/10	Memory Hierarchy Technologies	1	module-2 Advanced Processor Technology	8/10	1
17	10/10	Memory Hierarchy Technologies	1	Advanced Processor Technology	10/10	1

Period	Plan			Execution		
	Date	Topics to be covered	Source Material needed	Topics Covered	Date	Source Material Referred
18	12/10	Memory Hierarchy Technology	1	Advanced processor technology	12/10	1
19	15/10	Virtual memory Technology	1	Superscalar and vector processors	15/10	1
20	17/10	Virtual memory technology.	1	Superscalar and vector processors	17/10	1
21	19/10	Module-3. Bus Systems	1	Superscalar and vector processors	19/10	1
22	22/10	Cache memory organization	1	Memory Hierarchy Technology	22/10	1
23	24/10	Shared memory organization	1	Memory Hierarchy Technology	24/10	1
24	29/10	Sequential and weak Consistency models.	1	Memory Hierarchy Technology	29/10	1
25	2/11	Sequential and Weak Consistency models	1	Virtual memory technology	2/11	1
26	5/11	pipelining and Superscalar techniques	1	Virtual memory technology.	5/11	1
27	7/11	Linear pipeline processors	1	Module-3 Bus Systems	7/11	1
28	9/11	Non linear pipeline processors	1	Bus Systems	9/11	1
29	12/11	Instruction pipeline Design	1	Cache memory organizations	12/11	1
30	20/11	Arithmetic pipeline Design.	1	Cache memory organizations	20/11	1

Period	Plan			Execution		
	Date	Topics to be covered	Source Material needed	Topics Covered	Date	Source Material Referred
18	12/10	Memory Hierarchy Technology	1	Advanced processor technology	12/10	1
19	15/10	Virtual memory Technology	1	Superscalar and vector processors	15/10	1
20	17/10	Virtual memory technology.	1	Superscalar and vector processors	17/10	1
21	19/10	Module-3. Bus systems	1	Superscalar and vector processors	19/10	1
22	22/10	Cache memory organization	1	Memory Hierarchy Technology	22/10	1
23	24/10	Shared memory organizations	1	Memory Hierarchy Technology	24/10	1
24	29/10	Sequential and weak Consistency models.	1	Memory Hierarchy Technology	29/10	1
25	2/11	Sequential and Weak Consistency models	1	Virtual memory Technology	2/11	1
26	5/11	pipelining and Superscalar techniques	1	Virtual memory technology.	5/11	1
27	7/11	Linear pipeline processors	1	Module-3 Bus Systems	7/11	1
28	9/11	Non linear pipeline processors	1	Bus Systems	9/11	1
29	12/11	Instruction pipeline Design	1	Cache memory organizations	12/11	1
30	20/11	Arithmetic pipeline Design.	1	Cache memory organizations	20/11	1

Period	Plan			Execution		
	Date	Topics to be covered	Source Material needed	Topics Covered	Date	Source Material Referred
31	21/11	Module-4. Multiprocessor System Interconnects	1	Shared memory Organizations	21/11	1
32	23/11	Cache Coherence and Synchroni Zation Mechanisms	1	Shared memory organizations	23/11	1
33	25/11	Three generations of Multicomputers Message passing Mechanisms.	1	Sequential and weak Consistency models	25/11	1
34	26/11	Vector processing principles	1	Linear pipeline processors	26/11	1
35	27/11	Multivector Multiprocessors Compound vector processing	1	Linear pipeline processors	27/11	1
36	28/11	SIMD Computer organization	1	Non Linear pipeline processors	28/11	1
37	30/11	Latency Hiding techniques principles of Multithreading	1	Instruction pipeline Design	30/11	1
38	2/12	fine-grain Multicomputers	1	Arithmetic pipeline Design	2/12	1
39	3/12	Scalable and Multithreaded architectures	1	Arithmetic pipeline Design.	3/12	1
40	4/12	Data flow & Hybrid architectures.	1	module-4 Multiprocessor System Interconnects	4/12	1
41	5/12	Module-5 parallel programming models parallel languages & compilers	1	Cache Coherence & Synchronization Mechanisms.	5/12	1
42	7/12	Dependence analysis of data arrays Parallel programming environments	1	Three generations of Multicomputers	7/12	1
43	9/12	Synchronization and Multiprocessing models	1	Message passing Mechanisms.	9/12	1

Period	Plan			Execution		
	Date	Topics to be covered	Source Material needed	Topics Covered	Date	Source Material Referred
44	10/12	Shared Variable pgm Structures Computer architecture basic design issue	1	Vector Processing principles	10/12	1
45	11/12	problem definition model of a typical Processor	1	Multivector Multiprocessors	11/12	1
46	12/12	Compiler detected Instruction level parallelism.	1	Compound Vector Processing	12/12	1
47	14/12	Operand forwarding reorder buffer Register renaming	1	SIMD Computer Organizations	14/12	1
48	16/12	Tomasulo's Alg Branch prediction	1	Latency-Hiding Techniques	16/12	1
49	17/12	Limitations in exploiting instruction level parallelism	1	Principles of Multithreading	17/12	1
50	18/12	Thread level parallelism.	1	Fine-grain Multicomputers	18/12	1
51			1	Scalable & Multithreaded architectures.	19/12	1
52			1	Data flow & Hybrid architectures.	26/12	1
53			1	Module-5. parallel programming models.	28/12	1
54			1	Parallel languages & Compilers.	30/12	1
55			1	Dependence analysis of data arrays.	31/12	1
56			1	parallel programming environments	1/1/2021	1

Others	Planned	Actual	Remarks :
Special Classes	0	17	
Tutorials			
Assignments			
Seminars			
IA Tests			
Portions Covered in the entire Semester	100 %		

Course Effectiveness

Students Feedback	Very good		
Students Responce	Very good.		
Result	No. of Students AP	No. of Students Passed	% of Result
	59	59	100%

Faculty in Charge

Signature of Principal (& Remarks if any)

PRINCIPAL
Alva's Institute of Engg. & Technology,
Mijar, MOODBIDRI - 574 225, D.K.

HOD's Signature

Dept. Of Computer Science & Engineering
Alva's Institute of Engineering & Technology
Mijar, MOODBIDRI - 574 225