AIET	Lesson Plan & Execution	

Name of the Faculty	***Shilpa***
Dept-Sem-Sec :	***CS-3-A***
Date of Commencement	*1 Aug 2018*
Last working day of Semester	*7 Jan 2019* 30-Nov-2018

Source Material List

1	Anil K Maini, Varsha Agarwal: Electronic Devices and Circuits, Wiley, 2012
2	Donald P Leach, Albert Paul Malvino & Goutam Saha: Digital Principles and Applications, 8th Edition, Tata McGraw Hill, 2015
1	R D Sudhaker Samuel: Illustrative Approach to Logic Design, Sanguine-Pearson, 2010
2	M Morris Mano: Digital Logic and Computer Design, 10th Edition, Pearson, 2008

Course Outcome List

1	Explain the operation of JFETs and MOSFETs , Operational Amplifier circuits and their application
2	Describe and interpret different types of combinational logic circuits by using abridge mapping techniques viz., Karnaugh Maps, Quine-McClusky methods and develop program using HDL to simulate the behavior of various logical circuits.

3	Design and Demonstrate the Operation of Decoders, Encoders, Multiplexers, Adders and Subtractors, and develop program using HDL to simulate the behaviour of various logical circuits in the domain of economy, performance and efficiency.
4	Design and implement the working of Latches, Flip-flops, registers, counters and develop program using HDL to simulate the behaviour of various logical circuits within the realm of economic, performance, efficiency, user friendly and environmental constraints.
5	Demonstrate the fundamental knowledge of analog and digital electronics to get different types of analog to digitalized signal transformation and vice-versa
Subject Name	ANALOG AND DIGITAL ELECTRONICS

Period	Planned			Execution		
	Date	*Topic*	*Source material to be referred*	*Date*	*Topic*	*Source material to be referred*
Module 2						
1	1 Aug 2018	Review of Basic Logic gates	TEXT 2	1 Aug 2018	Review of Basic Logic gates	TEXT 2
2	2 Aug 2018	Positive and Negative Logic	TEXT 2	2 Aug 2018	Review of Basic Logic gates	TEXT 2
3	3 Aug 2018	Introduction to HDL	TEXT 2	3 Aug 2018	Positive and Negative Logic	TEXT 2
4	3 Aug 2018	Sum-of-Products Method, Truth Table to Karnaugh Map	TEXT 2	3 Aug 2018	Positive and Negative Logic	TEXT 2
5	7 Aug 2018	Pairs Quads, and Octets, Karnaugh Simplifications	TEXT 2	4 Aug 2018	Introduction to HDL	TEXT 2
6	8 Aug 2018	Don 't-care Conditions, Product-of-sums Method	TEXT 2	7 Aug 2018	Sum-of-Products Method	TEXT 2
7	9 Aug 2018	Product-of-sums simplifications	TEXT 2	8 Aug 2018	Truth Table to Karnaugh Map	TEXT 2
8	10 Aug 2018	Simplification by QuineMcClusky Method	TEXT 2	9 Aug 2018	Pairs Quads, and Octets	TEXT 2
9	10 Aug 2018	Hazards and Hazard covers	TEXT 2	10 Aug 2018	Karnaugh Simplifications	TEXT 2
10	14 Aug 2018	HDL Implementation Models	TEXT 2	10 Aug 2018	Karnaugh Simplifications	TEXT 2
Module 3						
11	16 Aug 2018	Multiplexers, Demultiplexers, 1-of-16 Decoder	TEXT 2	11 Aug 2018	Don 't-care Conditions	TEXT 2
12	17 Aug 2018	BCD to Decimal Decoders, Seven Segment Decoders	TEXT 2	11 Aug 2018	Product-of-sums Method	TEXT 2
13	17 Aug 2018	Encoders, Exclusive-OR Gates, Parity Generators and Checkers	TEXT 2	16 Aug 2018	Product-of-sums simplifications	TEXT 2
14	21 Aug 2018	Magnitude Comparator, Programmable Array Logic	TEXT 2	18 Aug 2018	Simplification by QuineMcClusky Method	TEXT 2
15	23 Aug 2018	Programmable Logic Arrays, HDL Implementation of Data Processing Circuits	TEXT 2	21 Aug 2018	Simplification by QuineMcClusky Method	TEXT 2

Period	Planned			Execution		
	Date	Topic	Source material to be referred	Date	Topic	Source material to be referred
16	24 Aug 2018	Arithmetic Building Blocks, Arithmetic Logic Unit	TEXT 2	23 Aug 2018	Hazards and Hazard covers	TEXT 2
17	24 Aug 2018	RS Flip-Flops, Gated Flip-Flops	TEXT 2	23 Aug 2018	HDL Implementation Models	TEXT 2
18	28 Aug 2018	Edge-triggered RS FLIP-FLOP	TEXT 2	28 Aug 2018	Multiplexers	TEXT 2
19	29 Aug 2018	Edge-triggered D FLIP-FLOPs	TEXT 2	28 Aug 2018	Multiplexers	TEXT 2
20	30 Aug 2018	Edge-triggered JK FLIPFLOPs	TEXT 2	29 Aug 2018	Multiplexers, Demultiplexers	TEXT 2
Module 4						
21	31 Aug 2018	FLIP-FLOP Timing, JK Master-slave FLIP-FLOP	TEXT 2	30 Aug 2018	Demultiplexers	TEXT 2
22	31 Aug 2018	Switch Contact Bounce Circuits, Various Representation of FLIP-FLOPs	TEXT 2	31 Aug 2018	1-of-16 Decoder	TEXT 2
23	4 Sep 2018	HDL Implementation of FLIP-FLOP	TEXT 2	31 Aug 2018	1-of-16 Decoder	TEXT 2
24	5 Sep 2018	Types of Registers, Serial In - Serial Out	TEXT 2	4 Sep 2018	BCD to Decimal Decoders	TEXT 2
25	11 Sep 2018	Serial In - Parallel out, Parallel In -Serial Out	TEXT 2	5 Sep 2018	Seven Segment Decoders	TEXT 2
26	12 Sep 2018	Parallel In - Parallel Out, Universal Shift Register	TEXT 2	6 Sep 2018	Encoders	TEXT 2
27	14 Sep 2018	Applications of Shift Registers, Register implementation in HDL	TEXT 2	7 Sep 2018	Exclusive-OR Gates	TEXT 2
28	14 Sep 2018	Asynchronous Counters	TEXT 2	7 Sep 2018	Parity Generators and Checkers	TEXT 2
29	18 Sep 2018	DecodingGates, Synchronous Counters	TEXT 2	11 Sep 2018	Magnitude Comparator	TEXT 2
30	19 Sep 2018	Changing the Counter Modulus	TEXT 2	12 Sep 2018	Programmable Array Logic	TEXT 2
Module 5						
31	20 Sep 2018	Decade Counters, Presettable Counters	TEXT 2	14 Sep 2018	Programmable Logic Arrays, HDL Implementation of Data Processing Circuits	TEXT 2

Period	Planned			Execution		
	Date	Topic	Source material to be referred	Date	Topic	Source material to be referred
32	25 Sep 2018	Counter Design as a Synthesis problem	TEXT 2	14 Sep 2018	Arithmetic Building Blocks	TEXT 2
33	26 Sep 2018	A Digital Clock	TEXT 2	20 Sep 2018	Arithmetic Logic Unit	TEXT 2
34	27 Sep 2018	Counter Design using HDL	TEXT 2	24 Sep 2018	RS Flip-Flops, Gated Flip-Flops	TEXT 2
35	28 Sep 2018	Variable, Resistor Networks, Binary Ladders	TEXT 2	25 Sep 2018	Edge-triggered RS FLIP-FLOP	TEXT 2
36	28 Sep 2018	D/A Converters, D/A Accuracy and Resolution	TEXT 2	27 Sep 2018	Edge-triggered D FLIP-FLOPs	TEXT 2
37	3 Oct 2018	A/D Converter-Simultaneous Conversion	TEXT 2	27 Sep 2018	Edge-triggered JK FLIPFLOPs	TEXT 2
38	4 Oct 2018	A/D Converter-Counter Method, Continuous A/D Conversion	TEXT 2	28 Sep 2018	FLIP-FLOP Timing, JK Master-slave FLIP-FLOP	TEXT 2
39	5 Oct 2018	A/D Techniques, Dual-slope A/D Conversion	TEXT 2	28 Sep 2018	Switch Contact Bounce Circuits	TEXT 2
40	5 Oct 2018	Dual-slope A/D Conversion, A/D Accuracy and Resolution	TEXT 2	28 Sep 2018	Various Representation of FLIP-FLOPs, HDL Implementation of FLIP-FLOP	TEXT 2
Module 1						
41	9 Oct 2018	Junction Field Effect Transistors, MOSFETs	TEXT 1	3 Oct 2018	Types of Registers, Serial In - Serial Out	TEXT 2
42	10 Oct 2018	Differences between JFETs and MOSFETs, Biasing MOSFETs	TEXT 1	4 Oct 2018	Serial In - Parallel out, Parallel In - Parallel Out	TEXT 2
43	11 Oct 2018	FET Applications, CMOS Devices	TEXT 1	5 Oct 2018	Parallel In -Serial Out, Universal Shift Register	TEXT 2
44	12 Oct 2018	Integrated Circuit(IC) Multivibrators	TEXT 1	5 Oct 2018	Applications of Shift Registers, Register implementation in HDL	TEXT 2
45	12 Oct 2018	Ideal v/s practical Opamp	TEXT 1	9 Oct 2018	Asynchronous Counters	TEXT 2
46	23 Oct 2018	Performance Parameters	TEXT 1	9 Oct 2018	DecodingGates, Synchronous Counters	TEXT 2
47	24 Oct 2018	Peak Detector Circuit, Comparator	TEXT 1	10 Oct 2018	Synchronous Counters, Changing the Counter Modulus	TEXT 2

Period	Planned			Execution		
	Date	*Topic*	*Source material to be referred*	*Date*	*Topic*	*Source material to be referred*
48	25 Oct 2018	Active Filters, NonLinear Amplifier	TEXT 1	11 Oct 2018	Decade Counters, Presettable Counters	TEXT 2
49	26 Oct 2018	Relaxation Oscillator, Current-To-Voltage Converter	TEXT 1	12 Oct 2018	Counter Design as a Synthesis problem	TEXT 2
50	26 Oct 2018	Current-To-Voltage Converter, Voltage-To-Current Converter	TEXT 1	12 Oct 2018	Counter Design as a Synthesis problem	TEXT 2
Module 2						
51	30 Oct 2018	Review of Basic Logic gates, Positive and Negative Logic, Introduction to HDL	TEXT 2	16 Oct 2018	A Digital Clock, Counter Design using HDL	TEXT 2
52	31 Oct 2018	Sum-of-Products Method, Truth Table to Karnaugh Map, Pairs Quads, and Octets	TEXT 2	23 Oct 2018	Variable, Resistor Networks, Resistor Networks	TEXT 2
53	2 Nov 2018	Karnaugh Simplifications, Don 't-care Conditions, Product-of-sums Method, Product-of-sums simplifications	TEXT 2	24 Oct 2018	Binary Ladders	TEXT 2
54	2 Nov 2018	Product-of-sums simplifications, Simplification by QuineMcClusky Method, Hazards and Hazard covers, HDL Implementation Models	TEXT 2	30 Oct 2018	D/A Converters, D/A Accuracy and Resolution	TEXT 2
Module 3						
55	7 Nov 2018	Multiplexers, Demultiplexers, 1-of-16 Decoder, BCD to Decimal Decoders, Seven Segment Decoders	TEXT 2	31 Oct 2018	A/D Converter-Simultaneous Conversion	TEXT 2
56	9 Nov 2018	Exclusive-OR Gates, Parity Generators and Checkers, Magnitude Comparator, Programmable Array Logic, HDL Implementation of Data Processing Circuits	TEXT 2	2 Nov 2018	A/D Techniques, Dual-slope A/D Conversion	TEXT 2

Period	Planned			Execution		
	Date	***Topic***	***Source material to be referred***	***Date***	***Topic***	***Source material to be referred***
57	9 Nov 2018	RS Flip-Flops, Gated Flip-Flops, Edge-triggered RS FLIP-FLOP	TEXT 2	2 Nov 2018	Dual-slope A/D Conversion, A/D Accuracy and Resolution	TEXT 2
58	13 Nov 2018	Edge-triggered D FLIP-FLOPs, Edge-triggered JK FLIPFLOPs	TEXT 2	5 Nov 2018	Junction Field Effect Transistors	TEXT 1
Module 4						
59	14 Nov 2018	JK Master-slave FLIP-FLOP, Switch Contact Bounce Circuits, Various Representation of FLIP-FLOPs, HDL Implementation of FLIP-FLOP	TEXT 2	13 Nov 2018	Biasing MOSFETs, MOSFETs	TEXT 1
60	15 Nov 2018	Serial In - Serial Out, Serial In - Parallel out, Parallel In -Serial Out, Universal Shift Register, Register implementation in HDL	TEXT 2	14 Nov 2018	FET Applications, CMOS Devices, Differences between JFETs and MOSFETs	TEXT 1
61	16 Nov 2018	Asynchronous Counters, DecodingGates, Synchronous Counters, Changing the Counter Modulus	TEXT 2	17 Nov 2018	Integrated Circuit(IC) Multivibrators	TEXT 1
Module 5						
62	16 Nov 2018	Decade Counters, Counter Design as a Synthesis problem, Counter Design using HDL	TEXT 2	19 Nov 2018	Ideal v/s practical Opamp, Performance Parameters	TEXT 1
63	20 Nov 2018	Variable, Binary Ladders, Resistor Networks, D/A Accuracy and Resolution	TEXT 2	20 Nov 2018	Performance Parameters	TEXT 1
64	22 Nov 2018	A/D Converter-Counter Method, Continuous A/D Conversion, A/D Techniques, A/D Accuracy and Resolution, Dual-slope A/D Conversion	TEXT 2	21 Nov 2018	Peak Detector Circuit, Comparator	TEXT 1

Period	Planned			Execution		
	Date	***Topic***	***Source material to be referred***	***Date***	***Topic***	***Source material to be referred***
Module 1						
65	23 Nov 2018	Junction Field Effect Transistors, MOSFETs, Biasing MOSFETs, FET Applications	TEXT 1	21 Nov 2018	Active Filters, NonLinear Amplifier	TEXT 1
66	23 Nov 2018	Integrated Circuit(IC) Multivibrators	TEXT 1	22 Nov 2018	Relaxation Oscillator, Current-To-Voltage Converter	TEXT 1
67	29 Nov 2018	Ideal v/s practical Opamp, Performance Parameters	TEXT 1	23 Nov 2018	Current-To-Voltage Converter, Voltage-To-Current Converter	TEXT 1
68	30 Nov 2018	Peak Detector Circuit, Comparator, Active Filters	TEXT 1	24 Nov 2018	Review of Basic Logic gates, Positive and Negative Logic, Introduction to HDL	TEXT 2
69	30 Nov 2018	Relaxation Oscillator, Current-To-Voltage Converter, Voltage-To-Current Converter, NonLinear Amplifier	TEXT 1	29 Nov 2018	Sum-of-Products Method, Truth Table to Karnaugh Map, Pairs Quads, and Octets	TEXT 2
70				30 Nov 2018	Karnaugh Simplifications, Don 't-care Conditions, Product-of-sums Method, Product-of-sums simplifications	TEXT 2

Module No.	*# of Classes Planned (till date)*	*Planned Effort (till date)*	*# of Classes Executed (till date)*	*Actual Effort (till date)*	*% Coverage*
2	20	18hrs 20min	20	18hrs 20min	100.0
3	20	18hrs 20min	20	18hrs 20min	100.0
4	10	9hrs 10min	10	9hrs 10min	100.0
5	10	9hrs 10min	10	9hrs 10min	100.0
1	10	9hrs 10min	10	9hrs 10min	100.0

Faculty in charge

HOD's Signature

Signature of Principal (&remarks if any)

PRINCIPAL
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225