ALVA'S
Education Foundation®

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

Computer Science and Engineering (CSE)

Course Name : Advanced Computer Architectures

Subject Name (Subject Code): 17CS72/15CS72

Class: VII A & B Sections

Dr.Manjunath Kotari & Mr. Madhusudhan S

Professor & Head, Sr. Asst. Professor

2020-21

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Computer Science and Engineering (CSE)

Faculty Details

Name	:	Dr. Manjunath Kotari & Mr. Madhusudhan S	
Qualification	:	Ph.D	M.Tech
Department	:	CSE	
Phone Number	:	9449586008	9480544177
Email ID	:	mkotari@aiet.org.in,madhusudhan@aiet.org.in	
Specimen Signature	:		

Alva's Institute of Engineering & Technology

Shobhavana Campus, Mijar, Moodbidri, D.K – 574225

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

ACADEMIC CALENDAR (2020-2021)-ODD

Sl.No	Departmental Activities	Dates
1.	Commencement of Online Classes	01st Sep, 2020
2.	Final Year Project Synopsis Submission	30th Sep, 2020
3.	FDP: FDP on "How to improve the Quality in Teaching Learning Process" (Online Mode)	2nd & 3rd Oct, 2020
4.	Submission of Assignment-1	Oct 2nd Week 2020
5.	Final year Project Screening	19th Oct, 2020
6.	**Alva's Technothon 2020**	**23rd Oct 2020 to 12th Nov, 2020**
7.	Final year Project Phase-I Evaluation	28th to 31st Dec, 2020
8.	Commencement of Offline Classes	17th Nov, 2020
9.	I.A Test -1	17th -19th Nov, 2020
10.	Submission of Assignment-2	Nov 3rd Week 2020
11.	Webinar on "How to crack Tech Giants "	20th Nov, 2020
12.	Submission of VTU- Non Credit Activity Report	30th Nov, 2020
13.	Webinar on "British Council IELTS for higher studies"	4th Dec,2020
14.	Webinar on "National Education Policy – Role of Teachers in Higher Education"	5th Dec, 2020
15.	Forum Activity: C Kaliyona for 2nd year Mechanical Students	2nd week of Dec, 2020
16.	Forum Activity: Linux Awareness for 1st year Chemistry Cycle	18th and 19th Dec,2020
17.	I.A Test -2	21st -23rd Dec, 2020
18.	Forum Activity: C Kaliyona for 2nd year Mechanical Students	Last week of Dec, 2020
19.	Forum Activity: Linux Awareness for 1st year Physics Cycle	01st and 02nd Jan,2021
20.	Submission of Assignment-3	Jan 2nd week 2021
21.	Technical Talk on "How to prepare for the Industries"	4th Jan, 2021
22.	Tech Club Activity: HTML Awareness for 1st year	4th & 6th Jan,2021
23.	Tech Club Activity: WarTecx Dept. Tech club event	8th & 9th Jan,2021
24.	I.A Test -3 for 3rd and final year students	13th -16th Jan, 2021
25.	I.A Test -3 for 2nd year students	15th – 17th Feb, 2021

Approved by HOD, CSE (IQAC Chairman)

H.O.D.
Dept. of Computer Science & Engineering
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY
Shobhavana Campus, Mijar, Moodbidri, D.K – 574225
Phone: 08258-262725, Fax: 08258-262726

Individual Faculty Time Table
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Academic Year	2020-21	Faculty Name	Dr.Manjunath Kotari (AMK)
Semester	ODD	Designation	Professor & Head

Time / Day	9.00 To 9.55	9.55 To 10.50	11.10 To 12.05	12.05 To 1.00	LUNCH BREAK	2.00 To 3.00	3.00 To 4.00	4.00 To 5.00
MON							ACA (7A)	
TUE			ACA (7A)					
WED		ACA (7A)						
THU								
FRI			ACA (7A)					
SAT		ACA (7A)						

UNITS:	Theory:10	LAB: --	Others: --	TOTAL UNITS: 10

Allocation of Subjects (Subjects with Subject Code)

17CS72	Advanced Computer Architecture (ACA)

Responsibilities

Head of the Department (H.O.D)

19/11/2020

Time Table Coordinator

H.O.D.
Dept. of Computer Science & Engineering
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

Head of the Department

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Individual Faculty Time Table
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Academic Year	2020-21	Faculty Name	Mr. Madhusudhan S.
Semester	ODD	Designation	Sr. Asst. Professor

Time / Day	9.00 To 9.55	9.55 To 10.50	11.10 To 12.05	12.05 To 1.00	LUNCH BREAK	2.00 To 3.00	3.00 To 4.00	4.00 To 5.00
MON	ACA (7B)		DAD (5B)			ADE LAB 3A B-1		
TUE						ADE LAB 3B B-1		
WED	ACA (7B)			DAD (5B)			SEMINAR 7B	
THU			DAD (5B)			ADE LAB 3A B-2		ACA (7B)
FRI	ACA (7B)			DAD (5B)		ADE LAB 3B B-2		
SAT			ACA (7B)					

UNITS:	Theory:18	LAB: 11	Others:01	TOTAL UNITS: 30

Allocation of Subjects (Subjects with Subject Code)

17CS72	Advanced Computer Architecture (ACA)
17CS564	Dot Net Framework for Application Development (DAD)

Responsibilities

Innovation & We Club, NBA- Criteria 4 , Student Review Paper

Time Table Coordinator 19/11/2020

Head of the Department

Dept. of CS&E
Alva's Institute of Engineering & Technology
Mijar, Moodbidri-574225

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Phone: 08258-262725, Fax: 08258-262726

Time Table

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Academic Year	Scheme	Semester	Section	Class Coordinator	Room No
2020-21	2017	VII	A	Mrs. Veena M.	312

Time / Day	9.00 To 9.55	9.55 To 10.50	10.50 To 11.10	11.10 To 12.05	12.05 To 1.00	1.00 To 2.00	2.00 To 3.00	3.00 To 4.00	4.00 To 5.00
MON	WTA	←----------WT LAB----------→				LUNCH	SAN	ACA	ML
TUE	WTA	ML		ACA	USP		←-----PROJECT/SEMINAR----→ [HK, KSU, SSJ, MDH]		
WED	WTA	ACA		SAN	ML		USP	PROJECT/SEMINAR [HK, SH, KSU, VM,VKT]	
THU	ML	SAN		WTA	USP		←----------ML LAB----------→		
FRI	SAN	USP		ACA	ML		←-----PROJECT/SEMINAR----→ [HK, MBS, SSJ, PR]		
SAT	SAN	ACA		USP	WTA				

Allocation of Subjects

Subjects			Staffs	Staff Code
17CS71	WTA	Web Technology and its Applications	Dr.Mohideen Badhusha S.	MBS
17CS72	ACA	Advanced Computer Architecture	Dr. Manjunath Kotari	AMK
17CS73	ML	Machine Learning	Mrs. Veena M	VM
17CS744	USP	Unix System Programming	Mr. Venkatesh	VKT
17CS754	SAN	Storage Area Network	Ms. Megha D. Hegde	MDH
17CSL76	ML LAB	Machine Learning Lab	Mrs. Veena M Ms. Megha D. Hegde	VM MDH
17CSL77	WT LAB	Web Technology Laboratory with Mini Project	Dr.Mohideen Badhusha S. Mr. Abdul Khader	MBS AK
17CSP78	PROJECT WORK/ SEMINAR	Project Phase –I/ Seminar	Mr. Harish Kunder Dr. Mohideen Badhusha S. Mr. Venkatesh Mr.Konanki Surendra Ms. Shruthi Shetty J. Ms. Megha D. Hegde Mrs. Veena M. Ms. Pranitha	HK MBS VKT KSU SSJ MDH VM PR

19/11/2020

Time Table Coordinator

H.O.D.
Dept. Of Computer Science & Engineering
Alva's Institute of Engg. & Technology
H.O.D

PRINCIPAL
Principal
Alva's Institute of Engg. & Technology

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

Shobhavana Campus, Mijar, Moodbidri, D.K – 574225

Time Table with effect from 01/09/2020

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Academic Year	Scheme	Semester	Section	Room No		Class Coordinator	
2020-21	2017	VII					

Time / Day	9.00 To 9.50	10.00 To 10.50	11.00 To 11.50	12.00 To 12.50	1.00 To 2.00	2.00 To 3.00	3.00 To 4.00	4.00 To 5.00
MON	WT	ACA	ML	USP	LUNCH	SEMINAR/PROJECT		
TUE	SAN	USP	ACA	ML		WT LAB		
WED	ML	WT	SAN	USP		SEMINAR/PROJECT		
THU	WT	SAN	USP	ACA		ML LAB		
FRI	SAN	ML	ACA	WT		USP	SEMINAR/PROJECT	
SAT	ML	WT	ACA	SAN				

Allocation of Subjects

Subjects			Staffs	Staff Code
17CS71	WT	Web Technology and its Applications	Dr.Mohideen Badhusha S.	MBS
17CS72	ACA	Advanced Computer Architecture	Dr. Manjunath Kotari	AMK
17CS73	ML	Machine Learning	Mr.Sayeesh	SS
17CS744	USP	Unix System Programming	Mr. Venkatesh	VKT
17CS754	SAN	Storage Area Network	Mr. Vivek Sharma S.	VSS
17CSL76	ML LAB	Machine Learning Lab	Mr.Sayeesh	SS
17CSL77	WT LAB	Web Technology Laboratory with Mini Project	Dr.Mohideen Badhusha S.	MBS
17CSP78	SEMINAR/ PROJECT	Project Phase -I /Seminar	Mr.Harish Kunder Mrs. Vidya	HK VD

Time Table Coordinator 28/8/2020

Head of the Department 28/8/2020

Dept. Of Computer Science & Engg.
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

Principal

PRINCIPAL
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225, D.K

ADVANCED COMPUTER ARCHITECTURES
[As per Choice Based Credit System (CBCS) scheme]
(Effective from the academic year 2017 - 2018)
SEMESTER – VII

Subject Code	17CS72	IA Marks	40
Number of Lecture Hours/Week	4	Exam Marks	60
Total Number of Lecture Hours	50	Exam Hours	03

CREDITS – 04

Module – 1	**Teaching Hours**
Theory of Parallelism: Parallel Computer Models, The State of Computing, Multiprocessors and Multicomputer ,Multivector and SIMD Computers ,PRAM and VLSI Models, Program and Network Properties ,Conditions of Parallelism, Program Partitioning and Scheduling, Program Flow Mechanisms, System Interconnect Architectures, Principles of Scalable Performance, Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches.	**10 Hours**
Module – 2	
Hardware Technologies: Processors and Memory Hierarchy, Advanced Processor Technology, Superscalar and Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology.	**10 Hours**
Module – 3	
Bus, Cache, and Shared Memory ,Bus Systems ,Cache Memory Organizations ,Shared Memory Organizations ,Sequential and Weak Consistency Models ,Pipelining and Superscalar Techniques ,Linear Pipeline Processors ,Nonlinear Pipeline Processors ,Instruction Pipeline Design ,Arithmetic Pipeline Design (Upto 6.4).	**10 Hours**
Module – 4	
Parallel and Scalable Architectures: Multiprocessors and Multicomputers ,Multiprocessor System Interconnects, Cache Coherence and Synchronization Mechanisms, Three Generations of Multicomputers ,Message-Passing Mechanisms ,Multivector and SIMD Computers ,Vector Processing Principles ,Multivector Multiprocessors ,Compound Vector Processing ,SIMD Computer Organizations (Upto 8.4),Scalable, Multithreaded, and Dataflow Architectures, Latency-Hiding Techniques, Principles of Multithreading, Fine-Grain Multicomputers, Scalable and Multithreaded Architectures, Dataflow and Hybrid Architectures.	**10 Hours**
Module – 5	
Software for parallel programming: Parallel Models, Languages, and Compilers ,Parallel Programming Models, Parallel Languages and Compilers ,Dependence Analysis of Data Arrays ,Parallel Program Development and Environments, Synchronization and Multiprocessing Modes. Instruction and System Level Parallelism, Instruction Level Parallelism ,Computer Architecture ,Contents, Basic Design Issues ,Problem Definition ,Model of a Typical Processor ,Compiler-detected Instruction Level Parallelism ,Operand Forwarding ,Reorder Buffer, Register Renaming ,Tomasulo's Algorithm ,Branch Prediction, Limitations in Exploiting Instruction Level Parallelism ,Thread Level Parallelism.	**10 Hours**
Course outcomes: The students should be able to:	

• Understand the concepts of parallel computing and hardware technologies • Illustrate and contrast the parallel architectures • Recall parallel programming concepts
Question paper pattern The question paper will have ten questions. There will be 2 questions from each module. Each question will have questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.
Text Books: 1. Kai Hwang and Naresh Jotwani, Advanced Computer Architecture (SIE): Parallelism, Scalability, Programmability, McGraw Hill Education 3/e. 2015
Reference Books:
1. John L. Hennessy and David A. Patterson, Computer Architecture: A quantitative approach, 5th edition, Morgan Kaufmann Elseveir, 2013

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Phone: 08258-262725, Fax: 08258-262726

Department of Computer Science and Engineering

SEMESTER VII

Course Code: **17CS72** | Course Name: **Advanced Computer Architectures(ACA)**

Course Teacher: **Dr. Manjunath Kotari**

Course Outcomes: After studying this course, students will be able to:

CO Numbers	Course Outcomes	Blooms Level	Target Level
17CS72.1	**Differentiate** the parallel computer models and **Identify** the performance metrics of scalable parallel computers.	Apply (L3)	2
17CS72.2	**Analyse** the various hardware technologies using processors and memory hierarchy.	Analyse (L4)	2
17CS72.3	**Distinguish** the performance of pipelining and non-pipelining environment in a processor	Apply (L3)	2
17CS72.4	**Compare** and **contrast** the parallel and scalable architectures	Apply (L3)	2
17CS72.5	**Demonstrate** the software for parallel programming concepts	Apply (L3)	2

CO-PO/CO-PSO Mapping Matrix:

CO Numbers	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	2	1	2								1	2	2	
CO2	2	2	1	1		1						2		1	1
CO3	2	2	2	1								1	1	2	
CO4	2	2	2	2								1	1	2	
CO5	2	2	2	1	1	1						2	1	1	
Avg	2	2	1.6	1.4	1	1						1.4	1.25	1.6	1

CO-PO/CO-PSO Mapping Matrix Justification: Student should have

CO Numbers	Justification	
17CS72.1	PO1	Moderately applying engineering knowledge about parallel computing to solve simple problems.
	PO2	Moderately analyse the problems of parallel computing and performance metrics
	PO3	Low level of design & development of theory of parallelism
	PO4	Moderately applied for research based knowledge of theory of parallelism
	PO12	Low level of mapping for lifelong learning of theory of parallelism
	PSO1	Moderately mapped for professional skills with respect to parallel computing
	PSO2	Moderately mapped for problem solving in parallel computing
17CS72.2	PO1	Adequate knowledge on memory technologies and processors to analyse related problems of processors.
	PO2	Moderate knowledge on problem analysis of hardware technologies
	PO3	Low mapping to design & development of solutions because here student are able to understand the technologies
	PO4	Low level of research knowledge assessed about memory and processor technologies
	PO6	Low level of engineer and society is required to judge the hardware technologies

	PO12	Moderate level of life long learning will be developed for further usages of parallel programming concepts in different software development.
	PSO1	Slightly professional skills will be developed after use of parallel programming concepts
	PSO2	Slightly problem solving skills will be developed after use of parallel programming concepts

Course Teacher
Signature with date

IQAC Member
Signature with date

IQAC Chairman
Signature with date

	PO12	Moderate level of lifelong learning to learn about architecture technologies
	PSO2	Low level of problem solving skills required in hardware technologies
	PSO3	Low level of entrepreneurship knowledge is required for hardware technologies
17CS72.3	PO1	Moderate engineering knowledge is needed to apply the operation of performance enhancements in ILP.
	PO2	Moderate problem analysis is needed to apply the operation of performance enhancements in ILP.
	PO3	Moderately mapped for design & development of solutions to apply the operation of performance enhancements in ILP.
	PO4	Low level is mapped for Conduct investigations of complex problems to apply the operation of performance enhancements in ILP.
	PO12	Low level is mapped for Lifelong learning because apply the operation of performance enhancements in ILPs are very less.
	PSO1	Low level is mapped for Professional Skills because apply the operation of performance enhancements in ILPs.
	PSO2	Moderate level of problem solving skills required to apply performance enhancements of ILPs
17CS72.4	PO1	Sufficient Engineering knowledge enough to distinguish between the different architecture.
	PO2	Moderate level problem analysis enough to compare the different architectures
	PO3	Moderate level design & development is needed to conclude the features of the different architectures
	PO4	Moderate level research based analysis is needed to compare the features of the different architectures
	PO12	Slight lifelong learning will be required to distinguish between the architectures
	PSO1	Slight professional skills will be developed for comparing the different architectures
	PSO2	Moderate level problem solving skills will be developed after comparing the different architectures
17CS72.5	PO1	Enough engineering knowledge is required on Software for parallel programming concepts.
	PO2	Sufficient problem analysis is needed to write problem statement on Software for parallel programming concepts.
	PO3	Moderate level of design & development of solutions needed on Software for parallel programming concepts.
	PO4	Slight research based analysis is required to understand the Software for parallel programming concepts.
	PO5	Slight modern tool will be used to analyse the parallel programming concepts.
	PO6	Slight engineer & society needs will be analysed here understand the Software for parallel programming concepts.

Lesson Delivery Plan, Execution Status and Progress Monitoring

Academic Year: 2020-21 Semester: VII Subject code: 17CS72/15CS72

Name of the Faculty: Dr.Manjunath Kotari & Mr. Madhusudhan S Subject: Advanced Computer Architectures

Hrs required as per Syllabus: 50 hrs Additional Classes required: 10

Lesson Delivery Plan		Execution Status		Progress Monitoring
Module No : 1.				
Planned Start Date : 01/09/2020 ***Planned Completion Date: 21/09/2020*** ***Planned Hrs : 10*** ***Actual Hrs:12***				
Class No	*Portion to be covered per hour*	*Regular Class Date*	*Extra Class Date*	*Content Beyond the Syllabus to fill the Gap*
01	Parallel Computer Models, The State of Computing	01/09/20		Introduction to MIPS Processor Architecture using QtSpim simulator. Assignment Questions on above topics
02	Multiprocessors and Multicomputer ,Multivector and SIMD Computers	03/09/20		
03	PRAM and VLSI Models, Program and Network Properties	04/09/20		
04	Conditions of Parallelism,Program Partitioning and Scheduling	07/09/20	09/09/20	
05	Program Flow Mechanisms, System Interconnect Architectures	11/09/20		
06	Principles of Scalable Performance	14/09/20		
07	Performance Metrics and Measures	16/09/20		
08	Parallel Processing Applications	18/09/20	21/09/20	
09	Speedup Performance Laws	23/09/20		
10	Scalability Analysis and Approaches	28/09/20		

Lesson Delivery Plan		Execution Status		Progress Monitoring
Module No : 2.				
Planned Start Date : 23/09/2020		***Planned Completion Date:21/10/2020***		***Planned Hrs : 10 Actual Hrs:13***
Class No	*Portion to be covered per hour*	*Regular Class Date*	*Extra Class Date*	*Content Beyond the Syllabus to fill the Gap*
01	Processors and Memory Hierarchy	30/09/20		Case Study of Various Architectures :- ARM vs ATOM Processors, Intel Processors – Pentium Pro I/II/III, Intel Processors – Pentium-4, M
02	Processors and Memory Hierarchy	01/10/20	05/10/20	
03	Advanced Processor Technology	06/10/20		
04	Advanced Processor Technology	08/10/20		
05	Superscalar and Vector Processors	12/10/20	14/10/20	
06	Superscalar and Vector Processors	15/10/20		
07	Memory Hierarchy Technology	19/10/20		
08	Memory Hierarchy Technology	21/10/20		
09	Virtual Memory Technology	22/10/20	26/10/20	
10	Virtual Memory Technology	27/10/20		

Lesson Delivery Plan		Execution Status		Progress Monitoring
Module No : 3.				
Planned Start Date :22/10/2020	***Planned Completion Date: 16/11/2020***		***Planned Hrs : 10***	***Actual Hrs:12***
Class No	*Portion to be covered per hour*	*Regular Class Date*	*Extra Class Date*	*Content Beyond the Syllabus to fill the Gap*
01	Bus Systems	28/10/20		Case Study of : Intel Processors – i5 vs i7, Intel Processors – Core2-Duo vs i3
02	Bus Systems	02/11/20		
03	Cache Memory Organizations	05/11/20	06/11/20	
04	Shared Memory Organizations	09/11/20		
05	Sequential and Weak Consistency Models	11/11/20		
06	Pipelining and Superscalar Techniques	12/11/20		
07	Linear Pipeline Processors	16/11/20	17/11/20	
08	Nonlinear Pipeline Processors	19/11/20		
09	Instruction Pipeline Design	20/11/20		
10	Arithmetic Pipeline Design	23/11/20		

Lesson Delivery Plan		Execution Status		Progress Monitoring
Module No : 4.				
Planned Start Date : 17/11/2020		***Planned Completion Date: 07/12/2020***		***Planned Hrs : 10 Actual Hrs:13***
Class No	*Portion to be covered per hour*	*Regular Class Date*	*Extra Class Date*	*Content Beyond the Syllabus to fill the Gap*
01	Multiprocessors and Multicomputers, Multiprocessor System Interconnects	24/11/20	25/11/20	~~NIL~~ Conducted Technical talk on Introduction to Parallel Computing - By Dr. Ansh S Anand IIIT Allahabad 5th NOV, 2020.
02	Cache Coherence and Synchronization Mechanisms,	27/11/20		
03	Message-Passing Mechanisms ,Multivector and SIMD Computers	28/11/20		
04	Vector Processing Principles ,Multivector Multiprocessors	30/11/20		
05	Compound Vector Processing ,SIMD Computer Organizations	01/12/20	02/12/20	
06	Scalable, Multithreaded	04/12/20		
07	Dataflow Architectures, Latency- Hiding Techniques	05/12/20		
08	Principles of Multithreading, Fine-Grain Multicomputers	07/12/20		
09	Scalable and Multithreaded Architectures	08/12/20	09/12/20	
10	Dataflow and Hybrid Architectures	11/12/20		

Lesson Delivery Plan		Execution Status		Progress Monitoring
Module No : 5.				
Planned Start Date :08/12/2020	*Planned Completion Date:24/01/2020*		*Planned Hrs : 10*	*Actual Hrs:18*
Class No	*Portion to be covered per hour*	*Regular Class Date*	*Extra Class Date*	*Content Beyond the Syllabus to fill the Gap*
01	Parallel Models, Languages, and Compilers	12/12/20		~~NIL~~ Conducted Webinar on Computer Arch. & Pgrmg Dr. Sharad Sinha IIT Goa 25th Oct, 2020. Online mode
02	Parallel Programming Models, Parallel Languages and Compilers ,Dependence Analysis of Data Arrays	14/12/20	15/12/20	
03	Parallel Program Development and Environments, Synchronization and Multiprocessing Modes Instruction and System Level Parallelism	16/12/20	17/12/20	
04	Instruction Level Parallelism ,Computer Architecture	18/12/20	19/12/20	
05	Contents, Basic Design Issues	24/12/20	26/12/20	
06	Problem Definition ,Model of a Typical Processor	28/12/20	29/12/20	
07	Compiler-detected Instruction Level Parallelism ,Operand Forwarding	30/12/20	01/01/21	
08	Reorder Buffer, Register Renaming	02/01/21	04/01/21	
09	Tomasulo's Algorithm ,Branch Prediction	05/01/21	06/01/21	
10	Limitations in Exploiting Instruction Level Parallelism ,Thread Level Parallelism	07/01/21		

Consolidated Report:

No. of classes planned	No. of classes Taken
50	68

Signature of the faculty

VII Sem CSE A-Section

SL.NO	USN	NAME OF THE STUDENT
1.	4AL16CS047	MADUSHREE R
2.	4AL17CS002	AJEYASHREE K
3.	4AL17CS005	AMRUTHA M
4.	4AL17CS007	ANUSHA
5.	4AL17CS010	APEKSHA RAJENDRA RANE
6.	4AL17CS012	APOORVA K N
7.	4AL17CS015	ASHA RUDRAPPA TOTAGI
8.	4AL17CS019	BHRAMARI P SHETTY
9.	4AL17CS020	CHANDANA PATIL
10.	4AL17CS021	CHETANA H
11.	4AL17CS028	DHEERAJ KRISHNA DEVADIG
12.	4AL17CS030	GAYATRI V KAMAT
13.	4AL17CS034	JAGATH HAREN
14.	4AL17CS035	JAYALAKSHMI M
15.	4AL17CS040	KAVANA V
16.	4AL17CS044	KOUSHIK S N
17.	4AL17CS046	LIKITHA M
18.	4AL17CS048	MADAN G GUDIGAR
19.	4AL17CS050	MHASKE POOJA SAMBHAJI
20.	4AL17CS051	MAHEK SABHA
21.	4AL17CS052	NAGASHREE ARUN M
22.	4AL17CS055	NETRA SURESH GUDAGAMNALA

23.	4AL17CS062	PRANAV L M
24.	4AL17CS066	PRIYA H T
25.	4AL17CS067	PRIYANKA KILLEDAR
26.	4AL17CS070	RACHANA K N
27.	4AL17CS071	RAGHAVI HARISCHANDRA GAONKAR
28.	4AL17CS073	RAKSHA S
29.	4AL17CS075	RANI M D
30.	4AL17CS076	RAVALI P
31.	4AL17CS077	ROHAN MAHAVEER
32.	4AL17CS080	SACHIN RAJORA
33.	4AL17CS081	SANA F HABIB
34.	4AL17CS089	SHETTY SATHVIK RAVINDRA
35.	4AL17CS090	SHILPA S U
36.	4AL17CS091	SHREETAL KALABANDI
37.	4AL17CS092	SHRINIVASA
38.	4AL17CS093	SHWETHA M S
39.	4AL17CS095	SNEHA K BAKALE
40.	4AL17CS097	SPOORTHI M S
41.	4AL17CS100	SUHAS M S
42.	4AL17CS101	SURYA PRAKASH S
43.	4AL17CS104	SYED HUDAIF IBRAHIM
44.	4AL17CS108	VIHA B RAJU
45.	4AL17CS109	VIKAS A L

46.	4AL17CS112	VINOD KUMAR
47.	4AL17CS115	SUMAN RATHOD
48.	4AL17CS116	SAHANA C
49.	4AL17CS117	SINCHANA
50.	4AL17CS119	NACHIKETH S BHAT
51.	4AL17CS120	B SAI HARSHA
52.	4AL17CS122	RAVI MATH
53.	4AL18CS401	SANDHYA KAPSE

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VII Semester CSE B-Section

SL.NO	USN	NAME OF THE STUDENT
1.	4AL14CS040	M G SHWETHA
2.	4AL15CS026	DARSHAN M
3.	4AL15CS061	NAOREM LAXMI DEVI
4.	4AL16CS015	ANUSHA P S
5.	4AL16CS063	POOJA RAJEEV
6.	4AL16CS113	TANOJ M
7.	4AL16CS078	HARSHITH S
8.	4AL17CS003	AKSHAT KHANDELWAL
9.	4AL17CS004	AKSHATA NARAYANA HEGDE
10.	4AL17CS006	ANILKUMAR B N
11.	4AL17CS008	ANVITHA POOJARY
12.	4AL17CS009	ANVITHA U
13.	4AL17CS011	APOORVA H P
14.	4AL17CS013	ARUNA K
15.	4AL17CS016	ASHIKA
16.	4AL17CS017	ASHWINI
17.	4AL17CS018	ASHWINI SHEKARAPPA JADAMALI
18.	4AL17CS022	CHETHANA J
19.	4AL17CS024	D JASMINE JOYLINE
20.	4AL17CS025	DATTA KIRAN A B
21.	4AL17CS027	DHANYA BHAT

22.	4AL17CS029	DSOUZA ELSTON RONALD
23.	4AL17CS031	GOWDA ROSHNI SHIVPRAKASH
24.	4AL17CS033	HEMALATHA S
25.	4AL17CS036	JAYRAJ CHIRAG KUMAR SHAH
26.	4AL17CS037	JOHN ALSTEN TAURO
27.	4AL17CS038	K THRISHUL
28.	4AL17CS039	KANAKA B S
29.	4AL17CS041	KAVYA
30.	4AL17CS042	KAVYA R SHETTY
31.	4AL17CS045	LATHIK MOGER
32.	4AL17CS047	M C SUCHITHRA HEGGADE
33.	4AL17CS053	NAIK NAYANA GANAPATI
34.	4AL17CS054	NANDITHA R SHETTY
35.	4AL17CS056	PALLAVI
36.	4AL17CS057	PAVANA P
37.	4AL17CS059	PRAJNA
38.	4AL17CS063	PRAVEEN KUMAR S
39.	4AL17CS065	PREETHI
40.	4AL17CS074	RAMITHA Y S
41.	4AL17CS078	ROHAN VASHISTA B M
42.	4AL17CS079	ROUSHA
43.	4AL17CS083	SHAH DHRUVIL AMIT
44.	4AL17CS084	SHAIFA SHALA

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Academic Year 2020-21

45.	4AL17CS085	SHANBHAG ATISH MANOJ
46.	4AL17CS086	SHETTY ANKIT SURESH
47.	4AL17CS087	SHETTY DISHA RAVINDRA
48.	4AL17CS094	SINDHU N
49.	4AL17CS096	SOUNDARYA R
50.	4AL17CS098	SPOORTHI BALAJI
51.	4AL17CS099	SHRILATHA K KAMATH
52.	4AL17CS102	SUSHMITHA
53.	4AL17CS103	SUSHMITHA B POOJARY
54.	4AL17CS106	VARSHITHA
55.	4AL17CS107	VIDYA K C
56.	4AL17CS114	NIRIKSHA A
57.	4AL17CS118	JAIDITYA Y
58.	4AL17CS123	PRUTHVI B C
59.	4AL18CS400	SAGAR B V

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DEPARTMENT OF COMPUTER SCIENCEAND ENGINEERING

I-INTERNAL

Semester:7
Subject: **Advanced Computer Architectures (17CS72/15CS72)**
MaxMarks:**30**
Faculty: **Dr.Manjunath Kotari**

Date: **17/11/2020**
Time: **03:00 PM-04:30 PM**

Answer any 2 full questions selecting one full question from each part

Question#		Question	Marks	CO	BT CL

PART-A

1. a Discuss the elements of modern computer systems with diagram. — 7 — CO1 — L

b Consider the execution of an object code with 200,000 instructions on a 40-MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment:

Instruction type	CPI	Instruction mix
Arithmetic and logic	1	60%
Load/store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

— 8 — CO1 — L

i) Calculate the average CPI when the program is executed on a uniprocessor with the above trace results.
ii) Calculate the corresponding MIPS rate based on the CPI obtained in part (i).

OR

2. a Explain any two types of shared memory processors with diagram — 7 — CO1

b A 40-MHz processor was used to execute a benchmark program with the following instructions mix and clock cycle counts:

Instruction Type	Instruction Count	Clock Cycle Count
Integer Arithmetic	5000	1
Data Transfer	3000	2
Floating Point	1500	2
Control Transfer	4000	3

— 8 — CO1

Determine the effective CPI, MIPS Rate and Execution Time for this program.

PART-B

3. a Discuss the various static interconnection network with bisection width, node degree, diameter and number of links. — 7 — CO1

b Design a Baseline Network of 16x16 by showing the calculation such as number of stages and type of network is static or dynamic? — 8 — CO1

OR

4. a Discuss the degree of parallelism & Average Parallelism with example — 7 — CO1

b Discuss the Amdahl's Law for a Fixed Workload. — 8 — CO1

Faculty 13/11/20 | HOD 13/11/20 | Principal 13/11/20

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY, MOODBIDRI

DEPARTMENT OF COMPUTER SCIENCEAND ENGINEERING

I-INTERNAL ASSESSMENT TEST

Subject: ADVANCED COMPUTER ARCHITECTURES (17CS72/15CS72) Date: 17/11/2020

Max Marks: 30 Time: 03:00 PM – 04:30 PM

Faculty: Dr.MANJUNATH KOTARI /Mr. MADHUSUDHAN. S Semester: 7

Note: Answer any TWO full Questions.

1 a	Discuss the elements of modern computer systems with diagram	7	CO1	L2
Ans	**Elements of Modern Computers:** The hardware, software, and programming elements of modern computer systems can be characterized by looking at a variety of factors, including: • Computing problems • Algorithms and data structures • Hardware resources • Operating systems • System software support • Compiler support			

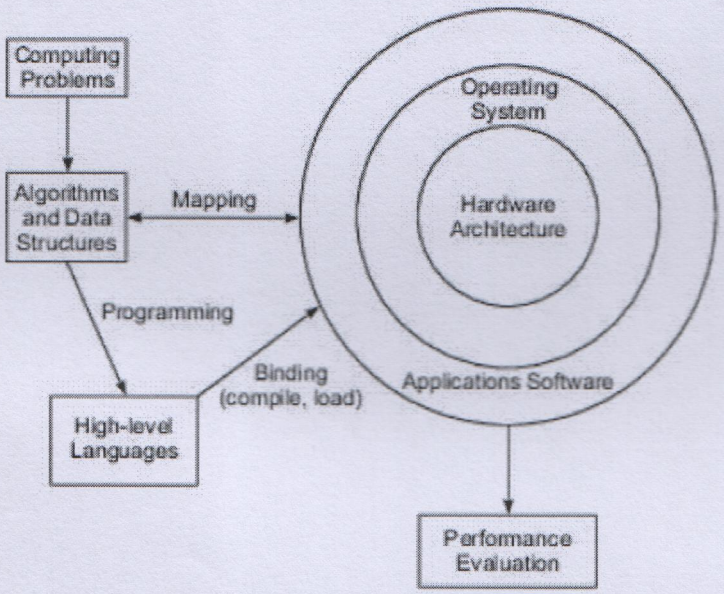


Fig. 1.1 Elements of a modern computer system

1 b	Consider the execution of an object code with 200,000 instructions on a 40-MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment: i) Calculate the average CPI when the program is executed on a uniprocessor with the above trace results. ii)Calculate the corresponding MIPS rate based on the CPI obtained in part (i).	8	CO1	L3

Instruction Type	CPI	Instruction Mix
Arithmetic & Logic	1	60%
Load Store	2	18%
Branch	4	12%
Memory Reference	8	10%

Ans

(i) Average CPI	$\textbf{Average CPI} = \frac{\textbf{Instruction Count x Clock Cycle Count}}{\textbf{Total Instructin Count}}$ **= (0.6 * 1) + (0.18 * 2) + (0.12 * 4) + (0.1 * 8)** **= 0.6 + 0.36 + 0.48 + 0.8 = 2.24**
(ii) MIPS Rate	**MIPS Rate = f /(CPI * 10^6)** **= (40 * 10^6) / (2.24 * 10^6)** **= 17.86**

2 a	Explain any two types of shared memory processors with diagram	7	CO1	L2

Ans

Shared-memory multiprocessor models:

- Uniform-memory-access (UMA)
- Non-Uuniform-Memory-access (NUMA)
- Cache-only memory architecture (COMA)

2 b

A 40-MHz processor was used to execute a benchmark program with the following instructions mix and clock cycle counts:

Instruction Type	Instruction Count	Clock Cycle Count
Integer Arithmetic	5000	1
Data Transfer	3000	2
Floating Point	1500	2
Control Transfer	4000	3

Determine the effective CPI, MIPS Rate and Execution Time for this program.

Ans

Average CPI= (5000 x 1+3000 x 2+1500 x 2+ 4000 x 3)/ (5000+3000+1500+ 4000)

= 1.92

MIPS Rate = f/ CPI*10^6

= (40 * 10^6) / (1.92 * 10^6)

= 20.76 MIPS

Execution Time = T = $I_c \times CPI \times \tau$.

= 13500x1.92x1/40x10^6

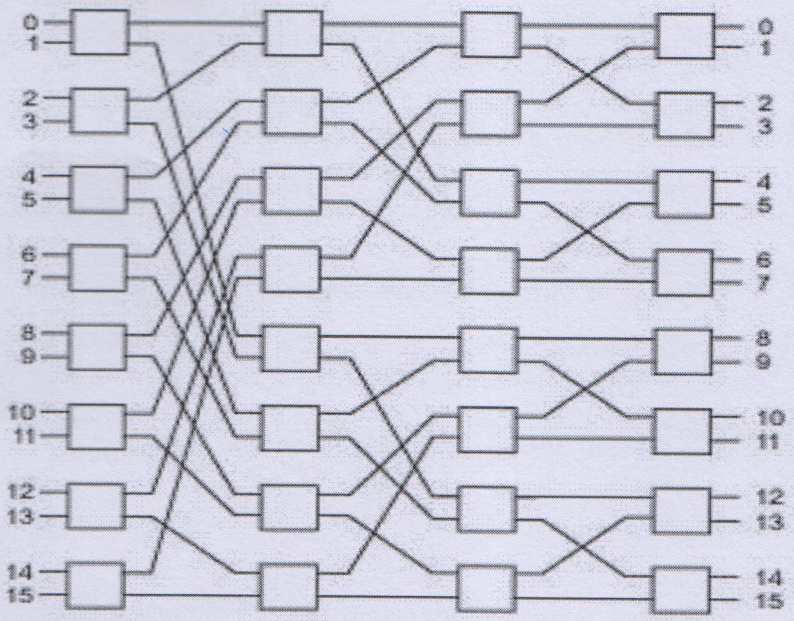
= 64.8 x 10^{-3} s

3 a	Discuss the various static interconnection network with bisection width, node degree, diameter and number of links.	7	CO1	L2

Ans

Table 2.2 *Summary of Static Network Characteristics*

Network type	*Node degree, d*	*Network diameter*	*No. of links, l*	*Bisection width, B*	*Symmetry*	*Remarks on network size*
Linear Array	2	$N-1$	$N-1$	1	No	N nodes
Ring	2	$\lfloor N/2 \rfloor$	N	2	Yes	N nodes
Completely Connected	$N-1$	1	$N(N-1)/2$	$(N/2)^2$	Yes	N nodes
Binary Tree	3	$2(h-1)$	$N-1$	1	No	Tree height $h = \lceil \log_2 N \rceil$
Star	$N-1$	2	$N-1$	$\lfloor N/2 \rfloor$	No	N nodes
2D-Mesh	4	$2(r-1)$	$2N-2r$	r	No	$r \times r$ mesh where $r = \sqrt{N}$
Illiac Mesh	4	$r-1$	$2N$	$2r$	No	Equivalent to a chordal ring of $r = \sqrt{N}$
2D-Torus	4	$2\lfloor r/2 \rfloor$	$2N$	$2r$	Yes	$r \times r$ torus where $r = \sqrt{N}$
Hypercube	n	n	$nN/2$	$N/2$	Yes	N nodes, $n = \log_2 N$ (dimension)
CCC	3	$2k-1+\lfloor k/2 \rfloor$	$3N/2$	$N/(2k)$	Yes	$N = k \times 2^k$ nodes with a cycle length $k \geq 3$
k-ary n-cube	$2n$	$n\lfloor k/2 \rfloor$	nN	$2k^{n-1}$	Yes	$N = k^n$ nodes

3 b	Design a Baseline Network of 16x16 by showing the calculation such as number of stages and type of network is static or dynamic?	8	CO1	L3
Ans	16x16 Baseline Network A Base-line network can be generated recursively. The first stage contains one N x N block and the second stage contains two (N/2) x (N/2) sub blocks, labeled C0, and C1. The construction process can be recursively applied to the subblocks until the M2 subblocks size 2 X 2 are reached.  			
4 a	Discuss the degree of parallelism & Average Parallelism with example	7	CO1	L2
Ans	***Degree of Parallelism*** The execution of a program on a parallel computer may use different numbers of processors at different time periods during the execution cycle. For each time period, the number of processors used to execute a program is defined as the *degree of parallelism* (DOP). This is a discrete time function, assuming only nonnegative integer values. The total amount of work W (instructions or computations) performed is proportional to the area under the profile curve: $$W = \Delta \int_{t_1}^{t_2} DOP(t)\, dt \quad (3.1)$$ This integral is often computed with the following discrete summation: $$W = \Delta \sum_{i=1}^{m} i \cdot t_i \quad (3.2)$$ where t_i is the total amount of time that DOP $= i$ and $\sum_{i=1}^{m} t_i = t_2 - t_1$ is the total elapsed time. The *average parallelism A* is computed by $$A = \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} DOP(t)\, dt \quad (3.3)$$ In discrete form, we have $$A = \left(\sum_{i=1}^{m} i \cdot t_i \right) \Big/ \left(\sum_{i=1}^{m} t_i \right) \quad (3.4)$$			

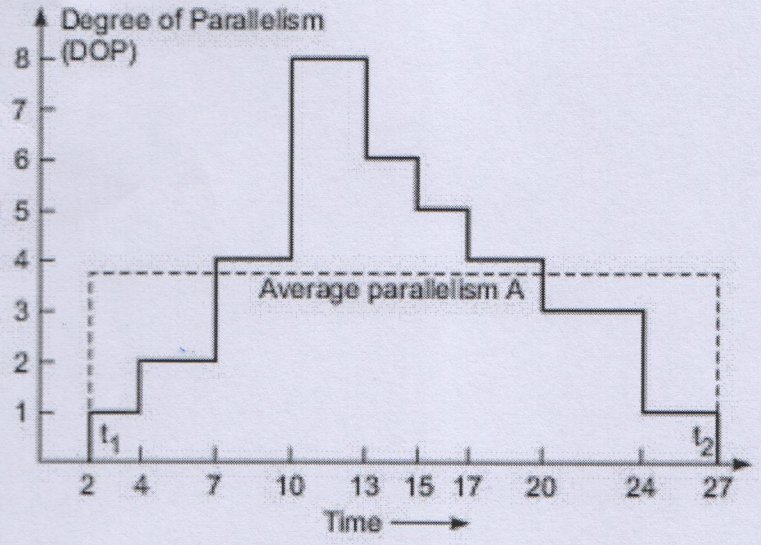


Fig. 3.1 Parallelism profile of a divide-and-conquer algorithm

In Fig. 3.1, the average parallelism $A = (1 \times 5 + 2 \times 3 + 3 \times 4 + 4 \times 6 + 5 \times 2 + 6 \times 2 + 8 \times 3)/(5 + 3 + 4 + 6 + 2 + 2 + 3) = 93/25 = 3.72$. In fact, the total workload $W = A\Delta\ (t_2 - t_1)$, and A is an upper bound of the asymptotic speedup to be defined below.

4 b	Discuss the Amdahl's Law for a Fixed Workload.	8	CO1	L2

Ans

Amdahl's Law for a Fixed Workload

- In many practical applications, the computational workload is often fixed with a fixed problem size.
- As the number of processors increases in a parallel computer, the fixed load is distributed to more processors for parallel execution.
- Minimal turnaround time is the primary goal.
- Speedup obtained for time-critical applications is called fixed-load speedup.
- Execution time & Response Time

$$t_i(n) = \frac{W_i}{i\Delta}\left\lceil \frac{i}{n} \right\rceil$$

$$T(n) = \sum_{i=1}^{m} \frac{W_i}{i\Delta}\left\lceil \frac{i}{n} \right\rceil$$

- Note that if i < n, then $t_i(n) = t_i(\infty) = W_i/i\Delta$.

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DEPARTMENT OF COMPUTER SCIENCEAND ENGINEERING

II-INTERNAL ASSESSMENT TEST

Subject: ADVANCED COMPUTER ARCHITECTURES (17CS72/15CS72) Date: 21/12/2020
Max Marks: 30 Time: 03:00 PM – 04:30 PM
Faculty: Mr. MADHUSUDHAN. S/Dr.MANJUNATH KOTARI Semester: 7

Answer any 2 full questions

Question#		Question	Marks	CO	BT/CL
		Part-A			
1.	a	With a diagram explain the hierarchical memory technology.	7	CO2	L2
	b	Explain typical superscalar RISC processor architecture	8	CO2	L2
		OR			
2.	a	Give the characteristics of symbolic processors	7	CO2	L2
	b	Illustrate page replacement policies with the help of an example.	8	CO2	L3
		Part- B			
3.	a	Explain bus arbitration and its types in multiprocessor systems.	7	CO3	L2
	b	Consider the following pipelined processor within 3 stages this pipeline has total evaluation time of 8 clock cycles. All successor stages must be used after each clock cycle.	8	CO3	L3

	0	1	2	3	4	5	6	7	8
S1	X								X
S2		X	X						
S3				X					
S4					X	X			
S5							X	X	

(i) List the set of forbidden latencies between task initiations.
(ii) Draw the state diagram which shows all possible latency cycles.
(iii) List all greedy cycles.
(iv) Determine the value of MAL & MCL.

OR

4.	a	Explain the Fully associative cache organization and a mapping example	7	CO3	L2
	b	Explain prefetch buffer and internal data forwarding mechanisms used in instruction pipelining.	8	CO3	L2

CO2: Analyze the various hardware technologies using processors and memory hierarchy.
CO3: Distinguish the performance of linear & non-linear pipelining environment in a processor

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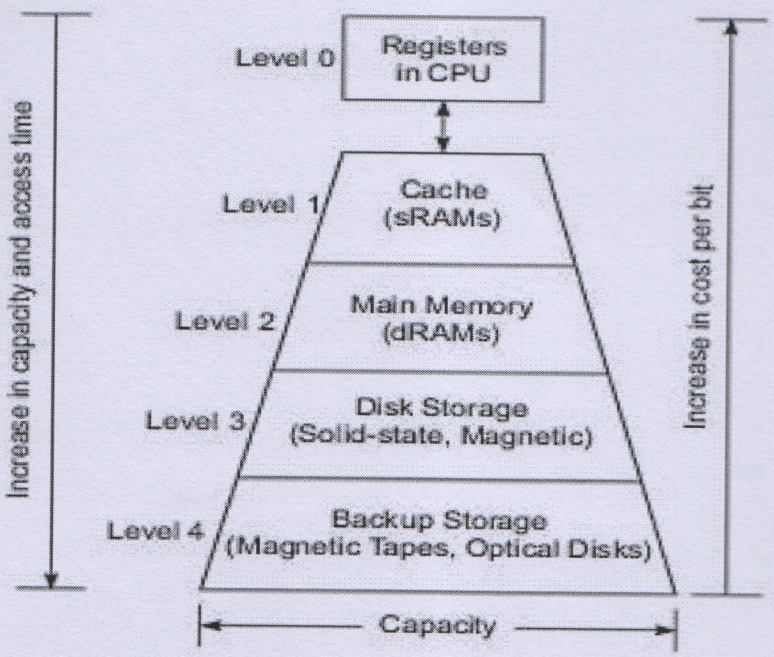
II-INTERNAL ASSESSMENT TEST

Subject: ADVANCED COMPUTER ARCHITECTURES (17CS72/15CS72) Date: 21/12/2020
Max Marks: 30 Time: 03:00 PM – 04:30 PM
Faculty: Mr. MADHUSUDHAN. S/Dr.MANJUNATH KOTARI Semester: 7

Answer any 2 full questions

Question#		Question	Marks	CO	BT/CL
		Part-A			
1.	a	With a diagram explain the hierarchical memory technology.	7	CO2	L2
		Answer:  Diagram : 3 marks Registers and Caches: 1 mark Main Memory : 1 mark Disk Drives and Backup storage: 1 mark Peripheral Technology : 1 mark			
	b	Explain typical superscalar RISC processor architecture	8	CO2	L2
		Answer:			

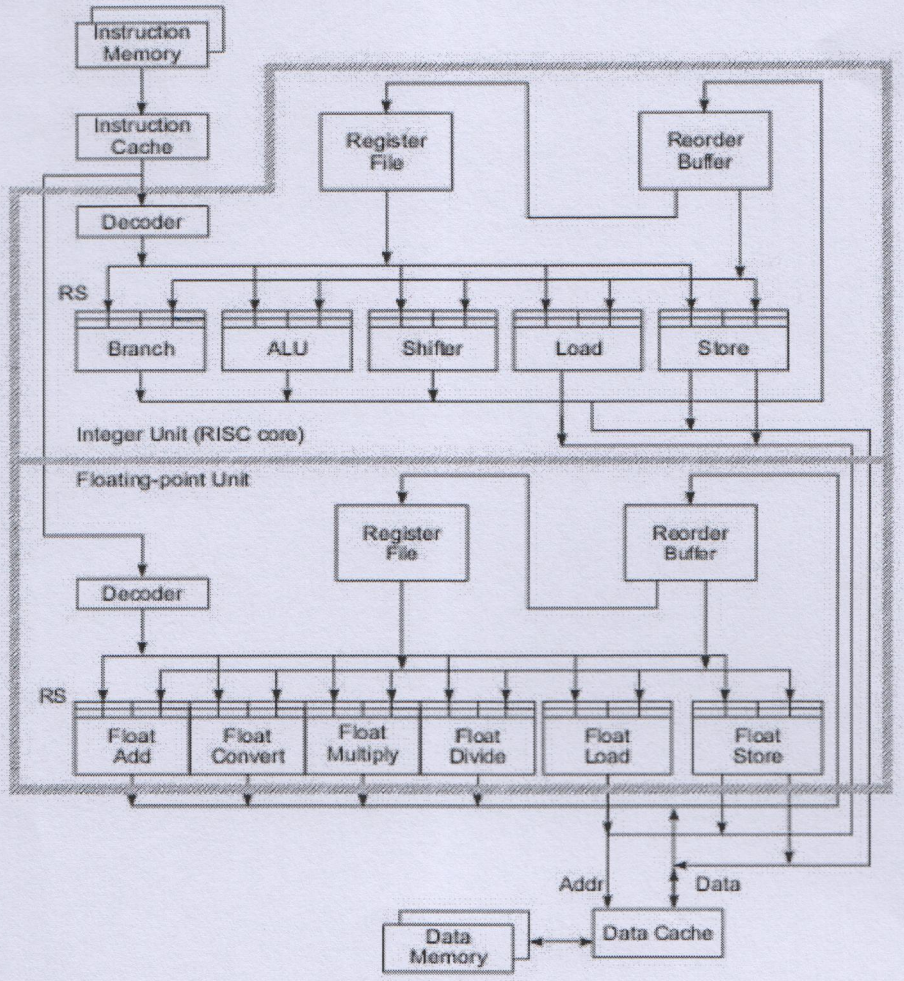


Diagram : 5 marks
Explanation : 3 marks

OR

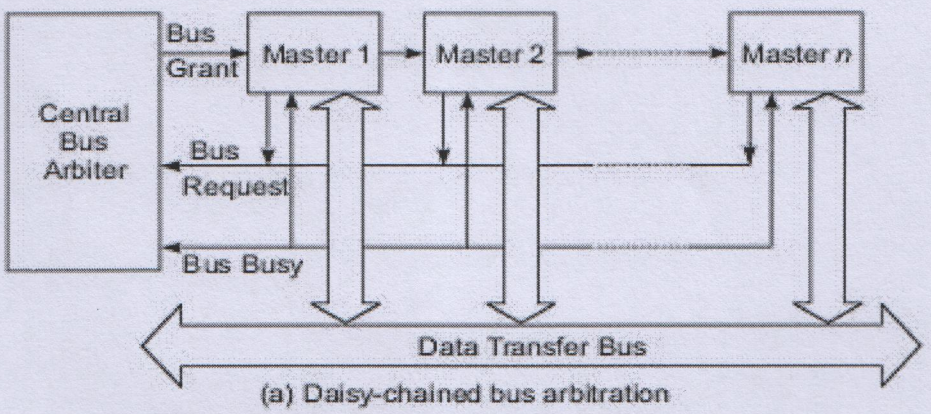
2.	a	Give the characteristics of symbolic processors	7	CO2	L2
		Answer: Knowledge Representation : 1 mark Common operation : 1 mark Memory requirements: 1 mark Communication patterns: 1 mark Properties of Algorithms : 1mark Input/output requirements: 1 mark Architecture features: 1 mark			
	b	Illustrate page replacement policies with the help of an example.	8	CO2	L3
		Answer: i) LRU : 1 mark ii) OPT : 1 mark iii) FIFO : 1 mark iv) Circular FIFO : 1 mark v) Random Replacement: 1 mark Examples: 3 marks			

	PF	0	1	2	4	2	3	7	2	1	3	1	Hit Ratio
LRU	*a*	0	0	0	4	4	4	7	7	7	3	3	
	b		1	1	1	1	3	3	3	1	1	1	$\frac{3}{11}$
	c			2	2	2	2	2	2	2	2	2	
	Faults	*	*	*	*		*	*		*	*		
OPT	*a*	0	0	0	4	4	3	7	7	7	3	3	
	b		1	1	1	1	1	1	1	1	1	1	$\frac{4}{11}$
	c			2	2	2	2	2	2	2	2	2	
	Fault	*	*	*	*		*	*			*		
FIFO	*a*	0	0	0	4	4	4	4	2	2	2	2	
	b		1	1	1	1	3	3	1	1	1	1	$\frac{2}{11}$
	c			2	2	2	2	7	7	7	3	3	
	Faults	*	*	*	*		*	*	*	*	*		

Part- B

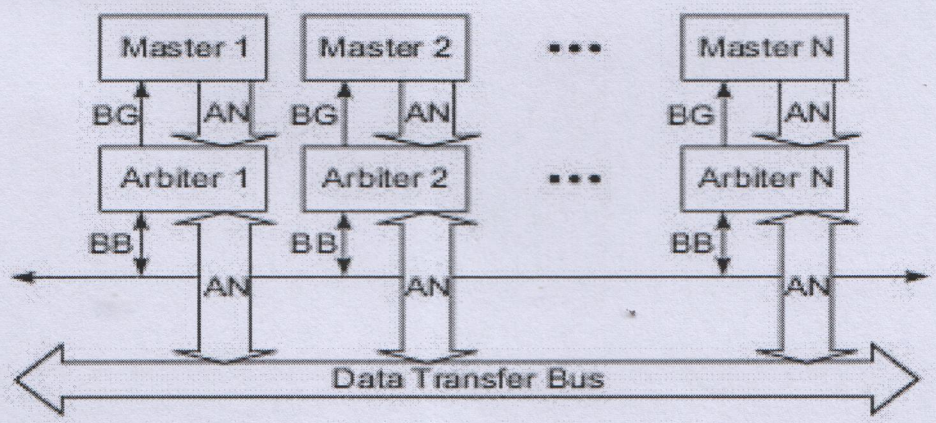
3.	a	Explain bus arbitration and its types in multiprocessor systems.	7	CO3	L2

Answer:
Definition: 1 mark
Central Arbitration: 3 marks



(a) Daisy-chained bus arbitration

Distributed Arbitration: 3 marks



	b	Consider the following pipelined processor within 3 stages this pipeline has total evaluation time of 8 clock cycles. All successor stages must be used after each clock cycle.	8	CO3	L3

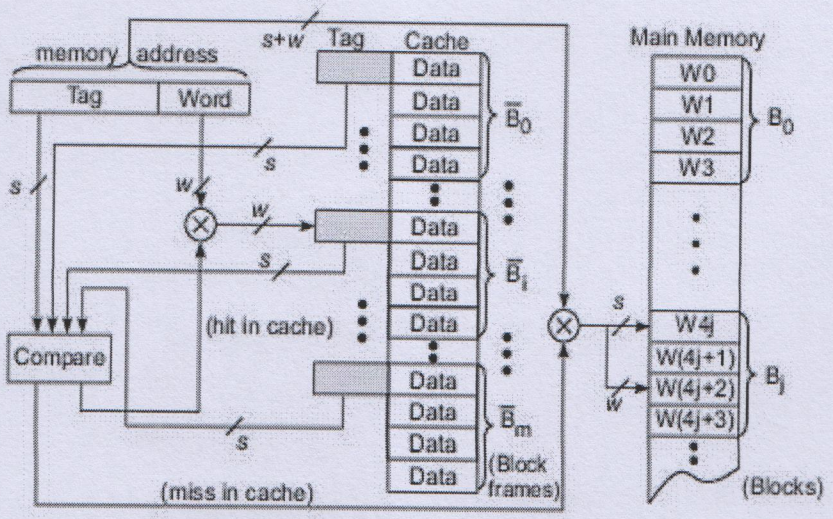
	0	1	2	3	4	5	6	7	8
S1	X								X
S2		X	X						
S3				X					
S4					X	X			
S5							X	X	

(i) List the set of forbidden latencies between task initiations.
(ii) Draw the state diagram which shows all possible latency cycles.
(iii) List all greedy cycles.
(iv) Determine the value of MAL & MCL.

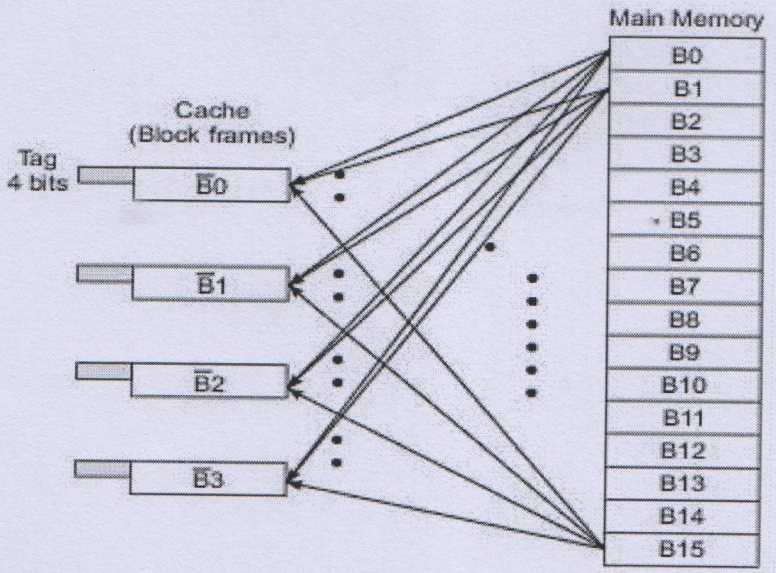
OR

4.	a	Explain the Fully associative cache organization and a mapping example	7	CO3	L2

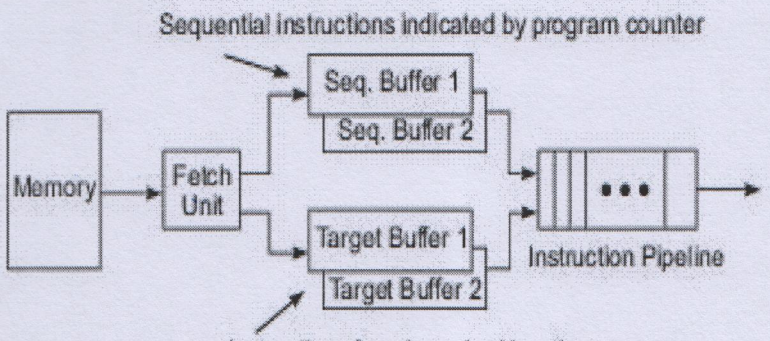
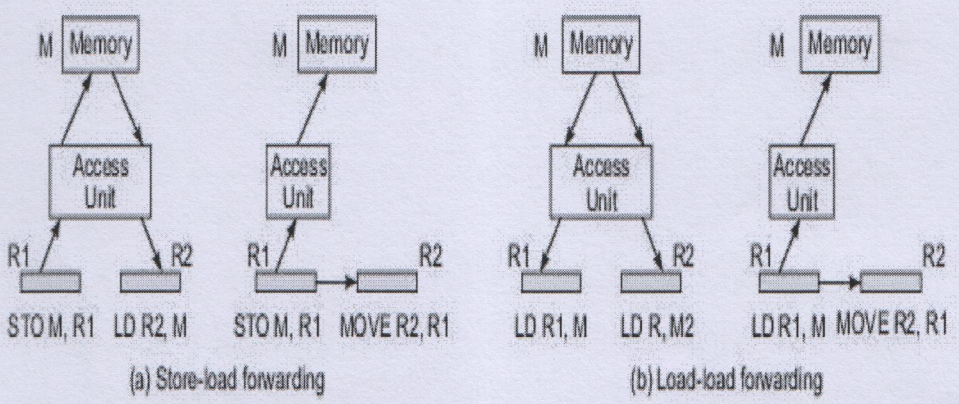
Answer:
Diagram: 5 marks



And



Explanation: 2 marks

	b	Explain prefetch buffer and internal data forwarding mechanisms used in instruction pipelining.  And  	8	CO3	L2

CO2: Analyze the various hardware technologies using processors and memory hierarchy.
CO3: Distinguish the performance of linear & non-linear pipelining environment in a processor

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III-INTERNAL ASSESSMENT TEST

Subject: ADVANCED COMPUTER ARCHITECTURES (17CS72/15CS72) Date: 13/01/202
Max Marks: 30 Time: 03:00 PM – 04:30 PM
Faculty: DR. MANJUNATH KOTHARI & Mr. MADHUSUDHAN. S Semester: 7

Note: Answer any 2 full questions selecting one FULL question from each part

Question#		Question	Marks	CO	BT/
		PART A			
1.	a	What are the different techniques for branch prediction? Explain.	7	3	L2
	b	Design a pipeline unit for fixed-point multiplication of 8-bit: integer	8	3	L3
		OR			
2.	a	Explain cache coherence problems. Describe directory based protocols to solve cache coherence problems.	7	4	L2
	b	Discuss the various Vector Access memory schemes.	8	4	L2
		PART B			
3.	a	Explain vector instruction types.	7	4	L2
	b	Briefly explain message routing schemes.	8	4	L2
		OR			
4.	a	Explain the implementation models of the SIMD Vector Computers	7	4	L3
	b	Draw the architecture of the Connection Machine CM-2.	8	4	L3

Madhusudhan S. 11/1/24 11/1/24

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CO3: **Distinguish** the performance of pipelining and non-pipelining environment in a processor

CO4: **Compare** and **contrast** the parallel and scalable architectures

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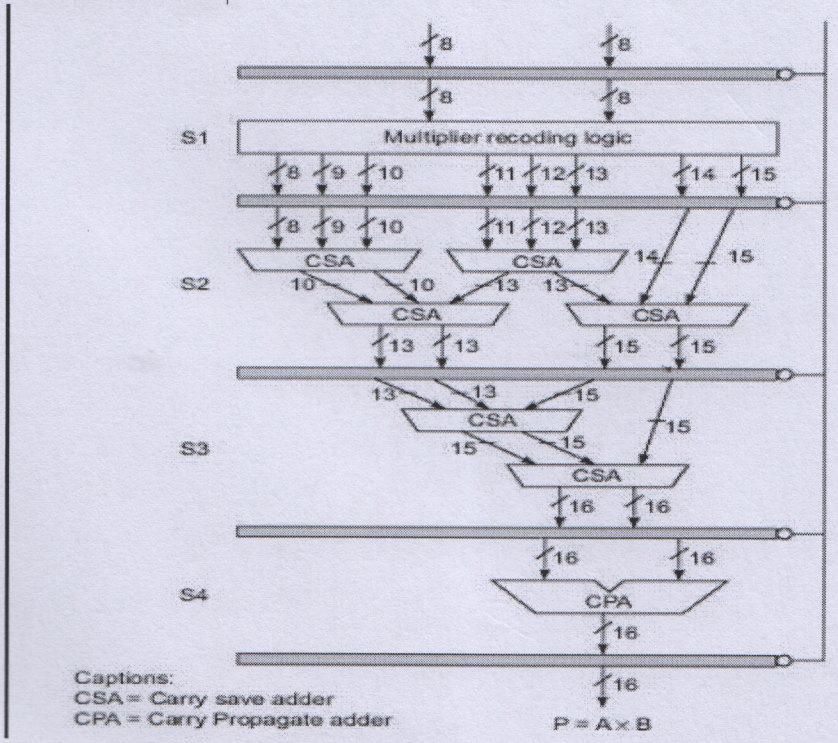
III-INTERNAL ASSESSMENT TEST

Subject: ADVANCED COMPUTER ARCHITECTURES (17CS72/15CS72) Date: 13/01/2021
Max Marks: 30 Time: 03:00 PM – 04:30 PM
Faculty: Mr. MADHUSUDHAN. S/Dr.MANJUNATH KOTARI Semester: 7

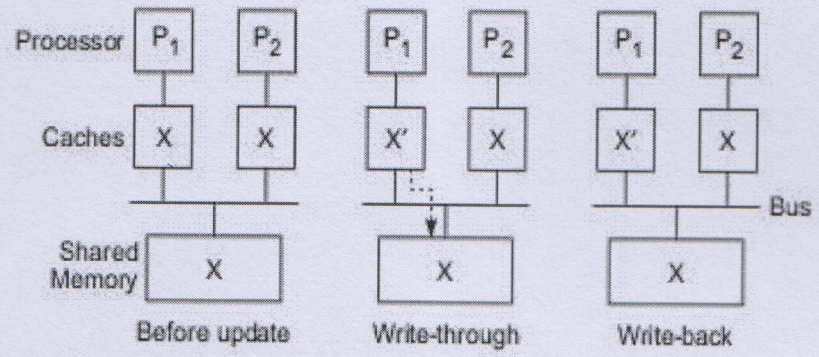
Answer any 2 full questions

Question#		Question	Marks	CO	BT/CL
		Part-A			
1.	a	What are the different techniques for branch prediction? Explain.	7	CO2	L2
		Answer: Definition : 2 marks Branch can be predicted either based on branch code types statically or based on branch history during program execution. The probability of branch with respect to a particular branch instruction type can be used to predict branch. Static branch: 2.5 mark Dynamic branch : 2.5 mark			
	b	Explain multiply pipeline design to multiply two 8-bit integers.	8	CO2	L2
		Answer: Diagram : 5 marks Explanation: 3 Marks  			
		OR			

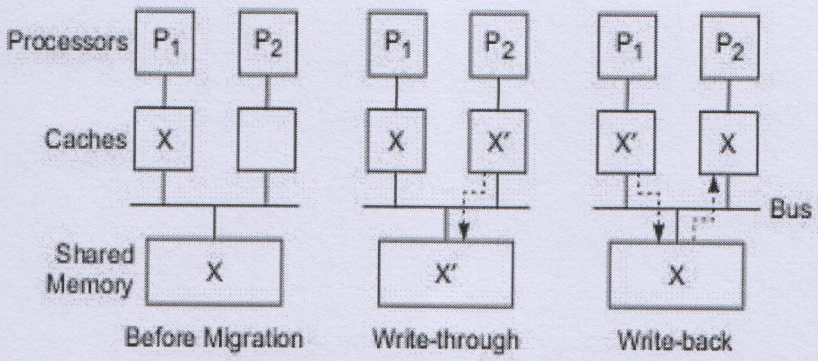
2	a	Explain cache coherence problems. Describe directory based protocols to solve cache coherence problems.	7	CO2	L2

Answer:

Cache coherence problem with explanation: 3 mark

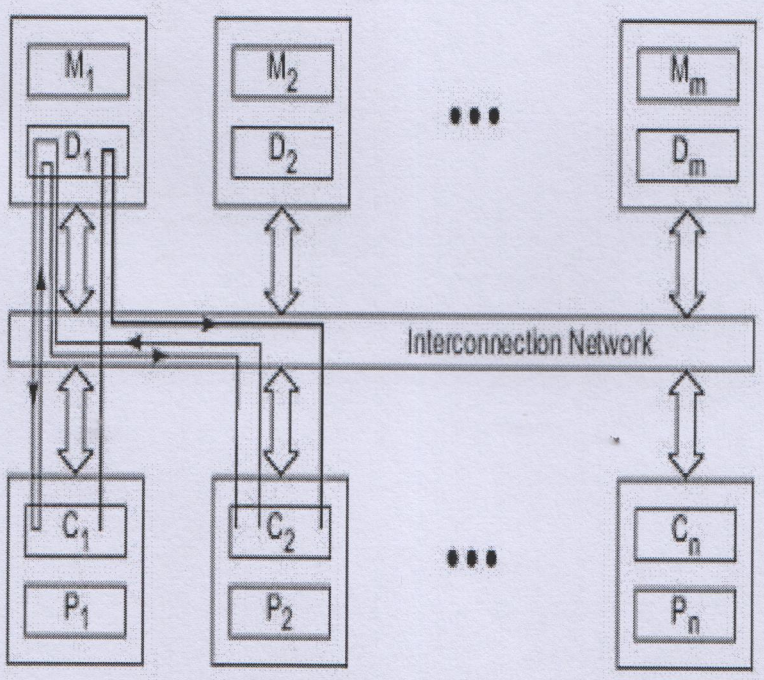


(a) Inconsistency in sharing of writable data



(b) Inconsistency after process migration

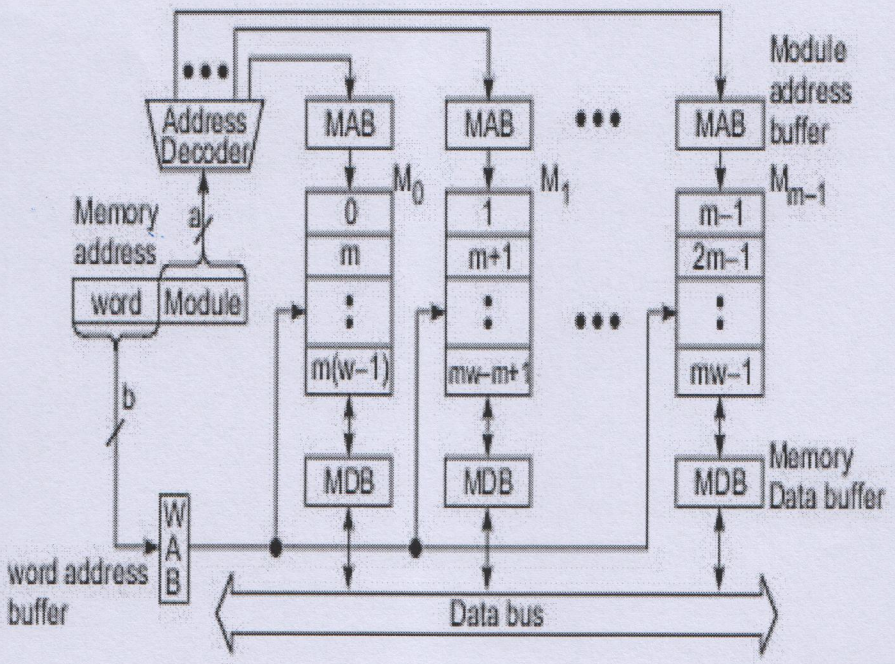
Directory based protocols with explanation : 4 mark



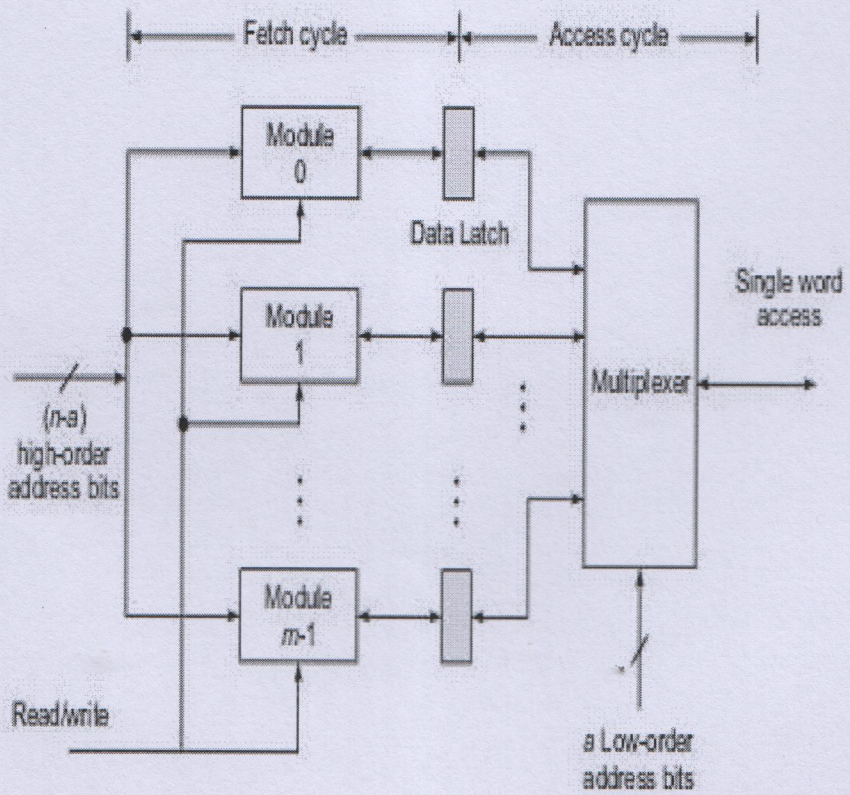
	b	Explain vector access memory schemes	8	CO2	L3

Answer:

i) C access memory scheme 4 marks

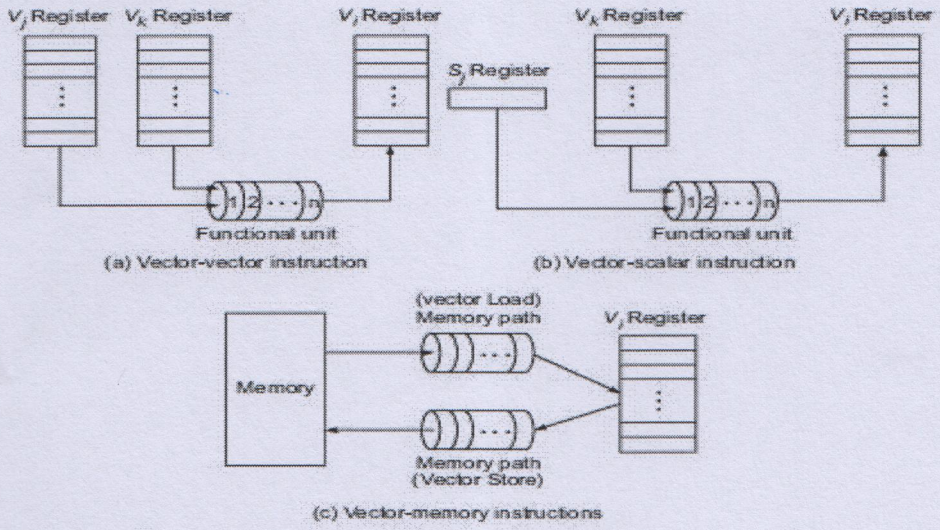
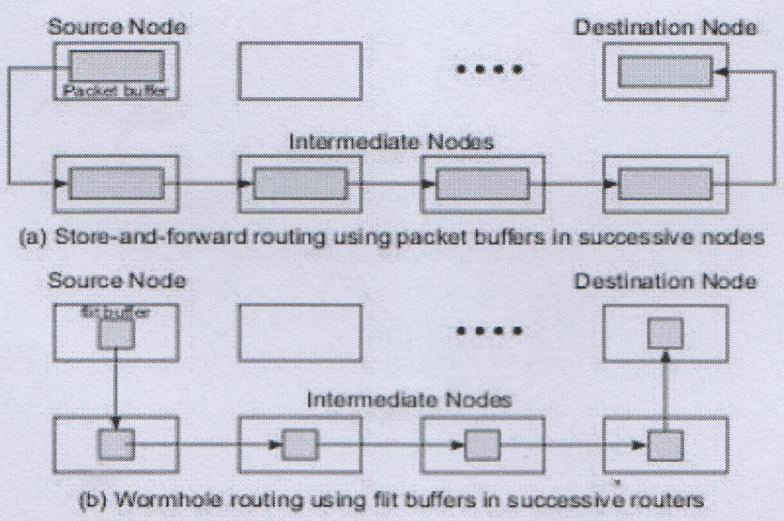


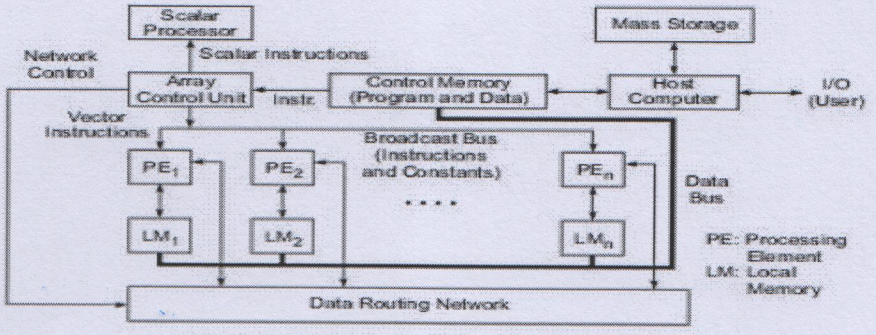
ii) S access memory access with explanation: 4marks



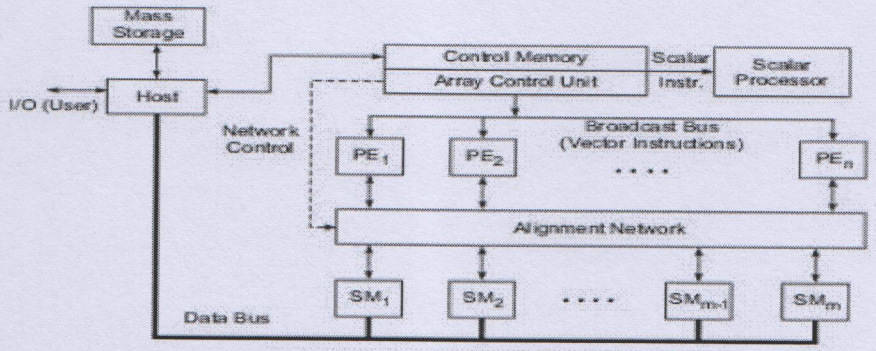
(a) S-access organization for an *m*-way interleaved memory

		Part- B			
3.	a	Explain vector instruction types.	7	CO3	L2
		Answer: Types with any three explanations : 7 marks Vector Instruction types:			

		Vector-vector instructions Vector-scalar instructions Vector-memory instructions Vector-reduction instructions Gather and Scatter instructions Masking Instructions  			
	b	Briefly explain message routing schemes.	8	CO3	L3
		Answer: store and forward : 4 marks Worm hole routing : 4 marks  **Fig. 7.27** Store-and-forward routing and wormhole routing (Courtesy of Lionel Ni, 1991) Marks			
		OR			
4.	a	What are the implementation model of the SIMD? Explain them.	7	CO3	L2
		Answer: Diagram: 5 marks			



(a) Using distributed local memories (e.g. the Illiac IV)

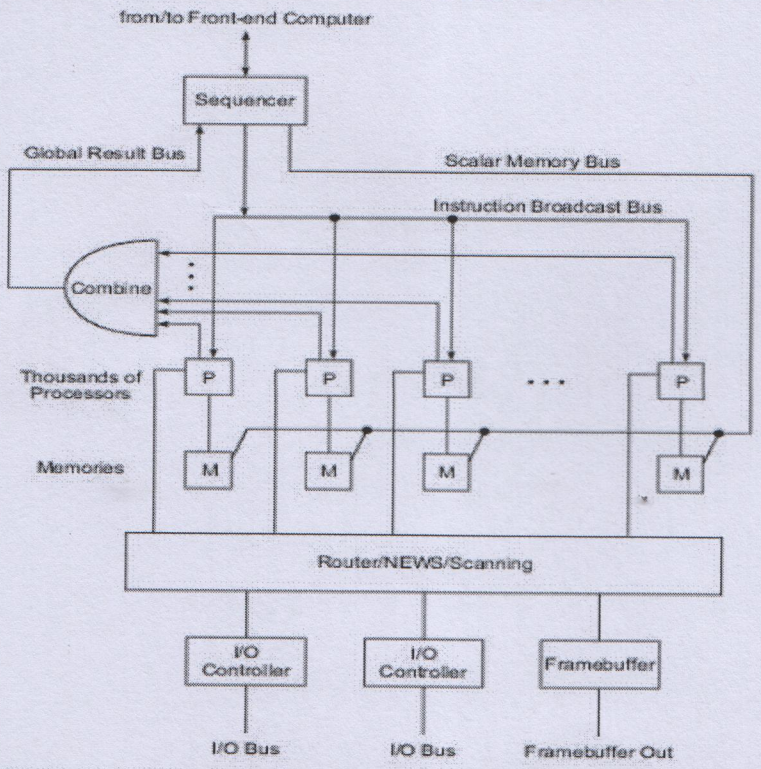


(b) Using shared-memory modules (e.g. the BSP)

Fig. 8.22 Two models for constructing SIMD supercomputers

Explanation: 2 marks

b Explain the architecture of the connection machine CM-2.



The architecture of the Connection Machine CM-2 (Courtesy of Thinking Machines Corporation, 1990)

Diagram: 6 marks explanation 2 marks

8 CO3 L2

Department of Computer Science & Engineering

Advanced Computer Architectures 17CS72/15CS72

VII Semester A & B Section

Assignment 2020-21 **Marks: 30**

Note:

1. Each group should need to solve the assigned problem & present the same in regular class on as per the schedule.
2. For the Question Number 2, you will need to use QtSPIM simulator. You can download and install using the link: https://sourceforge.net/projects/spimsimulator/files/
   a. You can install QtSPIM on either Windows or Linux systems.
   b. A tutorial for QtSPIM is available here:https://ecs-network.serv.pacific.edu/ecpe-170/tutorials/qtspim-tutorial
3. Submit all the 3 solutions in separate documentation file to Google Classroom.

Sl.No.	Question Number	Presentation Deadline
1	1	04-12-2020
2	2	11-12-2020
3	3	30-12-2020

<table>
<tr><th>Question. No</th><th>Problem Description</th><th>Group No.</th></tr>
<tr><td>1.</td><td>Consider the execution of an object code with 400,000 instructions on a 200-MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment:

<table>
<tr><th>Instruction type</th><th>CPI</th><th>Instruction mix</th></tr>
<tr><td>Arithmetic and logic</td><td>1</td><td>60%</td></tr>
<tr><td>Load/store with cache hit</td><td>2</td><td>18%</td></tr>
<tr><td>Branch</td><td>4</td><td>12%</td></tr>
<tr><td>Memory reference with cache miss</td><td>8</td><td>10%</td></tr>
</table>
a)Calculate the average CPI when the program is executed on a uniprocessor with the above trace results.

b)Calculate the corresponding MIPS rate based on the CPI obtained in part (a).</td><td rowspan="3">1</td></tr>
<tr><td>2.</td><td>Introduction to MIPS Processor Architecture using QtSpim simulator:
a) Store FFFF in $8. Left shift it 2 times and store the result in memory location 0x10000000.
b) Evaluate the expression $(2x+3)^2$ where x is the content in register $10 . Store the result in register $13.
You should check whether the results of the above exercises reflect correctly in the appropriate registers and the memory locations. Take the screenshot of the results.</td></tr>
<tr><td>3.</td><td>Consider the following reservation table for a four-stage pipeline with a clock cycle τ</td></tr>
</table>

= **20** ns.

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X			
S4				X	X	

a. What are the forbidden latency and the initial collision vector ?
b. Draw the state transition diagram for the scheduling the pipeline.
c. Determine the MAL associated with the shortest greedy cycle.
d. Determine the pipeline throughput corresponding to the MAL and given τ .
e. Determine the lower bound on the MAL for this pipeline.

1. Assume that you have the following mix of instructions with average CPIs:
The clock rate for this machine is 1 GHz.

	% of Mix	Average CPI
ALU	47%	6.7
Load	19%	7.9
Branch	20%	5.0
Store	14%	7.1

You want to improve the performance of this machine, and are considering redesigning your multiplier to reduce the average CPI of multiply instructions. If you make this change, the CPI of multiply instructions would drop to 6 (from 8). The percentage of ALU instructions that are multiply instructions is 23%. How much will performance improve by?

2. Complete the following code snippet to add 10 numbers stored consecutively in data memory. Print the result on console. 2

```
.data
array : .word 10 12 15 -10 13 82 -9 4 3 -7    #array={10,12,15,-10,13,82,-9,4,3,-7}
length: .word 10                               #load the length of the array as 10
sum: .word 0                                   #initialise sum to 0
.text
main:
la $t3, array                                  # load base address of the array
# $t3 has the base address of data. All the subsequent data can be accessed using respective offset values.
#Add your code here
```

Count the total number of machine instructions written and executed to complete this task.

3. Case Study : ARM vs ATOM Processors

1. Two compilers are being tested for a 1 GHz machine with 3 classes of instructions A, B, and C – again, requiring 1, 2, and 3 clock cycles respectively. 3

Instruction Type	Cycles per Instruction (CPI)
A	1
B	2
C	3

Compiler	# of A instructions	# of B instructions	# of C instructio
1	5 M	1 M	1 M
2	10 M	1 M	1 M

Compiler	Cycles from type A	Cycles from type B	Cycles from typ
1	($5x10^6$ inst.)(1 CC/ inst.) **$5x10^6$ CCs**	($1x10^6$ inst.)(2 CC/ inst.) **$2x10^6$ CCs**	($1x10^6$ inst.)(3 CC/ **$3x10^6$ CCs**
2	($10x10^6$ inst.)(1 CC/ inst.) **$10x10^6$ CCs**	($1x10^6$ inst.)(2 CC/ inst.) **$2x10^6$ CCs**	($1x10^6$ inst.)(3 CC/ **$3x10^6$ CCs**

Which sequence will produce more millions of instructions per clock cycle (MIPS)?

2. Introduction to MIPS Processor Architecture using QtSpim simulator:

c) Store FFFF in $8. Left shift it 2 times and store the result in memory location 0x10000000.

d) Evaluate the expression $(2x+3)^2$ where x is the content in register $10 . Store the result in register $13.

You should check whether the results of the above exercises reflect correctly in the appropriate registers and the memory locations. Take the screenshot of the results.

3. Case Study : Intel Processors – **Pentium Pro I/II/III**

1. Let's assume that we have a CPU that executes the following mix of instructions:
- 43% are ALU operations (i.e. adds, subtracts, etc.) that take 1 CC
- 21% are Load instructions (i.e. that bring data from memory to a register) that take 1 CC
- 12% are Store instructions (i.e. that write data in a register to memory) that take 2 CCs
- 24% are Jump instructions (i.e. that help to implement conditionals, etc.) that take 2 CCs

What happens if we implement 1 CC stores at the expense of a 15% slower clock?
Is this change a good idea?

2. Use lb $t1, 5($zero) to cause an exception when attempting to load a byte from address 5. What is the address of the lb instruction in your program? What is the value of the cause register, the exception code, the vaddr, and the epc when the exception occurs?

3. Consider the following reservation table for a **five-stage pipeline** with a **clock cycle** τ = **20** ns. 4

	1	2	3	4	5	6	7
S1	X						X
S2		X		X			
S3			X				
S4				X	→	X_1	
D					D_1		

a. List the forbidden & permissible latencies
b. Draw the state transition diagram for obtaining the optimal cycle.
c. List all the simple cycles and greedy cycles from the state diagram.
d. Prove that the MAL equals to the lower bound.
e. What is the optimal throughput of this pipeline ?

1. Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs: 5

Instruction Type	Instruction Count (millions)	Cycles per Instruction
Machine A		
Arithmetic and logic	8	1
Load and store	4	3
Branch	2	4
Others	4	3
Machine A		
Arithmetic and logic	10	1
Load and store	8	2
Branch	2	4
Others	4	3

Determine the effective CPI, MIPS rate, and execution time for each machine.

2. Evaluate the expression 'ab-10a+20b+16'. Consider that only $t0 and $t1 are available to store temporary values. Store a=10 and b=20 in the data section. Use stack for other memory requirements. Display the sum.

3. Consider the **five-staged pipelined** processor specified by the following reservation table:

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

a. List the set of forbidden latencies and the collision vector.
b. Draw the state transition diagram showing all possible initial sequence (cycles) without
causing a collision in the pipeline.
c. List all the simple cycles from the state diagram.
d. Identify the greedy cycles among the simple cycles.
e. What is the MAL of this pipeline ?
f. What is the minimum allowed constant cycle in using this pipeline ?
g. What will be the maximum throughput of this pipeline ?
h. What will be the throughput if the minimum constant cycle is used ?

1. **Consider two SRC programs having three types of instructions given as follows**

Instruction Type	Program 1	Program 2
Data transfer instructions	2	1
Control instructions	2	5
ALSU Instructions	2	1

6

Instruction Type	CPI
Control	2
ALSU	3
Data Transfer	4

Compare both the programs for the following parameters
1. Instruction count
2. Speed of execution

2. Introduction to MIPS Processor Architecture using QtSpim simulator:
   e) Store FFFF in $8. Left shift it 2 times and store the result in memory location 0x10000000.
   f) Evaluate the expression $(2x+3)^2$ where x is the content in register $10 . Store the result in register $13.
   You should check whether the results of the above exercises reflect correctly in the appropriate registers and the memory locations. Take the screenshot of the results.

3. Case Study : Intel Processors – **Pentium-4, M**

1. Analyze the data dependences among the following statements in a given program:
   S1: Load Rl, 1024 /Rl ← 1024/
   S2: Load R2, M(10) /R2 ← Memory(10) /
   S3: Add Rl, R2 /Rl ← (Rl) + (R2)/
   S4: Store M(1024), R1 /Memory(1024) ← (Rl)/
   S5: Store M((R2)), 1024 /Memory(64) ← 1024/
   where (Ri) means the content of register Ri and Memory(l0) contains 64 initially.
   (a) Draw a dependence graph to show all the dependences.
   (b) Are there any resource dependences if only one copy of each functional unit is available in the CPU?

2. Create a linked list of integers entered by user using the MIPS Assembly Language. Sort the list. You may take user input for the number of nodes initially. Print the numbers before and after sorting.

3. Case Study : Intel Processors – i5 vs **i7**

1. Design the 32x32 Omega Networks with required number of stages by using 2x2 switches

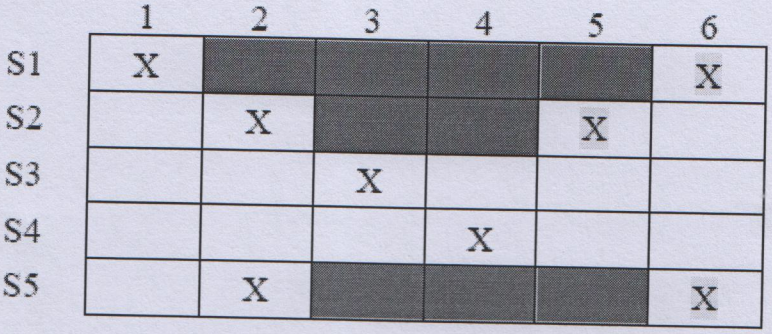
2. Complete the following code snippet to add 10 numbers stored consecutively in data memory. Print the result on console.

```
.data
array : .word 10 12 15 -10 13 82 -9 4 3 -7    #array={10,12,15,-10,13,82,-9,4,3,-7}
length: .word 10                              #load the length of the array as 10
sum: .word 0                                  #initialise sum to 0
.text
main:
la $t3, array                                 # load base address of the array
```

$t3 has the base address of data. All the subsequent data can be accessed using respective offset values.
#Add your code here
Include the following numbers in the array data segment of question (a).
10,20,30,40,50,77
Now you have 16 numbers residing in the array (data memory). Add these numbers and display the result.
Count the total number of instructions written and executed.
Compare and analyze the relation between the number of data elements and total number of machine instructions executed and written.

7

8

3.	Case Study : Intel Processors – **Core2-Duo vs i3**	
1.	Design the 32x32 Baseline Networks with required number of stages by using 2x2 switches	
2.	Create a linked list of integers entered by user using the MIPS Assembly Language. Sort the list. You may take user input for the number of nodes initially. Print the numbers before and after sorting.	
3.	Consider the **five-staged pipelined** processor specified by the following reservation table:  a. List the set of forbidden latencies and the collision vector. b. Draw the state transition diagram showing all possible initial sequence (cycles) without causing a collision in the pipeline. c. List all the simple cycles from the state diagram. d. Identify the greedy cycles among the simple cycles. e. What is the MAL of this pipeline ? f. What is the minimum allowed constant cycle in using this pipeline ? g. What will be the maximum throughput of this pipeline ? h. What will be the throughput if the minimum constant cycle is used ?	9
1.	A two-level memory system has eight virtual pages on a disk to be mapped into four page frames {PFs) in the main memory. A certain program generated the following page trace: 1,0,2,2,1,7,6,7,0,1,2,0,3,0,4,5,1,5,2,4,5,6,7,6,7,2,4,2,7,3,3,2,3 (a) Show the successive virtual pages residing in the four page frames with respect to the above page trace using the LRU replacement policy. Compute the hit ratio in the main memory. Assume the PFs are initially empty. (b) Repeat part (a) for the circular FIFO page replacement policy. Compute the hit ratio in the main memory (c) Compare the hit ratio in parts (a) and b) and comment on the effectiveness of using the circular FIFO policy to approximate the LRU policy with respect to this particular page trace.	
2.	Give the Case Study of Intel Xeon Phi	10
3.	Consider the execution of a program of **15,000 instructions** by a **linear pipeline** processor with a **clock rate of 25 Mhz**. Assume that the instruction pipeline has **five stages** and that **one instruction is issued per clock cycle**. The penalties due to branch instructions and out-of sequence executions are ignored. a. Calculate the speedup factor using this pipeline to execute the program as compared with the use of an equivalent non-pipelined processor with an equal amount of flow-through delay. b. What are the efficiency and throughput of this pipelined processor ?	

Course Teacher

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43.	4AL17CS104	SYED HUDAIF IBRAHIM	6	2	2	10	6	2	2	10	6	2	2	10	10
44.	4AL17CS108	VIHA B RAJU	6	2	2	10	6	2	2	10	6	2	2	10	10
45.	4AL17CS109	VIKAS A L	6	2	2	10	6	2	2	10	6	2	2	10	10
46.	4AL17CS112	VINOD KUMAR	6	2	2	10	6	2	2	10	6	2	2	10	10
47.	4AL17CS115	SUMAN RATHOD	6	2	2	10	6	2	2	10	6	2	2	10	10
48.	4AL17CS116	SAHANA C	6	2	2	10	6	2	2	10	6	2	2	10	10
49.	4AL17CS117	SINCHANA	6	2	2	10	6	2	2	10	6	2	2	10	10
50.	4AL17CS119	NACHIKETH S BHAT	5	2	2	10	6	2	2	10	6	2	2	10	10
51.	4AL17CS120	B SAI HARSHA	6	2	1	9	6	2	1	9	6	2	2	10	10
52.	4AL17CS122	RAVI MATH	6	2	1	9	6	2	1	9	6	2	2	10	10
53.	4AL18CS401	SANDHYA KAPSE	6	2	1	9	6	2	1	9	6	2	2	10	10

Dr-Manjunath Kini.

Faculty Name & Signature

26.	4AL17CS070	RACHANA K N	6	2	2	10	6	2	2	10	6	2	2	10	10
27.	4AL17CS071	RAGHAVI H	6	2	2	10	6	2	2	10	6	2	2	10	10
28.	4AL17CS073	RAKSHA S	6	2	2	10	6	2	2	10	6	2	2	10	10
29.	4AL17CS075	RANI M D	6	2	2	10	6	2	2	10	6	2	2	10	10
30.	4AL17CS076	RAVALI P	6	2	2	10	6	2	2	10	6	2	2	10	10
31.	4AL17CS077	ROHAN MAHAVEER	6	2	2	10	6	2	2	10	6	2	2	10	10
32.	4AL17CS080	SACHIN RAJORA	6	2	2	10	6	2	2	10	6	2	2	10	10
33.	4AL17CS081	SANA F HABIB	6	2	2	10	6	2	2	10	6	2	2	10	10
34.	4AL17CS089	SHETTY SATHVIK R	6	2	2	10	6	2	2	10	6	2	2	10	10
35.	4AL17CS090	SHILPA S U	6	2	1	10	6	2	1	10	6	2	2	10	10
36.	4AL17CS091	SHREETAL KALABANDI	6	2	2	10	6	2	2	10	6	2	2	10	10
37.	4AL17CS092	SHRINIVASA	6	2	2	10	6	2	2	10	6	2	2	10	10
38.	4AL17CS093	SHWETHA M S	6	2	2	10	6	2	2	10	6	2	2	10	10
39.	4AL17CS095	SNEHA K BAKALE	6	2	2	10	6	2	2	10	6	2	2	10	10
40.	4AL17CS097	SPOORTHI M S	6	2	2	10	6	2	2	10	6	2	2	10	10
41.	4AL17CS100	SUHAS M S	6	2	2	10	6	2	2	10	6	2	2	10	10
42.	4AL17CS101	SURYA PRAKASH S	6	2	2	10	6	2	2	10	6	2	2	10	10

9.	4AL17CS020	CHANDANA PATIL	6	2	2	10	6	2	2	9	6	2	2	10	10
10.	4AL17CS021	CHETANA H	6	2	2	10	6	2	2	9	6	2	2	10	10
11.	4AL17CS028	DHEERAJ KRISHNA D	6	2	1	10	6	2	1	9	6	2	2	10	10
12.	4AL17CS030	GAYATRI V KAMAT	6	2	1	10	6	2	1	9	6	2	2	10	10
13.	4AL17CS034	JAGATH HAREN	6	2	2	10	6	2	2	10	6	2	2	10	10
14.	4AL17CS035	JAYALAKSHMI M	6	2	2	10	6	2	2	10	6	2	2	10	10
15.	4AL17CS040	KAVANA V	6	2	2	10	6	2	2	10	6	2	2	10	10
16.	4AL17CS044	KOUSHIK S N	6	2	1	9	6	2	1	9	6	2	2	10	10
17.	4AL17CS046	LIKITHA M	6	2	1	9	6	2	1	9	6	2	2	10	10
18.	4AL17CS048	MADAN G GUDIGAR	6	2	2	10	6	2	2	9	6	2	2	10	10
19.	4AL17CS050	MHASKE POOJA S	6	2	1	9	6	2	1	9	6	2	2	10	10
20.	4AL17CS051	MAHEK SABHA	6	2	2	10	6	2	2	10	6	2	2	10	10
21.	4AL17CS052	NAGASHREE ARUN M	6	2	2	10	6	2	2	10	6	2	2	10	10
22.	4AL17CS055	NETRA SURESH G	6	2	2	10	6	2	2	10	6	2	2	10	10
23.	4AL17CS062	PRANAV L M	6	2	2	10	6	2	2	10	6	2	2	10	10
24.	4AL17CS066	PRIYA H T	6	2	2	10	6	2	2	10	6	2	2	10	10
25.	4AL17CS067	PRIYANKA KILLEDAR	6	2	2	10	6	2	2	10	6	2	2	10	10

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DEPARTMENT OF COMPUTER SCIENCE & EGINEERING

Advanced Computer Architectures 17CS72/15CS72

Assignment Marks as per Rubrics

Rubrics:

A: Presentation of Problem Solution/Subject Seminar – 6 Marks

B: Submission of Problem Solution in Book / Hand-outs – 2 Marks

C: Submission as per deadline – 2 Marks

VII A Section

Sl. No	USN	Name	Assignment 1				Assignment 2				Assignment 3				Final Marks
			A	B	C	Total	A	B	C	Total	A	B	C	Total	
1.	4AL16CS047	MADUSHREE R	6	2	1	9	6	2	1	9	6	2	2	10	10
2.	4AL17CS002	AJEYASHREE K	6	2	2	10	6	2	2	9	6	2	2	10	10
3.	4AL17CS005	AMRUTHA M	6	2	2	10	6	2	2	9	6	2	2	10	10
4.	4AL17CS007	ANUSHA	6	2	2	10	6	2	2	9	6	2	2	10	10
5.	4AL17CS010	APEKSHA RAJENDRA R	6	2	1	9	6	2	1	9	6	2	2	10	10
6.	4AL17CS012	APOORVA K N	6	2	2	10	6	2	2	9	6	2	2	10	10
7.	4AL17CS015	ASHA RUDRAPPA T	6	2	2	10	6	2	2	9	6	2	2	10	10
8.	4AL17CS019	BHRAMARI P SHETTY	6	2	2	10	6	2	2	9	6	2	2	10	10

43.	4AL17CS083	SHAH DHRUVIL A	6	2	2	10	6	2	2	10	6	2	2	10	10
44.	4AL17CS084	SHAIFA SHALA	6	2	2	10	6	2	2	10	6	2	2	10	10
45.	4AL17CS085	SHANBHAG ATISH	6	2	2	10	6	2	2	10	6	2	2	10	10
46.	4AL17CS086	SHETTY ANKIT S	6	2	2	10	6	2	2	10	6	2	2	10	10
47.	4AL17CS087	SHETTY DISHA R	6	2	2	10	6	2	2	10	6	2	2	10	10
48.	4AL17CS094	SINDHU N	6	2	2	10	6	2	2	10	6	2	2	10	10
49.	4AL17CS096	SOUNDARYA R	6	2	2	10	6	2	2	10	6	2	2	10	10
50.	4AL17CS098	SPOORTHI BALAJI	5	2	2	10	6	2	2	10	6	2	2	10	10
51.	4AL17CS099	SHRILATHA K K	6	2	1	9	6	2	1	9	6	2	2	10	10
52.	4AL17CS102	SUSHMITHA	6	2	1	9	6	2	1	9	6	2	2	10	10
53.	4AL17CS103	SUSHMITHA B P	6	2	1	9	6	2	1	9	6	2	2	10	10
54.	4AL17CS106	VARSHITHA	6	2	1	9	6	2	1	9	6	2	2	10	10
55.	4AL17CS107	VIDYA K C	6	2	1	9	6	2	1	9	6	2	2	10	10
56.	4AL17CS114	NIRIKSHA A	6	2	1	9	6	2	1	9	6	2	2	10	10
57.	4AL17CS118	JAIDITYA Y	6	2	1	9	6	2	1	9	6	2	2	10	10
58.	4AL17CS123	PRUTHVI B C	6	2	1	9	6	2	1	9	6	2	2	10	10
59.	4AL18CS400	SAGAR B V	6	2	1	9	6	2	1	9	6	2	2	10	10

Faculty Name & Signature

Radhesudhan. S

26.	4AL17CS037	JOHN ALSTEN TAURO	6	2	2	10	6	2	2	10	6	2	2	10	10
27.	4AL17CS038	K THRISHUL	6	2	2	10	6	2	2	10	6	2	2	10	10
28.	4AL17CS039	KANAKA B S	6	2	2	10	6	2	2	10	6	2	2	10	10
29.	4AL17CS041	KAVYA	6	2	2	10	6	2	2	10	6	2	2	10	10
30.	4AL17CS042	KAVYA R SHETTY	6	2	2	10	6	2	2	10	6	2	2	10	10
31.	4AL17CS045	LATHIK MOGER	6	2	2	10	6	2	2	10	6	2	2	10	10
32.	4AL17CS047	M C SUCHITHRA H	6	2	2	10	6	2	2	10	6	2	2	10	10
33.	4AL17CS053	NAIK NAYANA G	6	2	2	10	6	2	2	10	6	2	2	10	10
34.	4AL17CS054	NANDITHA R SHETTY	6	2	2	10	6	2	2	10	6	2	2	10	10
35.	4AL17CS056	PALLAVI	6	2	1	10	6	2	1	10	6	2	2	10	10
36.	4AL17CS057	PAVANA P	6	2	2	10	6	2	2	10	6	2	2	10	10
37.	4AL17CS059	PRAJNA	6	2	2	10	6	2	2	10	6	2	2	10	10
38.	4AL17CS063	PRAVEEN KUMAR S	6	2	2	10	6	2	2	10	6	2	2	10	10
39.	4AL17CS065	PREETHI	6	2	2	10	6	2	2	10	6	2	2	10	10
40.	4AL17CS074	RAMITHA Y S	6	2	2	10	6	2	2	10	6	2	2	10	10
41.	4AL17CS078	ROHAN VASHISTA	6	2	2	10	6	2	2	10	6	2	2	10	10
42.	4AL17CS079	ROUSHA	6	2	2	10	6	2	2	10	6	2	2	10	10

9.	4AL17CS004	AKSHATA N HEGDE	6	2	2	10	6	2	2	9	6	2	2	10	10
10.	4AL17CS006	ANILKUMAR B N	6	2	2	10	6	2	2	9	6	2	2	10	10
11.	4AL17CS008	ANVITHA POOJARY	6	2	1	10	6	2	1	9	6	2	2	10	10
12.	4AL17CS009	ANVITHA U	6	2	1	10	6	2	1	9	6	2	2	10	10
13.	4AL17CS011	APOORVA H P	6	2	2	10	6	2	2	10	6	2	2	10	10
14.	4AL17CS013	ARUNA K	6	2	2	10	6	2	2	10	6	2	2	10	10
15.	4AL17CS016	ASHIKA	6	2	2	10	6	2	2	10	6	2	2	10	10
16.	4AL17CS017	ASHWINI	6	2	1	9	6	2	1	9	6	2	2	10	10
17.	4AL17CS018	ASHWINI S J	6	2	1	9	6	2	1	9	6	2	2	10	10
18.	4AL17CS022	CHETHANA J	6	2	2	10	6	2	2	9	6	2	2	10	10
19.	4AL17CS024	D JASMINE JOYLINE	6	2	1	9	6	2	1	9	6	2	2	10	10
20.	4AL17CS025	DATTA KIRAN A B	6	2	2	10	6	2	2	10	6	2	2	10	10
21.	4AL17CS027	DHANYA BHAT	6	2	2	10	6	2	2	10	6	2	2	10	10
22.	4AL17CS029	DSOUZA ELSTON R	6	2	2	10	6	2	2	10	6	2	2	10	10
23.	4AL17CS031	GOWDA ROSHNI S	6	2	2	10	6	2	2	10	6	2	2	10	10
24.	4AL17CS033	HEMALATHA S	6	2	2	10	6	2	2	10	6	2	2	10	10
25.	4AL17CS036	JAYRAJ CHIRAG K	6	2	2	10	6	2	2	10	6	2	2	10	10

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DEPARTMENT OF COMPUTER SCIENCE & EGINEERING

Advanced Computer Architectures 17CS72/15CS72

Assignment Marks as per Rubrics

Rubrics:

A: Presentation of Problem Solution/Subject Seminar – 6 Marks

B: Submission of Problem Solution in Book / Hand-outs – 2 Marks

C: Submission as per deadline – 2 Marks

VII B Section

Sl. No	USN	Name	Assignment 1				Assignment 2				Assignment 3				Final
			A	B	C	Total	A	B	C	Total	A	B	C	Total	
1.	4AL14CS040	M G SHWETHA	6	2	1	9	6	2	1	9	6	2	2	10	5
2.	4AL15CS026	DARSHAN M	6	2	2	10	6	2	2	9	6	2	2	10	5
3.	4AL15CS061	NAOREM LAXMI DEVI	6	2	2	10	6	2	2	9	6	2	2	10	5
4.	4AL16CS015	ANUSHA P S	6	2	2	10	6	2	2	9	6	2	2	10	5
5.	4AL16CS063	POOJA RAJEEV	6	2	1	9	6	2	1	9	6	2	2	10	5
6.	4AL16CS113	TANOJ M	6	2	2	10	6	2	2	9	6	2	2	10	5
7.	4AL16CS078	HARSHITH S	6	2	2	10	6	2	2	9	6	2	2	10	10
8.	4AL17CS003	AKSHAT KHANDE	6	2	2	10	6	2	2	9	6	2	2	10	10

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Branch : CS Semester : 7

Sl NO.	USN	17CS72
1	4AL16CS047	32
2	4AL16CS078	25
3	4AL17CS002	35
4	4AL17CS003	35
5	4AL17CS004	30
6	4AL17CS005	36
7	4AL17CS006	25
8	4AL17CS007	34
9	4AL17CS008	30
10	4AL17CS009	32
11	4AL17CS010	33
12	4AL17CS011	28
13	4AL17CS012	40
14	4AL17CS013	28
15	4AL17CS015	29
16	4AL17CS016	31
17	4AL17CS017	32
18	4AL17CS018	33
19	4AL17CS019	35
20	4AL17CS020	29
21	4AL17CS021	32
22	4AL17CS022	33
23	4AL17CS024	40
24	4AL17CS025	28
25	4AL17CS027	29
26	4AL17CS028	35
27	4AL17CS029	30
28	4AL17CS030	28
29	4AL17CS031	31
30	4AL17CS033	23
31	4AL17CS034	40
32	4AL17CS035	31
33	4AL17CS036	31
34	4AL17CS037	26
35	4AL17CS038	28
36	4AL17CS039	30

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Sl NO.	USN	17CS72
37	4AL17CS040	32
38	4AL17CS041	27
39	4AL17CS042	24
40	4AL17CS044	30
41	4AL17CS045	22
42	4AL17CS046	34
43	4AL17CS047	33
44	4AL17CS048	27
45	4AL17CS050	36
46	4AL17CS051	36
47	4AL17CS052	40
48	4AL17CS053	31
49	4AL17CS054	32
50	4AL17CS055	35
51	4AL17CS056	27
52	4AL17CS057	29
53	4AL17CS059	25
54	4AL17CS062	38
55	4AL17CS063	21
56	4AL17CS065	28
57	4AL17CS066	30
58	4AL17CS067	40
59	4AL17CS070	29
60	4AL17CS071	31
61	4AL17CS073	33
62	4AL17CS074	30
63	4AL17CS075	26
64	4AL17CS076	34
65	4AL17CS077	40
66	4AL17CS078	26
67	4AL17CS079	28
68	4AL17CS080	25
69	4AL17CS081	31
70	4AL17CS083	36
71	4AL17CS084	29
72	4AL17CS085	36
73	4AL17CS086	31
74	4AL17CS087	26
75	4AL17CS089	33

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Sl NO.	USN	17CS72
76	4AL17CS090	28
77	4AL17CS091	35
78	4AL17CS092	26
79	4AL17CS093	33
80	4AL17CS094	26
81	4AL17CS095	40
82	4AL17CS096	21
83	4AL17CS097	28
84	4AL17CS098	27
85	4AL17CS099	29
86	4AL17CS100	29
87	4AL17CS101	36
88	4AL17CS102	28
89	4AL17CS103	29
90	4AL17CS104	39
91	4AL17CS106	31
92	4AL17CS107	33
93	4AL17CS108	40
94	4AL17CS109	40
95	4AL17CS112	21
96	4AL17CS114	29
97	4AL17CS115	37
98	4AL17CS116	35
99	4AL17CS117	40
100	4AL17CS118	28
101	4AL17CS119	33
102	4AL17CS120	31
103	4AL17CS122	22
104	4AL17CS123	21
105	4AL18CS400	21
106	4AL18CS401	31

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Branch : CS Semester : 7

Sl NO.	USN	15CS72
1	4AL14CS040	15
2	4AL15CS026	13
3	4AL15CS061	15
4	4AL16CS015	12
5	4AL16CS063	16
6	4AL16CS113	12

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DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Academic Year 2020-2021

VII SEM CSE TOPPERS LIST

4AL17CS067	PRIYANKA KILLEDAR
4AL17CS024	D JASMINE JOYLINE
4AL17CS052	NAGASHREE ARUN M
4AL17CS034	JAGATH HAREN
4AL17CS007	ANUSHA
4AL17CS053	NAIK NAYANA GANAPATI
4AL17CS017	ASHWINI
4AL17CS109	VIKAS A L

Dept. Of Computer Science & Engineering
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

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Alva's Institute of Engineering & Technology

Shobhavana Campus, Mijar, Moodbidri, D.K – 574225

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Academic Year 2020-2021

VII SEM CSE POOR PERFORMERS LIST

4AL14CS040	**M G SHWETHA**
4AL15CS061	**NAOREM LUXMI DEVI**
4AL16CS047	**MADHUSHREE R**
4AL16CS015	**ANUSHA P S**
4AL16CS063	**POOJA RAJEEV**
4AL16CS113	**TANOJ M**
4AL16CS078	S HARSHITH
4AL17CS045	LATHIK MOGER
4AL17CS063	PRAVEEN KUMAR S
4AL17CS066	PRIYA H T
4AL17CS120	B SAI HARSHA
4AL17CS123	PRUTHVI B C
4AL18CS401	SANDHYA KAPSE
4AL14CS040	M G SHWETHA
4AL15CS061	NAOREM LUXMI DEVI
4AL16CS047	MADHUSHREE R
4AL16CS015	ANUSHA P S
4AL16CS063	POOJA RAJEEV
4AL16CS113	TANOJ M
4AL16CS078	S HARSHITH
4AL17CS045	LATHIK MOGER
4AL17CS063	PRAVEEN KUMAR S
4AL17CS066	PRIYA H T
4AL17CS120	B SAI HARSHA
4AL17CS123	PRUTHVI B C
4AL18CS401	SANDHYA KAPSE

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Modified

CBCS SCHEME

USN | | | | | | | | | | |

17CS72

Seventh Semester B.E. Degree Examination, Jan./Feb.2021
Advanced Computer Architectures

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. With the help of block diagrams, explain Flynn's classification of computer architectures. **(10 Marks)**

b. Describe the shared-memory multiprocessor models. **(10 Marks)**

OR

2 a. Define the types of data dependence. Also compute the dependence graph for the following code segment:

S_1 : Load R1, A

S_2 : Add R2, R1

S_3 : Move R1, R3

S_4 : Store B, R1 **(10 Marks)**

b. Explain the characteristics of the following static connection networks :
(i) Linear array. (ii) Ring. (iii) Binary tree. (iv) Mesh. **(10 Marks)**

Module-2

3 a. Distinguish between RISC and CISC processor architectures, with block diagrams. **(10 Marks)**

b. Explain VLIW processor architecture and its pipeline operations. **(10 Marks)**

OR

4 a. Compare the two virtual memory models for multiprocessor systems. **(10 Marks)**

b. Illustrate four level memory hierarchy. **(04 Marks)**

c. Define the various page replacement policies. **(06 Marks)**

Module-3

5 a. Illustrate daisy-chained and distributed arbitration techniques. **(10 Marks)**

b. List the various Cache mapping schemes. Also explain any two schemes. **(10 Marks)**

OR

6 a. Consider the following pipeline reservation table:

Time →

Stages	1	2	3	4	5	6	7
S_1	X						X
S_2		X		X			
S_3			X		X		

(i) What are the forbidden latencies?
(ii) What is the initial collision vector?
(iii) Draw the state transition diagram
(iv) List all the simple cycles.
(v) List all the greedy cycles.
(vi) Determine the minimal average Latency. **(10 Marks)**

b. Explain the usage of prefetch buffers in instruction pipelining. **(06 Marks)**

c. Illustrate internal data forwarding technique. **(04 Marks)**

Module-4

7 a. Define the two approaches of snoopy bus cache coherence protocol. Also write the state transition graphs for write through and write back cache. **(10 Marks)**

b. Explain in detail, three types of cache directory protocols. **(10 Marks)**

OR

8 a. Explain the flow control methods for resolving a collision between two packets requesting the same outgoing channel. **(10 Marks)**

b. Distinguish between store-and-forward routing and wormhole routing schemes. **(04 Marks)**

c. Define the various vector instruction types. **(06 Marks)**

Module-5

9 a. Explain the mechanisms used for interprocess communication. **(06 Marks)**

b. Describe the compilation phases in parallel code generation. **(08 Marks)**

c. Explain the sole-access protocols used in synchronization. **(06 Marks)**

OR

10 a. Explain the concept of recorder buffer as a processor element. **(06 Marks)**

b. With the help of a block diagram, explain the role of reservation stations used in Tomasulo's algorithm. **(08 Marks)**

c. Write and explain state transition diagram of 2 bit branch predictor. **(06 Marks)**

* * * * *

17CS72

Re: Sir, regarding Modification of Scheme and solutions

"Ravishankar K C" <kcrshankar@gmail.com>

February 16, 2021 1:44 PM

To: boe@vtu.ac.in

Sir
Schemes of 17CS72 and 17IS72 have been verified and approved.
This is for your kind reference and needful
Regards
Dr K C Ravishankar
Chairman BOE CS AND IS

Dr K C Ravishankar
Principal GEC Hassan

> On 16-Feb-2021, at 11:41 AM, boe@vtu.ac.in wrote:

<17CS72.pdf>
<17IS72.pdf>

"APPROVED"
Registrar (Evaluation)
Visvesvaraya Technological University
BELAGAVI - 590018

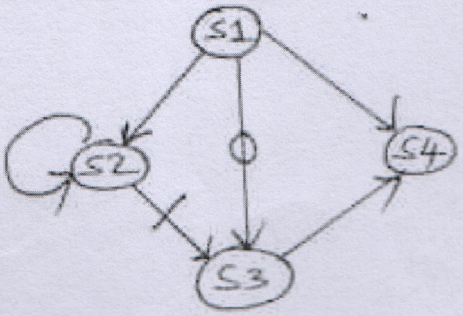
201117CS7224421

Visvesvaraya Technological University
Belagavi, Karnataka – 590 018.

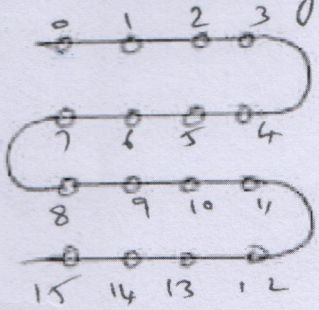
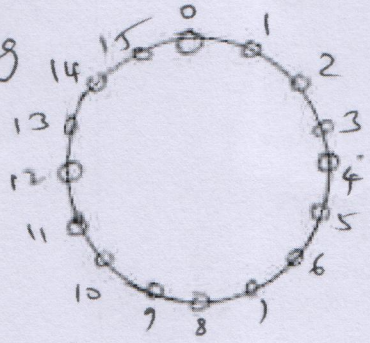
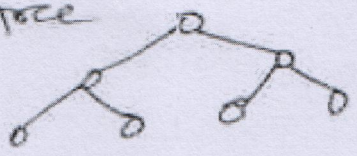
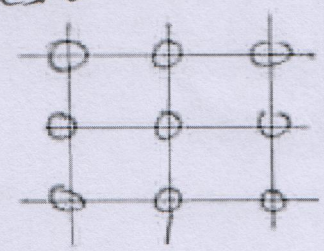
Scheme & Solutions

Signature of Scrutinizer

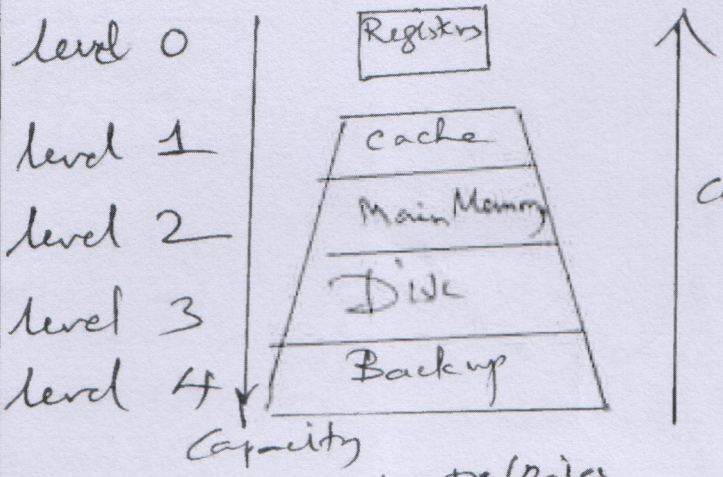
Subject Title : Advanced Computer Architecture Subject Code : 17CS72

Question Number	Solution	Marks Allocated
1. a)	Module-1: Flynn's classification SISD - Single instruction single data stream SIMD - Single instruction multiple data stream MIMD - Multiple instruction, multiple data stream MISD - Multiple instruction single data stream Block diagrams and explanation — 2.5 marks each	10
b)	Shared-memory models UMA — 3 marks NUMA — 4 marks COMA — 3 marks } Block diagram and explanation	10
2. a)	5 types of data dependences — 1 mark each flow dependence antidependence output dependence I/O dependence Unknown dependence dependence graph — 5 marks  	10

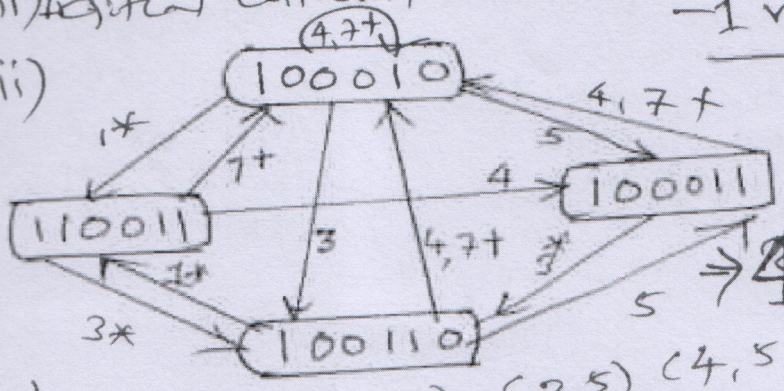
Subject Title : Advanced Computer Architectures Subject Code : 17CS72

Question Number	Solution	Marks Allocated
2 b)	Linear array  1-D network N-1 Links degree 2 b = 1 – 2.5 marks	10
	ring  uni directional or bi directional degree 2 $d = \lfloor N/2 \rfloor$ or N – 2.5 marks	
	binary tree  $N = 2^k - 1$ nodes (k level) max d = 3 (degree) diameter 2(k-1) Scalable – 2.5 marks	
	mesh  n^k nodes degree – 2k diameter k(n-1) – 2.5 marks	
	Module-2	
3. a)	RISC and CISC block diagram – 6 marks Explanation – 4 marks	10
b)	VLIW processor block diagram – 6 marks explanation – 4 marks	10

Subject Title : Advanced Computer Architecture Subject Code : 17CS72

Question Number	Solution	Marks Allocated
4. a)	Virtual memory models: - private virtual memory - 5 marks - Globally shared virtual memory - 5 marks	10
b)	four level Hierarchy in memory  	04
c)	Page replacement policies LRU, OPT, FIFO, LFU circular FIFO and Random replacement - 1 mark each	06
	Module-3	
5. a)	Daisy chained central arbitration - 5 marks distributed arbitration - 5 marks	10
b)	Cache mapping schemes direct fully associative Set associative & sector mapping - 2 marks Explanation to any two of the above schemes - 4 marks each.	10

Subject Title : Advanced Computer Architectures Subject Code : 17C572

Question Number	Solution	Marks Allocated
6. a)	i) forbidden latencies S1: 7-1 = 6 S2: 4-2 = 2 S3: 5-3 = 2 — 1 mark	10
	ii) Initial collision vector: 100010 — 1 mark	
	iii)  — 4 marks	
	iv) (4), (1,7), (1,3), (3,5), (4,5), (3,4), (5,7) Simple cycles — 1 mark	
	v) (1,7), (1,3), (3,5), greedy cycles — 1 mark	
	vi) MAL = (1+3)/2 = 2 — 2 marks	
b)	Explanation of prefetch buffers - Sequential buffer - target buffer - loop buffer — 2 marks each	06
* 6 c)	Module - 4	
7. a)	Write-invalidate policy - 2 marks Write-update policy - 2 marks State transition graphs Write through cache - 2 marks Write back cache 4 marks	10
b)	full map directory - 4 marks eviction - 3 marks; chained 3 marks	10
* 6 c)	Internal data forwarding i) store-load ii) load-load 2 marks each	04

Subject Title: Advanced Computer Architecture Subject Code: 17CS72

Question Number	Solution	Marks Allocated
8. a)	Flow control methods: 2.5 marks each Buffering Blocking discard & retransmission Detour after being blocked	10
b)	store-and-forward routing – 2 marks wormhole routing – 2 marks	04
c)	vector instruction types. 1 mark each vector–vector, vector reduction vector–scalar, Gather & Scatter vector–memory, Masking.	06
9. a)	Module – 5 IPC Shared variable – 3 marks message passing – 3 marks	06 08
b)	Compilation phases Flow analysis, program optimizations, Parallel code generation Super scalar scheduling/shared memory multiprocessor Distributed multicomputer	06
c)	Sole access protocols: 2 marks each Lock synchronization optimistic synchronization & server synchronization	06
10. a)	Reorder buffer entries – 2 marks diagram explanation – 4 marks	08
b)	Tomasulo's algorithm block diagram – 4 marks Explanation to reservation stations Register renaming concept – 4 marks	
c)	2 bit branch predictor State transition diagram – 3 marks explanation – 3 marks	06

"APPROVED"

Registrar (Evaluation)
Visvesvaraya Technological University
BELAGAVI - 590018

Question Bank

Advanced Computer Architectures (17CS72/15CS72)

Module-I

1. Briefly explain the generations of computers
2. Explain the elements of modern computers
3. Describe the Flynn;s classification with diagram
4. List the performance factors and system attributes. Explain how performance factors are influenced by system attributes
5. Problems related to Average CPI, MIPS and Execution time
6. Explain the different shared memory Multiprocessos
7. Explain the architecture of vector super computer with neat diagram.
8. Write a note on PRAM and VLSI Models
9. What are the conditions of parallelism? Explain the types of data dependence.
10. Illustrate the data dependence in programs with example
11. How to detect parallelism in a program using Bernsteins Conditions? Explain
12. Mismatch between software and hardware parallelism
13. Comparison of Flow mechanisms
14. Program graph before and after grain packing with diagram
15. List and explain static interconnection networks
16. Draw Baseline and Omega Networks
17. What is DoP? Explain Average Parallelism in Divide and Conquer algorithms
18. Explain Efficiency, Utilization , Quality and Amdahl's law with example
19. Scalability analysis and approaches

Module-II

1. What are the characteristic of CISC and RISC architecture? Explain
2. What are the virtual memory models for multiprocessor system?
3. Explain address translation mechanism using TLB and page table.
4. Explain typical superscalar RISC processor architecture with giagram
5. Explain inclusion, coherence and locality properties.
6. Explain the concept of register windows in the SPARC architecture with diagram
7. Describe VLIW architectures with diagram
8. Explain the four level memory hierarchy with parameters access rate and cost
9. Explain the page replacement policies and corresponding example
10. Explain the memory characteristics of a typical mainframe computers
11. Explain symbolic processors with diagram

Module-III

1. With diagram explain the Backplane bus specifications
2. What is arbitration? Explain different types of arbitration.

3. Explain the different cache addressing models
4. Explain sequential and weak consistency models.
5. With example diagram explain the direct mapping cache organization
6. What Set associative cache design? Explain with diagram
7. List the cache performance issues
8. Explain shared memory organizations with diagram
9. Explain the Asynchronous and Synchronous models of pipeline units
10. Define Speedup, Efficiency and Throughput
11. Problems related to Non-linear pipeline processors
12. Explain the mechanisms for Instruction pipelining
13. What are the different techniques for branch prediction? Explain.
14. Explain multiply pipeline design to multiply two 8-bit integers.

Module-IV

1. Explain the schematic design of a row of crosspoint switches in a crossbar network
2. Discuss the blocking and non-blocking effects of omega network with example
3. What is cache coherence problem? Explain cache coherence problems in data sharing and process migration
4. Explain two approaches of Snoopy bus protocols
5. Describe snoopy bus protocols with state diagrams
6. How to resolve cache coherence problems using directory based protocols? Explain with diagrams
7. Explain Message Routing schemes
8. List and explain the vector instruction types
9. Describe the Vector Memory Access Schemes
10. Compare the features of Cray Y-MP, C-90 and MPP
11. Draw the architecture model of Cray Y-MP system
12. Write a note on Compound Vector Operations
13. Explain the architecture of CM-2
14. Explain the latency hiding techniques
15. Define context switching policies
16. Explain MIT J machine architecture with schematic block diagram
17. Compare 3 types of dataflow machines
18. Draw the dataflow graph for the calculation of cos x

Module-V

1. Explain the shared variable models in parallel models
2. Describe the different language features for parallelism
3. Explain the Compilation phases in parallel code optimization with diagram
4. Explain Lexicographic order for sequential execution of successive iterations in loop structure
5. Write a Testing algorithm for dependence tests

6. Explain Vectorization and Parallelization methods
7. Construct a DAG for inner loop kernel of bubble sort program
8. Explain the following principles of Synchronization
    a. Atomic operations
    b. Wait protocols
    c. Fairness policies
    d. Sole access protocols
9. Explain the different modes of Multiprocessor Execution
10. Illustrate the model of typical processor
11. Explain the concept of operand forwarding
12. Write note on Reorder buffer and Register Renaming
13. Explain Tomasulo's Algorithm

Course Teacher

H. O. D.

Dept. Of Computer Science & Engineering
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

CBCS SCHEME

USN | | | | | | | | | | |

17CS72

Seventh Semester B.E. Degree Examination, Jan./Feb.2021
Advanced Computer Architectures

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. With the help of block diagrams, explain Flynn's classification of computer architectures. **(10 Marks)**

b. Describe the shared-memory multiprocessor models. **(10 Marks)**

OR

2 a. Define the types of data dependence. Also compute the dependence graph for the following code segment:

S_1 : Load R1, A
S_2 : Add R2, R1
S_3 : Move R1, R3
S_4 : Store B, R1 **(10 Marks)**

b. Explain the characteristics of the following static connection networks :
(i) Linear array. (ii) Ring. (iii) Binary tree. (iv) Mesh. **(10 Marks)**

Module-2

3 a. Distinguish between RISC and CISC processor architectures, with block diagrams. **(10 Marks)**

b. Explain VLIW processor architecture and its pipeline operations. **(10 Marks)**

OR

4 a. Compare the two virtual memory models for multiprocessor systems. **(10 Marks)**

b. Illustrate four level memory hierarchy. **(04 Marks)**

c. Define the various page replacement policies. **(06 Marks)**

Module-3

5 a. Illustrate daisy-chained and distributed arbitration techniques. **(10 Marks)**

b. List the various Cache mapping schemes. Also explain any two schemes. **(10 Marks)**

OR

6 a. Consider the following pipeline reservation table:

Time →

Stages	1	2	3	4	5	6	7
S_1	X						X
S_2		X		X			
S_3			X		X		

(i) What are the forbidden latencies?
(ii) What is the initial collision vector?
(iii) Draw the state transition diagram
(iv) List all the simple cycles.
(v) List all the greedy cycles.
(vi) Determine the minimal average Latency. **(10 Marks)**

b. Explain the usage of prefetch buffers in instruction pipelining. **(06 Marks)**

c. Illustrate internal data forwarding technique. **(04 Marks)**

Module-4

7 a. Define the two approaches of snoopy bus cache coherence protocol. Also write the state transition graphs for write through and write back cache. (10 Marks)

b. Explain in detail, three types of cache directory protocols. (10 Marks)

OR

8 a. Explain the flow control methods for resolving a collision between two packets requesting the same outgoing channel. (10 Marks)

b. Distinguish between store-and-forward routing and wormhole routing schemes. (04 Marks)

c. Define the various vector instruction types. (06 Marks)

Module-5

9 a. Explain the mechanisms used for interprocess communication. (06 Marks)

b. Describe the compilation phases in parallel code generation. (08 Marks)

c. Explain the sole-access protocols used in synchronization. (06 Marks)

OR

10 a. Explain the concept of recorder buffer as a processor element. (06 Marks)

b. With the help of a block diagram, explain the role of reservation stations used in Tomasulo's algorithm. (08 Marks)

c. Write and explain state transition diagram of 2 bit branch predictor. (06 Marks)

* * * * *

VTU-10-02-2021 01:04:45pm AL - AL - AL - AL - AL - AL - AL
AL - AL - AL - AL - AL - AL 10-02-2021 01:28:25pm AL - AL - AL - AL - AL - AL - AL

CBCS SCHEME

USN | | | | | | | | | | | **15CS72**

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
Advanced Computer Architecture

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. List the performance factors and system attributes. Explain how performance factors are influenced by system attributes. **(08 Marks)**
b. Explain the architecture of vector super computer with neat diagram. **(08 Marks)**

OR

2 a. What are the conditions of parallelism? Explain the types of data dependence. **(06 Marks)**
b. What are the metrics affecting scalability of a computer system? **(06 Marks)**
c. What are the important characteristics of parallel algorithms? **(04 Marks)**

Module-2

3 a. What are the characteristic of CISC and RISC architecture? **(04 Marks)**
b. What are the virtual memory models for multiprocessor system? **(04 Marks)**
c. Explain address translation mechanism using TLB and page table. **(08 Marks)**

OR

4 a. Explain typical superscalar RISC processor architecture. **(08 Marks)**
b. Explain inclusion, coherence and locality properties. **(08 Marks)**

Module-3

5 a. What is arbitration? Explain different types of arbitration. **(08 Marks)**
b. Explain sequential and weak consistency models. **(08 Marks)**

OR

6 a. What are the different techniques for branch prediction? Explain. **(08 Marks)**
b. Explain multiply pipeline design to multiply two 8-bit integers. **(08 Marks)**

Module-4

7 a. Explain routing in omega network. **(08 Marks)**
b. What are different vector – access memory schemes? Explain any two of them. **(08 Marks)**

OR

8 a. What are the implementation models of SIMD? Explain them. **(08 Marks)**
b. Explain four context-switching policies. **(08 Marks)**

Module-5

9 a. What are the issues in using shared-variable model? **(08 Marks)**
b. Explain different phases of parallelizing compiler with a diagram. **(08 Marks)**

OR

10 a. Explain testing algorithm for dependence testing. **(08 Marks)**
b. What are the principles of synchronization mechanisms? Explain them. **(08 Marks)**

* * * * *

VTU-26-12-2018 08:22:41am - TG - TG - TG - TG - TG
26-12-2018 08:46:42am - TG - TG - TG - TG - TG

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY
(A Unit of Alva's Education Foundation)
Shobhavana Campus, Mijar-574225, Moodbidri, D.K
Phone: 08258-262725, Fax: 08258-262726
Affiliated to VTU Belagavi and Approved by AICTE, New Delhi, Recognized by Govt. of Karnataka

ATTENDANCE BOOK

Academic Year : 2020 – 21

Semester : 7th Section B.

Period of the Semester : From 1st Sep, 2020 to 16th Jan, 2021

Subject with Code : ADVANCED COMPUTER ARCHITECTURES (17CS72)

Name of the Faculty : Dr ADHUSUDHAN. S.

Department : CSE

VISION OF THE INSTITUTE
"Transformative education by pursuing excellence in Engineering and Management through enhancing skills to meet the evolving needs of the community"

MISSION OF THE INSTITUTE
• To bestow quality technical education to imbibe knowledge, creativity and ethos to students community. • To inculcate the best engineering practices through transformative education. • To develop a knowledgeable individual for a dynamic industrial scenario. • To inculcate research, entrepreneurial skills and human values in order to cater the needs of the society.

AIET	Lesson Plan & Execution	Format No.	ACD 08
		Issue No.	01
		Rev. No.	00

Name of the faculty	Mr ADHUSUDHAN. S.
Semester and Section	7th Sem B-Sec.
Date of Commencement	1st Sept, 2020
Last Working Day of the Semester	16th Jan, 2021
Source Materials List	
1.	Advanced Computer Architectures Kai Hwang, Naresh Jotwani
2.	Computer Architecture: A quantitative approach. John L. Hennessy & D.A. Patterson
3.	
4.	
5.	
Subject Name	

Period	Plan			Execution		
	Date	Topics to be covered	Source Material needed	Topics Covered	Date	Source Material Referred
1	1/9	Theory of parallelism: parallel Computer models	1	Theory of parallelism: parallel Computer models.	1/9/20	1
2	5/9	The State of Computing	1	The State of Computing	5/9/20	1
3	7/9	Multiprocessors and Multicomputer	1	Multiprocessors and Multicomputer	7/9	1
4	10/9	Multivector and SIMD Computers PRAM and VLSI Models	1	Multivector and SIMD Computers	10/9	1

Period	Plan			Execution		
	Date	Topics to be covered	Source Material needed	Topics Covered	Date	Source Material Referred
5	12/9	Program and N/W properties Conditions of Parallelism	1	PRAM & VLSI Models	12/9	1
6	14/9	Program partitioning and Scheduling	1	Program and Network properties	14/9	1
7	17/9	Program flow mechanisms S/m interconnect architectures	1	Conditions of parallelism	17/9	1
8	19/9	Principles of Scalable Performance Performance metrics and measures	1	Program partitioning and Scheduling	19/9	1
9	21/9	Parallel Processing applications speed up performance laws.	1	Program flow mechanisms	21/9	1
10	24/9	Scalability analysis and approaches.	1	System Interconnect architectures	24/9	1
11	26/9	module-2 Advanced Processor Technology	1	Principles of Scalable Performance	26/9	1
12	28/9	Advanced Processor Technology	1	Performance metrics and measures	28/9	1
13	1/10	Superscalar and vector processors	1	Parallel Processing Applications	1/10	1
14	3/10	Superscalar and vector processors	1	Speed-up Performance laws.	3/10	1
15	5/10	Superscalar and vector processors	1	Scalability analysis and approaches	5/10	1
16	8/10	Memory Hierarchy Technologies	1	module-2 Advanced Processor Technology	8/10	1
17	10/10	Memory Hierarchy Technologies	1	Advanced Processor Technology	10/10	1

Period	Plan			Execution		
	Date	Topics to be covered	Source Material needed	Topics Covered	Date	Source Material Referred
18	12/10	Memory Hierarchy Technology	1	Advanced processor technology	12/10	1
19	15/10	Virtual memory Technology	1	Superscalar and vector processors	15/10	1
20	17/10	Virtual memory technology.	1	Superscalar and vector processors	17/10	1
21	19/10	Module-3. Bus Systems	1	Superscalar and vector processors	19/10	1
22	22/10	Cache memory organization	1	Memory Hierarchy Technology	22/10	1
23	24/10	Shared memory organization	1	Memory Hierarchy Technology	24/10	1
24	29/10	Sequential and weak Consistency models.	1	Memory Hierarchy Technology	29/10	1
25	2/11	Sequential and Weak Consistency models	1	Virtual memory technology	2/11	1
26	5/11	pipelining and Superscalar techniques	1	Virtual memory technology.	5/11	1
27	7/11	Linear pipeline processors	1	Module-3 Bus Systems	7/11	1
28	9/11	Non linear pipeline processors	1	Bus Systems	9/11	1
29	12/11	Instruction pipeline Design	1	Cache memory organizations	12/11	1
30	20/11	Arithmetic pipeline Design.	1	Cache memory organizations	20/11	1

Period	Plan			Execution		
	Date	Topics to be covered	Source Material needed	Topics Covered	Date	Source Material Referred
18	12/10	Memory Hierarchy Technology	1	Advanced processor technology	12/10	1
19	15/10	Virtual memory Technology	1	Superscalar and vector processors	15/10	1
20	17/10	Virtual memory technology.	1	Superscalar and vector processors	17/10	1
21	19/10	Module-3. Bus systems	1	Superscalar and vector processors	19/10	1
22	22/10	Cache memory organization	1	Memory Hierarchy Technology	22/10	1
23	24/10	Shared memory organizations	1	Memory Hierarchy Technology	24/10	1
24	29/10	Sequential and weak Consistency models.	1	Memory Hierarchy Technology	29/10	1
25	2/11	Sequential and Weak Consistency models	1	Virtual memory Technology	2/11	1
26	5/11	pipelining and Superscalar techniques	1	Virtual memory technology.	5/11	1
27	7/11	Linear pipeline processors	1	Module-3 Bus Systems	7/11	1
28	9/11	Non linear pipeline processors	1	Bus Systems	9/11	1
29	12/11	Instruction pipeline Design	1	Cache memory organizations	12/11	1
30	20/11	Arithmetic pipeline Design.	1	Cache memory organizations	20/11	1

Period	Plan			Execution		
	Date	Topics to be covered	Source Material needed	Topics Covered	Date	Source Material Referred
31	21/11	Module-4. Multiprocessor System Interconnects	1	Shared memory Organizations	21/11	1
32	23/11	Cache Coherence and Synchroni Zation Mechanisms	1	Shared memory organizations	23/11	1
33	25/11	Three generations of Multicomputers Message passing Mechanisms.	1	Sequential and weak Consistency models	25/11	1
34	26/11	Vector processing principles	1	Linear pipeline processors	26/11	1
35	27/11	Multivector Multiprocessors Compound vector processing	1	Linear pipeline processors	27/11	1
36	28/11	SIMD Computer organization	1	Non Linear pipeline processors	28/11	1
37	30/11	Latency Hiding techniques principles of Multithreading	1	Instruction pipeline Design	30/11	1
38	2/12	fine-grain Multicomputers	1	Arithmetic pipeline Design	2/12	1
39	3/12	Scalable and Multithreaded architectures	1	Arithmetic pipeline Design.	3/12	1
40	4/12	Data flow & Hybrid architectures.	1	module-4 Multiprocessor System Interconnects	4/12	1
41	5/12	Module-5 parallel programming models parallel languages & compilers	1	Cache Coherence & Synchronization Mechanisms.	5/12	1
42	7/12	Dependence analysis of data arrays Parallel programming environments	1	Three generations of Multicomputers	7/12	1
43	9/12	Synchronization and Multiprocessing models	1	Message passing Mechanisms.	9/12	1

Period	Plan			Execution		
	Date	Topics to be covered	Source Material needed	Topics Covered	Date	Source Material Referred
44	10/12	Shared Variable pgm Structures Computer architecture basic design issue	1	Vector Processing principles	10/12	1
45	11/12	problem definition model of a typical Processor	1	Multivector Multiprocessors	11/12	1
46	12/12	Compiler detected Instruction level parallelism.	1	Compound Vector Processing	12/12	1
47	14/12	Operand forwarding reorder buffer Register renaming	1	SIMD Computer Organizations	14/12	1
48	16/12	Tomasulo's Alg Branch prediction	1	Latency-Hiding Techniques	16/12	1
49	17/12	Limitations in exploiting instruction level parallelism	1	Principles of Multithreading	17/12	1
50	18/12	Thread level parallelism.	1	Fine-grain Multicomputers	18/12	1
51			1	Scalable & Multithreaded architectures.	19/12	1
52			1	Data flow & Hybrid architectures.	26/12	1
53			1	Module-5. parallel programming models.	28/12	1
54			1	Parallel languages & Compilers.	30/12	1
55			1	Dependence analysis of data arrays.	31/12	1
56			1	parallel programming environments	1/1/2021	1

Others	Planned	Actual	Remarks :
Special Classes	0	17	
Tutorials			
Assignments			
Seminars			
IA Tests			
Portions Covered in the entire Semester	100 %		

Course Effectiveness

Students Feedback	Very good		
Students Responce	Very good.		
Result	No. of Students AP	No. of Students Passed	% of Result
	59	59	100%

Faculty in Charge

Signature of Principal (& Remarks if any)

PRINCIPAL
Alva's Institute of Engg. & Technology,
Mijar, MOODBIDRI - 574 225, D.K.

HOD's Signature

Dept. Of Computer Science & Engineering
Alva's Institute of Engineering & Technology
Mijar, MOODBIDRI - 574 225

ALVA'S INSTITUTE OF ENGINEERING AND TECHNOLOGY

MIJAR, MOODBIDRI - 574 225

ATTENDANCE CUM INTERNAL

Class : 7th CSE B

Subject : Advanced Computer Architecture

No. of Classes held : 66

Sl. No.	U.S.N. 4 AI	Name	1/9	5/9	7/9	10/9	12/9	14/9	17/9	19/9	21/9	24/9	26/9	28/9	1/10	3/10	5/10
		Date / Month	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	14CS040	M. G. Shwetha	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
2	15CS026	Darshan M	1	2	3	4	5	6	7	7	8	9	10	10	11	12	13
3	15CS061	Naorem Lapmi Devi	1	2	3	3	4	4	4	5	6	7	8	9	10	11	12
4	16CS015	Anusha. P.S.	1	2	3	3	4	5	5	6	7	8	9	9	10	11	12
5	16CS063	Pooja Rajeev	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
6	16CS113	Tanoj. M	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
7	16CS078	Harshith. S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
8	17CS003	Akshat Khandelwal	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
9	17CS004	Akshata Narayana Hyt	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
10	CS006	Anil Kumar B.N	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
11	008	Anistha Poojary	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
12	009	Anistha U	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
13	011	Apoorva H. P.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
14	013	Aruna. K.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
15	016	Ashika	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16	017	Ashwini	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
17	018	Ashwini Shekarappa Jakkanalli	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
18	022	Chethana J	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
19	024	B. Jasmine Joyline	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
20	025	Datla kiran A B	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
21	027	Dhanya Bhat	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
22	029	Divya Elston Ronald	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
23	031	Gowda Roshni Shiva Prakash	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
24	033	Hemalatha. S.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
25	036	Jayraj Chiraj Kumarsrah.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
26	037	John Alston Tauro.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
27	038	K. Thrishul	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
28	039	Kanaka. B.S.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
29	041	Kavya	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
30	042	Kavya R. Shetty.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Staff Initials																	

19/10	12/10	15/10	17/10	19/10	22/10	24/10	29/10	31/10	5/11	7/11	9/11	12/11	14/11
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30

Students Attendence

Conducted		No. of Class Attended	% of Attendance	Internal Assessment (30)			Average Marks
48	60			I	II	III	
		63	95%	14	6	.	10
		62	93%	11	3	5	8
		61	92%	7	13	.	10
		60	90%	15	4	8	7
		63	95%	9	.	12	11
		64	96%	9	5	5	7
		63	95%	16	14	15	15
		64	96%	26	18	27	25
		63	95%	22	17	19	20
		66	100%	20	14	09	15
		61	92%	22	14	23	20
		63	95%	25	25	25	25
		64	96%	28	09	17	18
		64	96%	18	19	15	18
		63	95%	22	18	23	21
		63	95%	22	19	23	22
		64	96%	23	23	21	23
		64	96%	30	14	25	23
		65	98%	30	30	30	30
		65	98%	23	15	16	18
		63	95%	21	20	16	19
		62	93%	23	16	20	20
		63	95%	26	16	20	21
		63	95%	12	15	12	13
		62	93%	23	16	23	21
		61	92%	21	12	15	16
		62	93%	23	08	23	18
		62	93%	19	14	25	20
		60	90%	18	15	17	17
		61	92%	15	11	16	14

ALVA'S INSTITUTE OF ENGINEERING AND TECHNOLOGY

MIJAR, MOODBIDRI - 574 225

ATTENDANCE CUM INTERNAL

Class : 7th CSE B

Subject : Advanced Computer Architecture

No. of Classes held : 66

Sl. No.	U.S.N.	Name	1/9	5/9	7/9	10/9	12/9	14/9	17/9	19/9	21/9	23/9	25/9	28/9	1/10	3/10	5/10	8/10	10/10	12/10	15/10	17/10	19/10	22/10	24/10	29/10	2/11	5/11	7/11	9/11	12/11	29/11
		Date / Month	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
1	17CS045	Lathik Dlogu	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
2	047	MC Suchithra Hegde	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
3	053	Naik Nayana Ganapati	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
4	054	Nandita R. Shetty	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
5	056	Pallavi	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
6	057	Pavana P.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
7	059	Prajna	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
8	062	Praveen Kumar S.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
9	065	Preethi	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
10	074	Ramitha. Y.S.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
11	078	Rohan Vashista B M	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
12	079	Rousha	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
13	083	Shet Dhruvil Amit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
14	084	Shaifa Shala	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
15	085	Shanbhag Atish Manoj	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
16	086	Shetty Ankit Suresh	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
17	087	Shetty Disha Ravindra	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
18	094	Sindhu N	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
19	096	Soundarya R.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
20	098	Spoorthi Balaji	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
21	099	Shrilatha K Kamath	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
22	102	Sushmitha	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
23	103	Sushmitha B. Poojary	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
24	106	Varshitha	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
25	107	Vidya K.C.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
26	114	Nirikesha A	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
27	118	Jaidithya. Y.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
28	123	Pruthvi B.C.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
29	400	Sagar B.V.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
30																																
	Staff Initials																															

Subject :

Students attendence

Conducted		No. of Class Attended	% of Attendance	Internal Assessment (30)			Average Marks
48	60			I	II	III	
		63	95%	19	10	07	12
		64	96%	28	18	21	23
		63	95%	30	30	30	30
		61	92%	27	14	23	22
		62	93%	19	16	16	17
		61	92%	19	15	21	19
		63	95%	20	12	13	15
		64	96%	6	15	12	11
		62	93%	23	15	16	18
		62	93%	23	15	22	20
		63	95%	17	13	17	16
		63	95%	16	12	24	18
		64	96%	30	23	25	26
		64	96%	16	14	26	19
		64	96%	30	23	24	26
		65	98%	26	14	25	21
		66	100%	15	15	17	16
		63	95%	17	15	15	16
		62	93%	15	08	10	11
		63	95%	14	12	23	17
		63	95%	15	16	25	19
		64	96%	16	19	19	18
		64	96%	19	21	16	19
		64	98%	29	21	18	21
		65	98%	23	23	23	23
		64	96%	21	14	20	19
		65	98%	21	15	18	18
		63	95%	12	6	15	11
		62	93%	14	9	10	11

AIET	INTERNAL EXAM RESULT ANALYSIS	Format No.	ACD 12
		Issue No.	01
		Rev. No.	00

Department	CSE	Semester	7th
		Subject Code	17CS72
Total No. of Students	59	Academic Year	2020-21

Test	Date	Number of Students				Signature		Remarks
		Attended	0-14	15-20	21-25	Faculty	HOD	
T_1	26/11/20	59	10	19	29			
T_2	21/12/20	58	26	24	8			
T_3	13/01/21	56	11	21	24			
T_4								
T_5								

Signature of Staff in - charge

HOD's Signature

PROGRAM OUTCOMES (POs)	
PO1	**Engineering knowledge:** Apply the knowledge of mathematics, science, Engineering fundamentals and an engineering specialization to the solution of complex engineering problems.
PO2	**Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences.
PO3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal and environmental considerations.
PO4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6	**The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	**Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	**Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	**Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	**Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSOs)	
PSO1	Professional skills. After the graduating Student will be able to:
PSO2	Problem solving skills
PSO3	Successful Career and Entrepreneurship.
PSO4	

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)	
PEO1	Exhibit fundamental strength in core cases of Comp. Engg to solve the problems of computing world.
PEO2	Adapt and contribute the emerging technological changes
PEO3	Get employed in computing profession or engaged in learning to pursue higher studies.
PEO4	