

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

Computer Science and Engineering

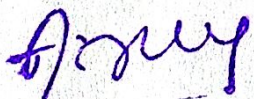
Course Name : ANALOG AND DIGITAL ELECTRONICS (17CS32)

Class : Semester 3 A

**Shilpa,
Assistant Professor,
2018-19**

1. Faculty Details

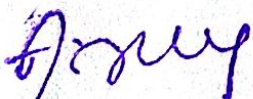
Name	:	Ms Shilpa
Qualification	:	M.Tech, BE
Department	:	CS
Permanent Address	:	D/O Hav Y Gowda Bilgunda(Vill), Shankaranahally (P), Hassan, 573128, India
Phone Number	:	9008873670
Email ID	:	shilpa@aiet.org.in
Specimen Signature	:	



HOD

2. Course Allotted

Allotted Duty	Course Title	Course Code
Theory 1	ANALOG AND DIGITAL ELECTRONICS	17CS32
Lab 1	ANALOG AND DIGITAL ELECTRONICS LABORATORY	17CSL37



HOD



ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

(A Unit of Alva's Education Foundation)

Shobhavana Campus, Mijar-574225, Moodbidri, D.K

Phone: 08258-262725, Fax: 08258-262726

Affiliated to VTU Belagavi and Approved by AICTE, New Delhi, Recognized by Govt. of Karnataka

CALENDAR OF EVENTS (ODD SEMESTER – 2018-19) BE & MBA

VISION OF THE INSTITUTE

"Transformative education by pursuing excellence in Engineering and Management through enhancing skills to meet the evolving needs of the community"

MISSION OF THE INSTITUTE

- To bestow quality technical education to imbibe knowledge, creativity and ethos to students community.
- To inculcate the best engineering practices through transformative education.
- To develop a knowledgeable individual for a dynamic industrial scenario.
- To inculcate research, entrepreneurial skills and human values in order to cater the needs of society.

Week	Month	Days							Activities
		Mon	Tue	Wed	Thu	Fri	Sat	Sun	
1	AUG			1	2	3	4	5	1 st : Commencement of III, V - Semester BE & III Semester MBA 6 th : Commencement of VII - Semester BE 8 th : Inauguration Program for I-Semester BE 9 th to 30 th : Induction Program for I-Sem BE 15 th : Independence day 22 nd : Bakrid
2		6	7	8	9	10	11	12	
3		13	14	15	16	17	18	19	
4		20	21	22	23	24	25	26	
5		27	28	29	30	31			
5	SEP						1	2	6 th , 7 th , 8 th : I-IA Test for III, V - Semester BE & III Semester MBA 13 th : Varasiddhi Vinayaka Vrata 17 th , 18 th , 19 th : I-IA Test for VII-Sem BE 21 st : Last day of Muharram
6		3	4	5	6	7	8	9	
7		10	11	12	13	14	15	16	
8		17	18	19	20	21	22	23	
9		24	25	26	27	28	29	30	
10	OCT	1	2	3	4	5	6	7	2 nd : Gandhi Jayanthi , 8 th : Mahalaya Amavasye 11 th , 12 th , 13 th : I-IA Test for I - Semester BE 15 th , 16 th , 17 th : II-IA Test for III, V - Semester BE & III Semester MBA 18 th : Ayudhapooja, 19 th : Vijayadashami 25 th , 26 th , 27 th : II-IA Test for VII - Sem BE 24 th : Maharshi Valmiki Jayanthi
11		8	9	10	11	12	13	14	
12		15	16	17	18	19	20	21	
13		22	23	24	25	26	27	28	
14		29	30	31					
14	NOV				1	2	3	4	1 st : Kannada Rajyothsava , 6 th : Naraka Chaturdashi 8 th : Deepavali, 21 st : Id-e-Milad 26 th : Kanakadasa Jayanthi 26 th , 27 th , 28 th : II-IA Test for I - Sem BE / III-IA Test for III, V - Sem BE & III Sem MBA 30 th : Last Working Day of III, V-Semester BE & III Semester MBA
15		5	6	7	8	9	10	11	
16		12	13	14	15	16	17	18	
17		19	20	21	22	23	24	25	
18		26	27	28	29	30			
18	DEC						1	2	1 st , 3 rd , 4 th : III-IA Test for VII - Semester BE 4 th : Last Working Day of VII - Semester BE 25 th : Christmas 27 th , 28 th , 29 th : III-IA Test for I - Sem BE 31 st : Onwards Crash course for I- Sem BE
19		3	4	5	6	7	8	9	
20		10	11	12	13	14	15	16	
21		17	18	19	20	21	22	23	
22		24	25	26	27	28	29	30	
23		31							
23	JAN		1	2	3	4	5	6	15 th : Makar Sankranti 17 th : Last Working Day of I-Semester BE
24		7	8	9	10	11	12	13	
25		14	15	16	17				

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

ACADEMIC CALENDAR (2018-19)-ODD

Sl. No.	Departmental Activities	Dates
1.	Pre-placement Training to Final Years	10-07-2018 to 30-07-2018
2.	Certification Course "Apple iOS App Development" by Callibre Code Pvt. Ltd., Bangalore - Third Years	10-07-2018 to 03-08-2018
3.	Workshop on Web Development - 2 nd Years	30-07-2018 to 03-08-2018
4.	Submission of Project Synopsis Final Year	31-07-2018
5.	Certification Course "Machine Learning using Python Programming" by Dlite Software, Bangalore	27-08-2018 to 01-09-2018
6.	Commencement of Classes	01-08-2018
7.	External Screening of Project Synopsis	14-09-2018
8.	Certification Course "Data Science and Big Data Analytics by ICT Academy (Dell EMC), Bangalore	03-09-2018 to 08-09-2018
9.	Forum Inauguration	25/08/2018
10.	Technical Talk - 1	25/08/2018
11.	Last date to Submit the Internship Report	28 th Sep 2018
12.	Technical Talk - 2	03/09/2018
13.	Technical Talk - 3	22/09/2018
14.	IA-Test-I	17 th , 18 th & 19 th Sep 2018
15.	Technical Talk - 4	09/10/2018
16.	Internship Viva	5 th Oct 2018
17.	Technical Talk - 5	13/10/2018
18.	Project Phase - I Evaluation	29 th Oct 2018
19.	Kaliyona Computer - Rural Computer Education Camp	2 nd & 3 rd Nov 2018
20.	IA-Test-II	25 th to 27 th Oct 2018
21.	Technical Talk - 6	13/11/2018
22.	IA-Test-III	26 th to 28 th Nov 2018
23.	Internship on "Deep Learning"	15-01-2019 to 29-01-2019
24.	Last Working Day	04-12-2018
25.	FDP on "Data Science, Machine Learning & Deep Learning"	15 th to 29 th Jan 2019
26.	Workshop for Students "Mobile Application Development"	16 th to 23 rd Jan 2019


HOD, CSE
 Dept. Of Computer Science & Engineering
 Alva's Institute of Engg. & Technology
 Mijar, MOODBIDRI - 574 225

CC to: Principal Table

All Faculty -CSE



ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY
Shobhavana Campus, Mijar, Moodbidri, D.K - 574225
Phone: 08258-262725, Fax: 08258-262726

Time Table with effect from 01/09/2018

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Academic Year		Scheme		Semester		Section		Room No		Class Coordinator	
2018-19		2017		III		A		101		Ms. SHILPA	
Time Day	9.00 To 9.55	9.55 To 10.50	10.50 To 11.10	11.10 To 12.05	12.05 To 1.00	1.00 To 2.00	2.00 To 3.00	3.00 To 4.00	4.00 To 5.00		
MON	DSA	USP	B R E A K	CO	EM-III	L U N C H	← ADE LAB A1/ DSA LAB A2→				
TUE	DSA	CO		DMS	USP		C++	ADE	APT		
WED	ADE	DMS		EM-III	CO		← ADE LAB A2/ DSA LAB A1→				
THU	DMS	DSA		APT	ADE		EM-III	USP	C++		
FRI	ADE	EM-III		USP	CPH		ADE	DSA	DMS		
SAT	EM-III	DMS		DSA	CO						
Allocation of Subjects											
Subjects						Staffs			Staff Code		
17MAT31	EM-III	Engg. Mathematics- III				Mrs. Kavitha B			KB		
17CS32	ADE	Analog & Digital Electronics				Ms. Shilpa			SH		
17CS33	DSA	Data Structure & Application				Mr. Tahir N H B			TNHB		
17CS34	CO	Computer Organization				Ms. Ankitha Shetty			AS		
17CS35	USP	Unix Shell Programming				Mr. Chanchal Antony			CA		
17CS36	DMS	Discrete Mathematical Structure				Mrs. Mangala Kini			MK		
17CSL37	ADE Lab	Analog & Digital Electronics Lab				Ms. Shilpa			SH		
						Mr. Vasudeva Shahapur			VS		
17CSL38	DSA Lab	Data Structure & Application Lab				Mr. Tahir N H B			TNHB		
						Mr. Venkatesh			VKT		
17CPH39	CPH	Constitution of India, Professional Ethnics & Human Rights				Mr. Ajith Kumar			AK		
INDUSTRY ORIENTED COURSES (IOC)											
APT		Aptitude				Mr. Vasudev Shahapur Ms. Reena Lobo			VS RL		
C++		Object Oriented Prog. With C++				Mr. Hemanth KUMAR N P			HNP		

Time Table Coordinator
31/8/18

Head of the Department
H.O.D.

Dept. Of Computer Science & Engineering
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

Principal
PRINCIPAL

Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225, D.K.



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Individual Faculty Time Table with effect from 01/09/2018 DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Academic Year		2018-19	Faculty Name			Ms.Shilpa (SH)			
Semester		ODD	Designation			Assistant Professor			
Time To Day	9.00 To 9.55	9.55 To 10.50	10.50 To 11.10	11.10 To 12.05	12.05 To 1.00	1.00 To 2.00	2.00 To 3.00	3.00 To 4.00	4.00 To 5.00
MON						L U N C H	←-ADE LAB(A2)-→		
TUE		←CPL LAB(A1)→					CPL LAB (B2)	ADE(A)	CPL LAB (B2)
WED	ADE(A)	←CPL LAB(B1)→					←-ADE LAB(C2)-→		
THU			B R E A K		ADE(A)		ML LAB (A)		GATE (V-A)
FRI	ADE(A)						ADE(A)		
SAT									

UNITS: Theory: 12 LAB: 18 Others: -- TOTAL UNITS: 30

Allocation of Subjects (Subjects with Subject Code)

18CPS13	C PROGRAMMING FOR PROBLEM SOLVING
18CPL17	C PROGRAMMING LABORATORY
17CS32	Analog & Digital Electronics
17CSL37	Analog & Digital Electronics Lab

Responsibilities

1	NBA 7 th Criteria
2	Class / EMS Coordinator

Time Table Coordinator

Head of the Department
Alva's Institute of Engineering & Technology
Mijar, MOODBIDRI - 574 225



III Semester CSE A-Section

S. No	USN	Name
1.	4AL15CS050	Kiran A S
2.	4AL16CS047	Madushree R
3.	4AL16CS078	Harshith S
4.	4AL16CS114	Thokchom Sanjit
5.	4AL17CS002	Ajeyashree K
6.	4AL17CS003	Akshat Khandelwal
7.	4AL17CS004	Akshata Narayana Hegde
8.	4AL17CS005	Amrutha M
9.	4AL17CS006	Anilkumar B N
10.	4AL17CS007	Anusha
11.	4AL17CS008	Anvitha Poojary
12.	4AL17CS009	Anvitha U
13.	4AL17CS010	Apeksha Rajendra Rane
14.	4AL17CS011	Apoorva H P
15.	4AL17CS012	Apoorva K N
16.	4AL17CS013	Aruna K
17.	4AL17CS015	Asha Rudrappa Totagi
18.	4AL17CS016	Ashika
19.	4AL17CS017	Ashwini
20.	4AL17CS018	Ashwini Shekarappa Jadamali
21.	4AL17CS019	Bhramari P Shetty
22.	4AL17CS020	Chandana Patil
23.	4AL17CS021	Chetana H
24.	4AL17CS022	Chethana J
25.	4AL17CS024	D Jasmine Joyline
26.	4AL17CS025	Datta Kiran A B
27.	4AL17CS027	Dhanya Bhat
28.	4AL17CS028	Dheeraj Krishna Devadig
29.	4AL17CS029	Dsouza Elston Ronald
30.	4AL17CS030	Gayatri V Kamat
31.	4AL17CS031	Gowda Roshni Shivprakash
32.	4AL17CS032	Harshith C P
33.	4AL17CS033	Hemalatha S
34.	4AL17CS034	Jagath Haren
35.	4AL17CS035	Jayalakshmi M
36.	4AL17CS036	Jayraj ChiragKumar shah
37.	4AL17CS037	John Alsten Tauro
38.	4AL17CS038	K Thrishul
39.	4AL17CS039	Kanaka B S
40.	4AL17CS040	Kavana V
41.	4AL17CS041	Kavya
42.	4AL17CS042	Kavya R Shetty

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
Student List : Academic Year 2018-19

43.	4AL17CS044	Koushik S N
44.	4AL17CS045	Lathik Moger
45.	4AL17CS046	Likitha M
46.	4AL17CS047	M C Suchithra Heggade
47.	4AL17CS048	Madan G Gudigar
48.	4AL17CS049	Madan Gowda V
49.	4AL17CS050	Mhaske Pooja Sambhaji
50.	4AL17CS051	Mahek Sabha
51.	4AL17CS052	Nagashree Arun M
52.	4AL17CS053	Naik Nayana Ganapati
53.	4AL17CS054	Nanditha R Shetty
54.	4AL17CS055	Netra Suresh Gudagamnala
55.	4AL17CS056	Pallavi
56.	4AL17CS057	Pavana P
57.	4AL17CS059	Prajna
58.	4AL17CS096	Soundarya R
59.	4AL17CS097	Spoorthi M S
60.	4AL17CS098	Spoorthi Balaji
61.	4AL17CS114	Niriksha A



H.O.D.

Dept. Of Computer Science & Engineering
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

4. Department Details

4.1 Preliminary Information

THE VISION

Engendering competent, excellent professionals by transforming the knowledge and computing skills to individuals through modern innovative tools and techniques;

THE MISSION

1. • To produce skilled, creative software developers through rigorous training.
2. • To conduct specific technical courses to keep abreast to the latest technological developments and transformations in the domain.
3. • To establish Industry-Institute Interaction programs to enhance the skills of employability and entrepreneurship. • To implement the ideas of research and innovations in interdisciplinary domains.

PROGRAM EDUCATIONAL OBJECTIVES

Peo 1 : PEO1: To provide students with fundamental strength in core disciplines of computer engineering to solve the problems of computing world.

Peo 2 : • PEO2: To ensure that graduates conquer the difficulties of emerging adaptive technological changes.

Peo 3 : • PEO3: To prepare students for successful career in the industry of international standard.

PROGRAM OUTCOME'S (PO's)

1. **Engineering knowledge :** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems
2. **Problem analysis :** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences
3. **Design/development of solutions :** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations
4. **Conduct investigations of complex problems :** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions
5. **Modern tool usage :** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations

4. Department Details

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Peo 3 : • PEO3: To prepare students for successful career in the industry of international standard.

PROGRAM OUTCOME'S (PO's)

6. **The engineer and society** : Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice
7. **Environment and sustainability** : Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development
8. **Ethics** : Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice
9. **Individual and team work** : Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings
10. **Communication** : Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions
11. **Project management and finance** : Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments
12. **Life-long learning** : Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change

PROGRAM SPECIFIC OUTCOME'S (PSO's)

PSO 1 : Professional Skills: The ability to understand & implement the computer programs in the areas of Computer Architecture, System Software, Database Management Systems, Web Design, Multimedia and Computer Networking.

PSO 2 : PSO2: Problem-Solving Skills: The ability to solve real-world problems by suitable mathematical model with strong technological concepts in rapidly growing arena of computer technology.

PSO 3 : PSO3: Successful Career and Entrepreneurship: Knowledge in diverse areas of Software Engineering and Management & Entrepreneurship for IT Industry, conducive in cultivating skills for successful career development.

HOD



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Department of Computer Science and Engineering

SEMESTER III

Course Code: **17CS32** | Course Name: **Analog and Digital Electronics**

Course Teacher: **Mr. Vasudev S Shahapur and Ms. Shilpa**

Course Outcomes: After studying this course, students will be able to:

CO Numbers	Course Outcomes	Blooms Level	Target Level
17CS32.1	Explain the operation of JFETs and MOSFETs, Operational Amplifier circuits and their applications	Remember (L1) Understand (L2)	2
17CS32.2	Describe and interpret different types of combinational logic circuits by using abridge mapping techniques Viz., Karnaugh Maps, Quine-McClusky method and develop program using HDL to simulate the behaviour of various logical circuits.	Understand (L2) Apply (L3) Create (L6)	2
17CS32.3	Design and Demonstrate the Operation of Decoders, Encoders, Multiplexers, Adders and Subtractors and develop program using HDL to simulate the behaviour of various logical circuits. in the domain of economy, performance and efficiency	Apply (L3) Analyze(L4) Evaluate (L5) Create (L6)	2
17CS32.4	Design and implement the working of Latches, Flip-Flops, registers, counters and develop program using HDL to simulate the behaviour of various logical circuits within the realm of economic, performance, efficiency, user friendly and environmental constraints	Apply (L3) Analyze(L4) Evaluate (L5) Create (L6)	
17CS32.5	Demonstrate the fundamental knowledge of analog and digital electronics to get different types of analog to digitalized signal transformation and vice-versa	Understand (L2) Apply(L3)	2

CO-PO/CO-PSO Mapping Matrix:

CO Numbers	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
17CS32.1	2	1											2	1	
17CS32.2	2	1	2	1									2	2	1
17CS32.3	3		2	1		1	1						3	2	1
17CS32.4	3	2	1	1		1	1					1	3	2	1
17CS32.5	2		2										2	2	

CO-PO/CO-PSO Mapping Matrix Justification: Students to

CO Numbers	Justification
17CS32.1	moderately understand the basics of Analog concepts such as MOSFETs, JFET, Opamp etc.
17CS32.2	describe various digital circuits in depth and implement combinational circuits using the concepts Viz., K-map, QM methods and able to develop code in HDL
17CS32.3	design and develop the working of adder, subtractor, decoder, encoder, multiplexer strongly for the given problem and able to develop code in HDL
17CS32.4	devise working of Latches, Flip-Flops, registers, counters strongly and develop program using HDL
17CS32.5	slightly understand and relate the concept of A/D and D/A conversion.

ANALOG AND DIGITAL ELECTRONICS
[As per Choice Based Credit System (CBCS) scheme]
(Effective from the academic year 2017 -2018)

SEMESTER - III

Subject Code	17CS32	IA Marks	40
Number of Lecture Hours/Week	04	Exam Marks	60
Total Number of Lecture Hours	50	Exam Hours	03
CREDITS – 04			
Module -1			Teaching Hours
Field Effect Transistors: Junction Field Effect Transistors, MOSFETs, Differences between JFETs and MOSFETs, Biasing MOSFETs, FET Applications, CMOS Devices. Wave-Shaping Circuits: Integrated Circuit(IC) Multivibrators. Introduction to Operational Amplifier: Ideal v/s practical Opamp, Performance Parameters, Operational Amplifier Application Circuits: Peak Detector Circuit, Comparator, Active Filters, Non-Linear Amplifier, Relaxation Oscillator, Current-To-Voltage Converter, Voltage-To-Current Converter. Text book 1:- Ch5: 5.2, 5.3, 5.5, 5.8, 5.9, 5.1.Ch13: 13.10.Ch 16: 16.3, 16.4. Ch 17: 7.12, 17.14, 17.15, 17.18, 17.19, 17.20, 17.21.)			10 Hours
Module -2			
The Basic Gates: Review of Basic Logic gates, Positive and Negative Logic, Introduction to HDL. Combinational Logic Circuits: Sum-of-Products Method, Truth Table to Karnaugh Map, Pairs Quads, and Octets, Karnaugh Simplifications, Don't-care Conditions, Product-of-sums Method, Product-of-sums simplifications, Simplification by Quine-McClusky Method, Hazards and Hazard covers, HDL Implementation Models. Text book 2:- Ch2: 2.4, 2.5. Ch3: 3.2 to 3.11.			10 Hours
Module – 3			
Data-Processing Circuits: Multiplexers, Demultiplexers, 1-of-16 Decoder, BCD to Decimal Decoders, Seven Segment Decoders, Encoders, Exclusive-OR Gates, Parity Generators and Checkers, Magnitude Comparator, Programmable Array Logic, Programmable Logic Arrays, HDL Implementation of Data Processing Circuits. Arithmetic Building Blocks, Arithmetic Logic Unit Flip- Flops: RS Flip-Flops, Gated Flip-Flops, Edge-triggered RS FLIP-FLOP, Edge-triggered D FLIP-FLOPs, Edge-triggered JK FLIP-FLOPs. Text book 2:- Ch 4:- 4.1 to 4.9, 4.11, 4.12, 4.14.Ch6:-6.7, 6.10.Ch8:- 8.1 to 8.5.			10 Hours
Module-4			
Flip- Flops: FLIP-FLOP Timing, JK Master-slave FLIP-FLOP, Switch Contact Bounce Circuits, Various Representation of FLIP-FLOPs, HDL Implementation of FLIP-FLOP. Registers: Types of Registers, Serial In - Serial Out, Serial In - Parallel out, Parallel In - Serial Out, Parallel In - Parallel Out, Universal Shift Register, Applications of Shift Registers, Register implementation in HDL. Counters: Asynchronous Counters, Decoding Gates, Synchronous Counters, Changing the Counter Modulus. (Text book 2:- Ch 8: 8.6, 8.8, 8.9, 8.10, 8.13. Ch 9: 9.1 to 9.8. Ch 10: 10.1 to 10.4)			10 Hours
Module-5			

Counters: Decade Counters, Presettable Counters, Counter Design as a Synthesis problem, A Digital Clock, Counter Design using HDL. D/A Conversion and A/D Conversion: Variable, Resistor Networks, Binary Ladders, D/A Converters, D/A Accuracy and Resolution, A/D Converter-Simultaneous Conversion, A/D Converter-Counter Method, Continuous A/D Conversion, A/D Techniques, Dual-slope A/D Conversion, A/D Accuracy and Resolution. Text book 2:- Ch 10: 10.5 to 10.9. Ch 12: 12.1 to 12.10	10 Hours
Course outcomes: After Studying this course, students will be able to • Explain the operation of JFETs and MOSFETs , Operational Amplifier circuits and their application • Explain Combinational Logic, Simplification Techniques using Karnaugh Maps, Quine McClusky technique. • Demonstrate Operation of Decoders, Encoders, Multiplexers, Adders and Subtractors, working of Latches, Flip-Flops, Designing Registers, Counters, A/D and D/A Converters • Design of Counters, Registers and A/D & D/A converters	
Question paper pattern: The question paper will have ten questions. There will be 2 questions from each module. Each question will have questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.	
Text Books: 1. Anil K Maini, Varsha Agarwal: Electronic Devices and Circuits, Wiley, 2012. 2. Donald P Leach, Albert Paul Malvino & Goutam Saha: Digital Principles and Applications, 8th Edition, Tata McGraw Hill, 2015	
Reference Books: 1. Stephen Brown, Zvonko Vranesic: Fundamentals of Digital Logic Design with VHDL, 2nd Edition, Tata McGraw Hill, 2005. 2. R D Sudhaker Samuel: Illustrative Approach to Logic Design, Sanguine-Pearson, 2010. 3. M Morris Mano: Digital Logic and Computer Design, 10th Edition, Pearson, 2008.	

ALVA 'S INSTITUTE OF ENGINEERING & TECHNOLOGY

Moodbidri

COURSE BOOK



Period of the Semester : From 1 Aug 2018 To ~~7 Jan 2019~~ 30 Nov 2018

Dept-Sem-Sec : CS-3-A

Subject with Code : ANALOG AND DIGITAL ELECTRONICS 17CS32

Time Slot

Mon :	Tue : 14:00 - 15:00
Wed : 09:00 - 09:55	Thu : 12:05 - 13:00
Fri : 09:00 - 09:55 14:00 - 15:00	Sat :

Name of the Teacher : Shilpa

AIET	Lesson Plan & Execution	
Name of the Faculty	Shilpa	
Dept-Sem-Sec :	CS-3-A	
Date of Commencement	1 Aug 2018	
Last working day of Semester	7 Jan 2019 30-Nov - 2018	
Source Material List		
1	Anil K Maini, Varsha Agarwal: Electronic Devices and Circuits, Wiley, 2012	
2	Donald P Leach, Albert Paul Malvino & Goutam Saha: Digital Principles and Applications, 8th Edition, Tata McGraw Hill, 2015	
1	R D Sudhaker Samuel: Illustrative Approach to Logic Design, Sanguine-Pearson, 2010	
2	M Morris Mano: Digital Logic and Computer Design, 10th Edition, Pearson, 2008	
Course Outcome List		
1	Explain the operation of JFETs and MOSFETs , Operational Amplifier circuits and their application	
2	Describe and interpret different types of combinational logic circuits by using abridge mapping techniques viz., Karnaugh Maps, Quine-McClusky methods and develop program using HDL to simulate the behavior of various logical circuits.	

3	Design and Demonstrate the Operation of Decoders, Encoders, Multiplexers, Adders and Subtractors, and develop program using HDL to simulate the behaviour of various logical circuits in the domain of economy, performance and efficiency.
4	Design and implement the working of Latches, Flip-flops, registers, counters and develop program using HDL to simulate the behaviour of various logical circuits within the realm of economic, performance, efficiency, user friendly and environmental constraints.
5	Demonstrate the fundamental knowledge of analog and digital electronics to get different types of analog to digitalized signal transformation and vice-versa
Subject Name	ANALOG AND DIGITAL ELECTRONICS

Period	Planned			Execution		
	Date	Topic	Source material to be referred	Date	Topic	Source material to be referred
Module 2						
1	1 Aug 2018	Review of Basic Logic gates	TEXT 2	1 Aug 2018	Review of Basic Logic gates	TEXT 2
2	2 Aug 2018	Positive and Negative Logic	TEXT 2	2 Aug 2018	Review of Basic Logic gates	TEXT 2
3	3 Aug 2018	Introduction to HDL	TEXT 2	3 Aug 2018	Positive and Negative Logic	TEXT 2
4	3 Aug 2018	Sum-of-Products Method, Truth Table to Karnaugh Map	TEXT 2	3 Aug 2018	Positive and Negative Logic	TEXT 2
5	7 Aug 2018	Pairs Quads, and Octets, Karnaugh Simplifications	TEXT 2	4 Aug 2018	Introduction to HDL	TEXT 2
6	8 Aug 2018	Don't-care Conditions, Product-of-sums Method	TEXT 2	7 Aug 2018	Sum-of-Products Method	TEXT 2
7	9 Aug 2018	Product-of-sums simplifications	TEXT 2	8 Aug 2018	Truth Table to Karnaugh Map	TEXT 2
8	10 Aug 2018	Simplification by QuineMcClusky Method	TEXT 2	9 Aug 2018	Pairs Quads, and Octets	TEXT 2
9	10 Aug 2018	Hazards and Hazard covers	TEXT 2	10 Aug 2018	Karnaugh Simplifications	TEXT 2
10	14 Aug 2018	HDL Implementation Models	TEXT 2	10 Aug 2018	Karnaugh Simplifications	TEXT 2
Module 3						
11	16 Aug 2018	Multiplexers, Demultiplexers, 1-of-16 Decoder	TEXT 2	11 Aug 2018	Don't-care Conditions	TEXT 2
12	17 Aug 2018	BCD to Decimal Decoders, Seven Segment Decoders	TEXT 2	11 Aug 2018	Product-of-sums Method	TEXT 2
13	17 Aug 2018	Encoders, Exclusive-OR Gates, Parity Generators and Checkers	TEXT 2	16 Aug 2018	Product-of-sums simplifications	TEXT 2
14	21 Aug 2018	Magnitude Comparator, Programmable Array Logic	TEXT 2	18 Aug 2018	Simplification by QuineMcClusky Method	TEXT 2
15	23 Aug 2018	Programmable Logic Arrays, HDL Implementation of Data Processing Circuits	TEXT 2	21 Aug 2018	Simplification by QuineMcClusky Method	TEXT 2

Period	Planned			Execution		
	Date	Topic	Source material to be referred	Date	Topic	Source material to be referred
16	24 Aug 2018	Arithmetic Building Blocks, Arithmetic Logic Unit	TEXT 2	23 Aug 2018	Hazards and Hazard covers	TEXT 2
17	24 Aug 2018	RS Flip-Flops, Gated Flip-Flops	TEXT 2	23 Aug 2018	HDL Implementation Models	TEXT 2
18	28 Aug 2018	Edge-triggered RS FLIP-FLOP	TEXT 2	28 Aug 2018	Multiplexers	TEXT 2
19	29 Aug 2018	Edge-triggered D FLIP-FLOPs	TEXT 2	28 Aug 2018	Multiplexers	TEXT 2
20	30 Aug 2018	Edge-triggered JK FLIPFLOPs	TEXT 2	29 Aug 2018	Multiplexers, Demultiplexers	TEXT 2
Module 4						
21	31 Aug 2018	FLIP-FLOP Timing, JK Master-slave FLIP-FLOP	TEXT 2	30 Aug 2018	Demultiplexers	TEXT 2
22	31 Aug 2018	Switch Contact Bounce Circuits, Various Representation of FLIP-FLOPs	TEXT 2	31 Aug 2018	1-of-16 Decoder	TEXT 2
23	4 Sep 2018	HDL Implementation of FLIP-FLOP	TEXT 2	31 Aug 2018	1-of-16 Decoder	TEXT 2
24	5 Sep 2018	Types of Registers, Serial In - Serial Out	TEXT 2	4 Sep 2018	BCD to Decimal Decoders	TEXT 2
25	11 Sep 2018	Serial In - Parallel out, Parallel In -Serial Out	TEXT 2	5 Sep 2018	Seven Segment Decoders	TEXT 2
26	12 Sep 2018	Parallel In - Parallel Out, Universal Shift Register	TEXT 2	6 Sep 2018	Encoders	TEXT 2
27	14 Sep 2018	Applications of Shift Registers, Register implementation in HDL	TEXT 2	7 Sep 2018	Exclusive-OR Gates	TEXT 2
28	14 Sep 2018	Asynchronous Counters	TEXT 2	7 Sep 2018	Parity Generators and Checkers	TEXT 2
29	18 Sep 2018	Decoding Gates, Synchronous Counters	TEXT 2	11 Sep 2018	Magnitude Comparator	TEXT 2
30	19 Sep 2018	Changing the Counter Modulus	TEXT 2	12 Sep 2018	Programmable Array Logic	TEXT 2
Module 5						
31	20 Sep 2018	Decade Counters, Presettable Counters	TEXT 2	14 Sep 2018	Programmable Logic Arrays, HDL Implementation of Data Processing Circuits	TEXT 2

Period	Planned			Execution		
	Date	Topic	Source material to be referred	Date	Topic	Source material to be referred
32	25 Sep 2018	Counter Design as a Synthesis problem	TEXT 2	14 Sep 2018	Arithmetic Building Blocks	TEXT 2
33	26 Sep 2018	A Digital Clock	TEXT 2	20 Sep 2018	Arithmetic Logic Unit	TEXT 2
34	27 Sep 2018	Counter Design using HDL	TEXT 2	24 Sep 2018	RS Flip-Flops, Gated Flip-Flops	TEXT 2
35	28 Sep 2018	Variable, Resistor Networks, Binary Ladders	TEXT 2	25 Sep 2018	Edge-triggered RS FLIP-FLOP	TEXT 2
36	28 Sep 2018	D/A Converters, D/A Accuracy and Resolution	TEXT 2	27 Sep 2018	Edge-triggered D FLIP-FLOPs	TEXT 2
37	3 Oct 2018	A/D Converter-Simultaneous Conversion	TEXT 2	27 Sep 2018	Edge-triggered JK FLIPFLOPs	TEXT 2
38	4 Oct 2018	A/D Converter-Counter Method, Continuous A/D Conversion	TEXT 2	28 Sep 2018	FLIP-FLOP Timing, JK Master-slave FLIP-FLOP	TEXT 2
39	5 Oct 2018	A/D Techniques, Dual-slope A/D Conversion	TEXT 2	28 Sep 2018	Switch Contact Bounce Circuits	TEXT 2
40	5 Oct 2018	Dual-slope A/D Conversion, A/D Accuracy and Resolution	TEXT 2	28 Sep 2018	Various Representation of FLIP-FLOPs, HDL Implementation of FLIP-FLOP	TEXT 2
Module 1						
41	9 Oct 2018	Junction Field Effect Transistors, MOSFETs	TEXT 1	3 Oct 2018	Types of Registers, Serial In - Serial Out	TEXT 2
42	10 Oct 2018	Differences between JFETs and MOSFETs, Biasing MOSFETs	TEXT 1	4 Oct 2018	Serial In - Parallel out, Parallel In - Parallel Out	TEXT 2
43	11 Oct 2018	FET Applications, CMOS Devices	TEXT 1	5 Oct 2018	Parallel In -Serial Out, Universal Shift Register	TEXT 2
44	12 Oct 2018	Integrated Circuit(IC) Multivibrators	TEXT 1	5 Oct 2018	Applications of Shift Registers, Register implementation in HDL	TEXT 2
45	12 Oct 2018	Ideal v/s practical Opamp	TEXT 1	9 Oct 2018	Asynchronous Counters	TEXT 2
46	23 Oct 2018	Performance Parameters	TEXT 1	9 Oct 2018	Decoding Gates, Synchronous Counters	TEXT 2
47	24 Oct 2018	Peak Detector Circuit, Comparator	TEXT 1	10 Oct 2018	Synchronous Counters, Changing the Counter Modulus	TEXT 2

Period	Planned			Execution		
	Date	Topic	Source material to be referred	Date	Topic	Source material to be referred
48	25 Oct 2018	Active Filters, NonLinear Amplifier	TEXT 1	11 Oct 2018	Decade Counters, Presettable Counters	TEXT 2
49	26 Oct 2018	Relaxation Oscillator, Current-To-Voltage Converter	TEXT 1	12 Oct 2018	Counter Design as a Synthesis problem	TEXT 2
50	26 Oct 2018	Current-To-Voltage Converter, Voltage-To-Current Converter	TEXT 1	12 Oct 2018	Counter Design as a Synthesis problem	TEXT 2
Module 2						
51	30 Oct 2018	Review of Basic Logic gates, Positive and Negative Logic, Introduction to HDL	TEXT 2	16 Oct 2018	A Digital Clock, Counter Design using HDL	TEXT 2
52	31 Oct 2018	Sum-of-Products Method, Truth Table to Karnaugh Map, Pairs Quads, and Octets	TEXT 2	23 Oct 2018	Variable, Resistor Networks, Resistor Networks	TEXT 2
53	2 Nov 2018	Karnaugh Simplifications, Don't-care Conditions, Product-of-sums Method, Product-of-sums simplifications	TEXT 2	24 Oct 2018	Binary Ladders	TEXT 2
54	2 Nov 2018	Product-of-sums simplifications, Simplification by QuineMcClusky Method, Hazards and Hazard covers, HDL Implementation Models	TEXT 2	30 Oct 2018	D/A Converters, D/A Accuracy and Resolution	TEXT 2
Module 3						
55	7 Nov 2018	Multiplexers, Demultiplexers, 1-of-16 Decoder, BCD to Decimal Decoders, Seven Segment Decoders	TEXT 2	31 Oct 2018	A/D Converter-Simultaneous Conversion	TEXT 2
56	9 Nov 2018	Exclusive-OR Gates, Parity Generators and Checkers, Magnitude Comparator, Programmable Array Logic, HDL Implementation of Data Processing Circuits	TEXT 2	2 Nov 2018	A/D Techniques, Dual-slope A/D Conversion	TEXT 2

Period	Planned			Execution		
	Date	Topic	Source material to be referred	Date	Topic	Source material to be referred
57	9 Nov 2018	RS Flip-Flops, Gated Flip-Flops, Edge-triggered RS FLIP-FLOP	TEXT 2	2 Nov 2018	Dual-slope A/D Conversion, A/D Accuracy and Resolution	TEXT 2
58	13 Nov 2018	Edge-triggered D FLIP-FLOPs, Edge-triggered JK FLIPFLOPs	TEXT 2	5 Nov 2018	Junction Field Effect Transistors	TEXT 1
Module 4						
59	14 Nov 2018	JK Master-slave FLIP-FLOP, Switch Contact Bounce Circuits, Various Representation of FLIP-FLOPs, HDL Implementation of FLIP-FLOP	TEXT 2	13 Nov 2018	Biasing MOSFETs, MOSFETs	TEXT 1
60	15 Nov 2018	Serial In - Serial Out, Serial In - Parallel out, Parallel In -Serial Out, Universal Shift Register, Register implementation in HDL	TEXT 2	14 Nov 2018	FET Applications, CMOS Devices, Differences between JFETs and MOSFETs	TEXT 1
61	16 Nov 2018	Asynchronous Counters, Decoding Gates, Synchronous Counters, Changing the Counter Modulus	TEXT 2	17 Nov 2018	Integrated Circuit(IC) Multivibrators	TEXT 1
Module 5						
62	16 Nov 2018	Decade Counters, Counter Design as a Synthesis problem, Counter Design using HDL	TEXT 2	19 Nov 2018	Ideal v/s practical Opamp, Performance Parameters	TEXT 1
63	20 Nov 2018	Variable, Binary Ladders, Resistor Networks, D/A Accuracy and Resolution	TEXT 2	20 Nov 2018	Performance Parameters	TEXT 1
64	22 Nov 2018	A/D Converter-Counter Method, Continuous A/D Conversion, A/D Techniques, A/D Accuracy and Resolution, Dual-slope A/D Conversion	TEXT 2	21 Nov 2018	Peak Detector Circuit, Comparator	TEXT 1

Period	Planned			Execution		
	Date	Topic	Source material to be referred	Date	Topic	Source material to be referred
Module 1						
65	23 Nov 2018	Junction Field Effect Transistors, MOSFETs, Biasing MOSFETs, FET Applications	TEXT 1	21 Nov 2018	Active Filters, NonLinear Amplifier	TEXT 1
66	23 Nov 2018	Integrated Circuit(IC) Multivibrators	TEXT 1	22 Nov 2018	Relaxation Oscillator, Current-To-Voltage Converter	TEXT 1
67	29 Nov 2018	Ideal v/s practical Opamp, Performance Parameters	TEXT 1	23 Nov 2018	Current-To-Voltage Converter, Voltage-To-Current Converter	TEXT 1
68	30 Nov 2018	Peak Detector Circuit, Comparator, Active Filters	TEXT 1	24 Nov 2018	Review of Basic Logic gates, Positive and Negative Logic, Introduction to HDL	TEXT 2
69	30 Nov 2018	Relaxation Oscillator, Current-To-Voltage Converter, Voltage-To-Current Converter, NonLinear Amplifier	TEXT 1	29 Nov 2018	Sum-of-Products Method, Truth Table to Karnaugh Map, Pairs Quads, and Octets	TEXT 2
70				30 Nov 2018	Karnaugh Simplifications, Don't-care Conditions, Product-of-sums Method, Product-of-sums simplifications	TEXT 2

Module No.	# of Classes Planned (till date)	Planned Effort (till date)	# of Classes Executed (till date)	Actual Effort (till date)	% Coverage
2	20	18hrs 20min	20	18hrs 20min	100.0
3	20	18hrs 20min	20	18hrs 20min	100.0
4	10	9hrs 10min	10	9hrs 10min	100.0
5	10	9hrs 10min	10	9hrs 10min	100.0
1	10	9hrs 10min	10	9hrs 10min	100.0


Faculty in charge


HOD's Signature


Signature of Principal (& responsible for)

Alva's Institute of Engg. & Technology
Mijar, MOODESIDRI - 574 225

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY, MOODBIDRI
 DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
 I - INTERNAL ASSESSMENT

Semester:3-CBCS2017

Subject: ANALOGANDDIGITALELECTRONICS(17CS32)

Faculty: Ms Shilpa

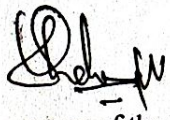
Date:17Sep2018

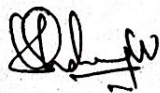
Time:03:00PM-04:30PM

MaxMarks:30

Answer any 2question(s)

Q.No		Marks	CO	BT/CL
1 a	Simplify $y=f(A,B,C,D) = \sum m(0,1,4,5,7,13,15) + d(2,8,10)$ using K-map.	5	CO2	L3
1 b	Simplify $y=f(A,B,C,D) = \sum m(2,5,7,8,13,15) + d(0,10)$ using QM method and draw logic circuit using nand gate only.	6	CO2	L3
1 c	Explain Positive and Negative Logics with examples.	4	CO2	L2
OR				
2 a	Construct a Digital System in which the names of week days are given as input in the form of 3 bits and assign binary values from Sunday=000, Monday=001, Tuesday =010 and so on up to Saturday = 110. The output of the system must be '1' corresponding to week day name consists of '6' characters or otherwise it is '0'. Let 111 = X (Don't care term). For the abovesystem i. Write the Truth Table and Boolean Expressions for min.terms, maxterms ii. Simplify all canonical min terms Boolean Expression usingK-map	5	CO2	L3
2 b	UsingQMmethod,simplifytheexpression $f(A,B,C,D)=\sum m(0,3,5,6,7,11,14)$ anddrawthe logic circuit using nor gateonly.	6	CO2	L3
2 c	What are 0-Hazard and 1-Hazard ? Explain how to eliminate Hazards using K-map	4	CO2	L2
3 a	Construct Binary to Gray convertor using basic gate and give simplifiedboolean expression for each bit.	5	CO3	L4
3 b	Implement $y=f(A,B,C,D) = \sum m(0,2,3,5,7,10,12,13)$ using 8:1 Multiplexer with the help of D variable as entered variable.	6	CO3	L3
3 c	Construct 16:1 multiplexer using 4:1 and 2:1 multiplexer.	4	CO3	L3
OR				
4 a	Explain1:8Demultiplexerandshowhow1:8demultiplexercanbeusedtoconstruct1:16 demultiplexer.	5	CO3	L4
4 b	Whatismagnitudecomparator?Construct2-bitcomparatortruthtableanddrawlogic circuitdiagramforsimplifiedoutputs.	6	CO3	L3
4 c	Write a veilog code for Full adder circuit and Full subtractor circuit.	4	CO3	L3


 Signature of the Faculty


 Signature of IQAC member

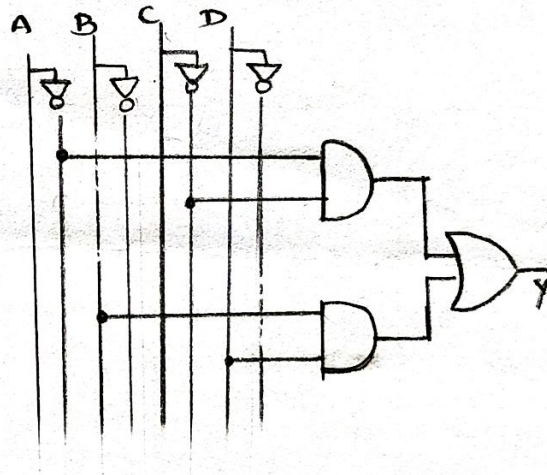

 Signature of HOD

Semester: 3-CBCS 2017
Subject: ANALOG AND DIGITAL ELECTRONICS(17CS32)
Faculty: Ms. Shilpa
Mr. Vasudev S Shahapur

Date: 17 Sep 2018
Time: 03:00PM-04:30PM
Max Marks: 30

Answer any 2 question(s)

Q.No		Marks	CO	BT/CL																																																																																																														
1 a	Simplify $y=f(A,B,C,D) = \sum m(0,1,4,5,7,13,15) + d(2,8,10)$ using K-map. Truth table <table border="1"> <thead> <tr> <th>A</th><th>B</th><th>C</th><th>D</th><th>Y</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>X</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>X</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>X</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>AB \ CD</th><th>C'D'</th><th>C'D</th><th>CD</th><th>CD'</th></tr> </thead> <tbody> <tr> <th>A'B'</th><td>1</td><td>1</td><td>0</td><td>X</td></tr> <tr> <th>A'B</th><td>1</td><td>1</td><td>1</td><td>0</td></tr> <tr> <th>AB</th><td>0</td><td>1</td><td>1</td><td>0</td></tr> <tr> <th>AB'</th><td>X</td><td>0</td><td>0</td><td>X</td></tr> </tbody> </table> $Y = A'C' + BD$	A	B	C	D	Y	0	0	0	0	1	0	0	0	1	1	0	0	1	0	X	0	0	1	1	0	0	1	0	0	1	0	1	0	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	X	1	0	0	1	0	1	0	1	0	X	1	0	1	1	0	1	1	0	0	0	1	1	0	1	1	1	1	1	0	0	1	1	1	1	1	AB \ CD	C'D'	C'D	CD	CD'	A'B'	1	1	0	X	A'B	1	1	1	0	AB	0	1	1	0	AB'	X	0	0	X	1+2+1+1	CO2	L3
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1 b

Simplify $y=f(A,B,C,D) = \sum m(2,5,7,8,13,15) + d(0,10)$ using QM method and draw logic circuit using nand gate only.

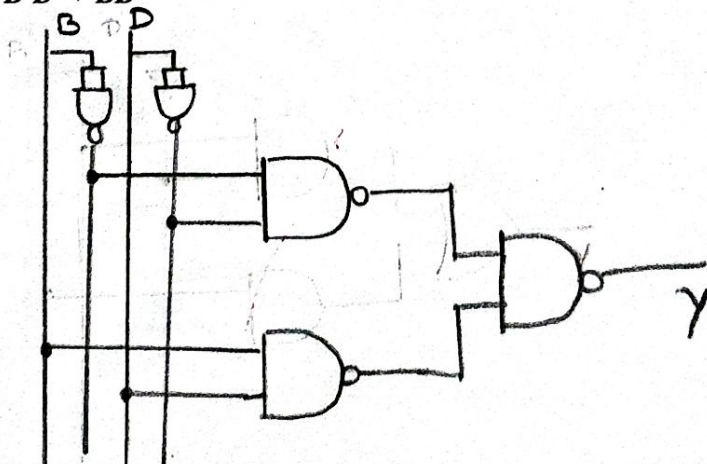
A	B	C	D	Y
0	0	0	0	X
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	X
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Stage 1	Stage 2	Stage 3	Stage 4
0000 (0)	00_0 (0,2) _000 (0,8)	_0_0 (0,2,8,10) _0_0 (0,8,2,10)	_0_0 (0,2,8,10) _1_1 (5,7,13,15)
0010 (2)			
1000 (8)	_010 (2,10) 10_0 (8,10)	_1_1 (5,7,13,15) _1_1 (5,13,7,15)	
0101 (5)	01_1 (5,7)		
1010 (10)	_101 (5,13) _111 (7,15)		
0111 (7)	11_1 (13,15)		
1101 (13)			
1111 (15)			

Prime implicants	2	5	7	8	13	15
B'D'	*			*		
BD		*	*		*	*

Therefore essential prime implicants are :

$$Y = B'D' + BD$$



1+2+
1+1+
1

CO2

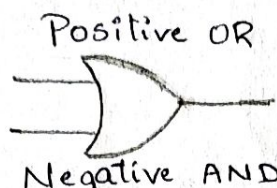
L3

1 c

Explain Positive and Negative Logics with examples.

In positive logic a binary 0 represents low voltage and a binary 1 for high voltage. In negative logic where binary 0 stands for high voltage and binary 1 for low voltage.

Example



An OR gate in a positive logic system becomes an AND gate in a negative logic system. In a positive logic system, binary 0 stands for low and binary 1 for high. So, we can convert Table (a) to Table (b). Y is a 1 if either A or B is 1 which is OR gate. In a negative logic system, binary 1 stands for low and binary 0 for high. With this code, we can convert Table (a) to Table (c). The output Y is a 1 only when both A and B are 1. This is like an AND gate.

A	B	Y
Low	Low	Low
Low	High	High
High	Low	High
High	High	

Table (a)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Table (b)

A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

Table (c)

OR

2 a

Construct a Digital System in which the names of week days are given as input in the form of 3 bits and assign binary values from Sunday=000, Monday=001, Tuesday=010 and so on up to Saturday=110. The output of the system must be '1' corresponding to week day name consists of '6' characters or otherwise it is '0'. Let 111 = X (Don't care term). For the above system

- Write the Truth Table and Boolean Expressions for min terms, maxterms
- Simplify all canonical min terms Boolean Expression using K-map

i)

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	X

Boolean expression for minterms is

$$Y = \sum m(0,1,5) + d(7) \text{ OR } A'B'C' + A'B'C + AB'C$$

Boolean expression for maxterms is

$$Y = \prod M(2,3,4,6) + d(7)$$

OR

$$(A'+B+C')(A'+B+C)(A+B'+C')(A+B+C')$$

2+2

CO2

L2

1+2+2

CO2

L3

ii)

	C'	C
A'B'	1	1
A'B	0	0
AB	0	X
AB'	0	1

$$Y = A'B' + AC$$

2 b

Using QM method, simplify the expression $f(A,B,C,D) = \sum m(0,3,5,6,7,11,14)$ and draw the logic circuit using nor gate only.

1+2+
+1+1

CO2

L3

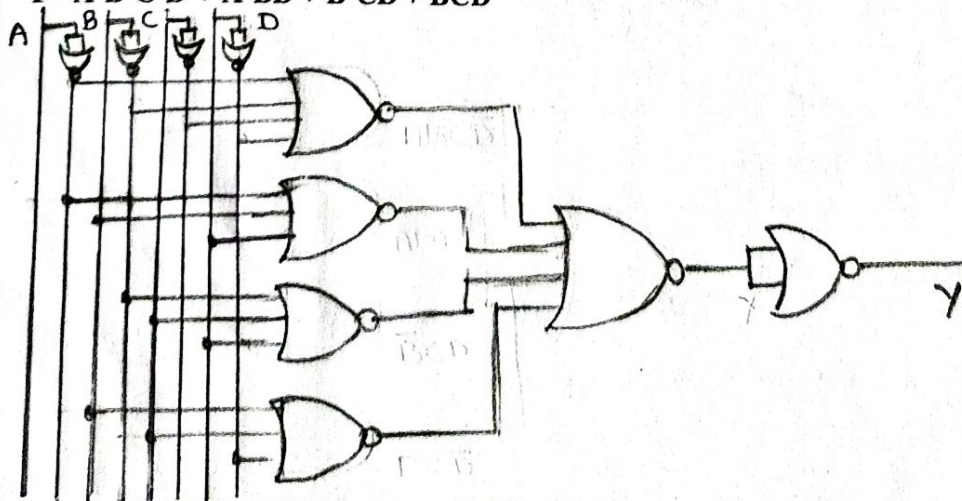
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

Stage 1	Stage 2
0000 (0)	0_11 (3,7)
0011 (3)	0_11 (3,11)
0101 (5)	01_1 (5,7)
0110 (6)	_110 (6,14)
0111 (7)	
1011 (11)	
1110 (14)	

Prime implicants	0	3	5	6	7	11	14
A'CD		*			*		
B'CD		*				*	
A'BD			*		*		
BCD'				*			*
A'B'C'D'	*						

Therefore essential prime implicants are :

$$Y = A'B'C'D' + A'BD + B'CD + BCD'$$



2 c

What are 0-Hazard and 1-Hazard ? Explain how to eliminate Hazards using K-map

2+2

CO2

L2

Static 1 Hazards

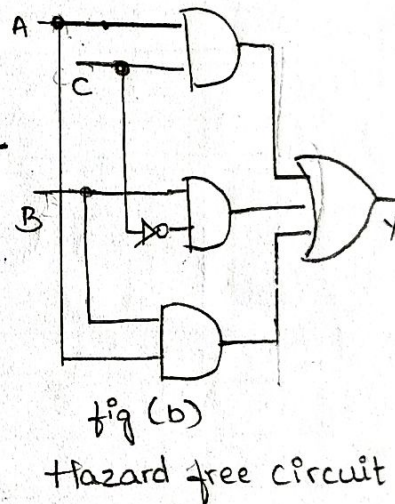
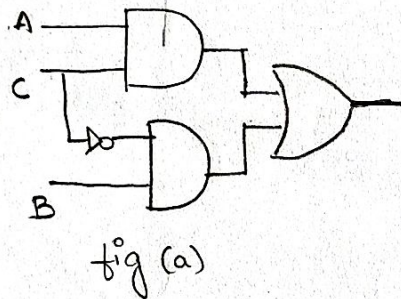
This type of hazard occurs when $Y = A + A'$ type of situation appears for a logic circuit for certain combination of other inputs and A makes a transition $1 \sim 0$. An $A + A'$ condition should always generate 1 at the output.

Static 0 Hazards

This type of hazard occurs when $Y = A.A'$ kind of situation occurs in a logic circuit for certain combination of other inputs and A makes a transition $0 \rightarrow 1$. An $A.A'$ condition should always generate 0 at the output.

Karnaugh map shown in Fig, which is minimally represented by $Y = BC' + AC$. The corresponding circuit is shown in Fig. b. Consider, for this circuit input $B = 1$ and $A = 1$ and then C makes transition $1 \sim 0$. Consider another grouping for the same map in Fig. c. This includes one additional term AB and now output $Y = BC' + AC + AB$. The additional term AB ensures $Y = 1$ for $A = 1, B = 1$ through the third input of final OR gate and a $1 \sim 0$ transition at C does not affect output.

	C	$\bar{C}$	C
$\bar{A}\bar{B}$	0	0	
$\bar{A}B$	1	0	
$A\bar{B}$	1	1	
AB	0	1	



3 a

Construct Binary to Gray convertor using basic gate and give simplified Boolean expression for each bit.

2+2+
1

CO3

L4

Binary				Gray			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

K map simplification

		B1B0			
B3B2	B1B0	B1'B0'	B1'B0	B1B0	B1B0'
	B3'B2'	0	0	0	0
	B3'B2	0	0	0	0
	B3B2	1	1	1	1
	B3B2'	1	1	1	1

$$G3 = B3$$

		B1B0			
B3B2	B1B0	B1'B0'	B1'B0	B1B0	B1B0'
	B3'B2'	0	0	0	0
	B3'B2	1	1	1	1
	B3B2	0	0	0	0
	B3B2'	1	1	1	1

$$G2 = B3 \oplus B2$$

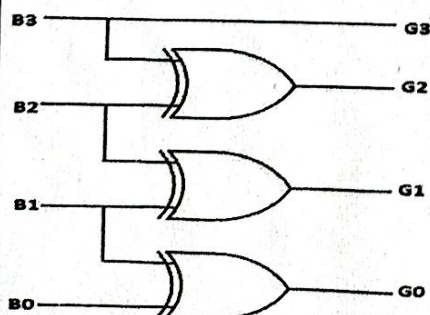
		B1B0			
B3B2	B1B0	B1'B0'	B1'B0	B1B0	B1B0'
	B3'B2'	0	0	1	1
	B3'B2	1	1	0	0
	B3B2	1	1	0	0
	B3B2'	0	0	1	1

$$G1 = B2 \oplus B1$$

		B1B0			
B3B2	B1B0	B1'B0'	B1'B0	B1B0	B1B0'
	B3'B2'	0	1	0	1
	B3'B2	0	1	0	1
	B3B2	0	1	0	1
	B3B2'	0	1	0	1

$$G0 = B1 \oplus B0$$

Logic diagram



3 b

Implement $y=f(A,B,C,D) = \sum m(0,2,3,5,7,10,12,13)$ using 8:1 Multiplexer with the help of D variable as entered variable.

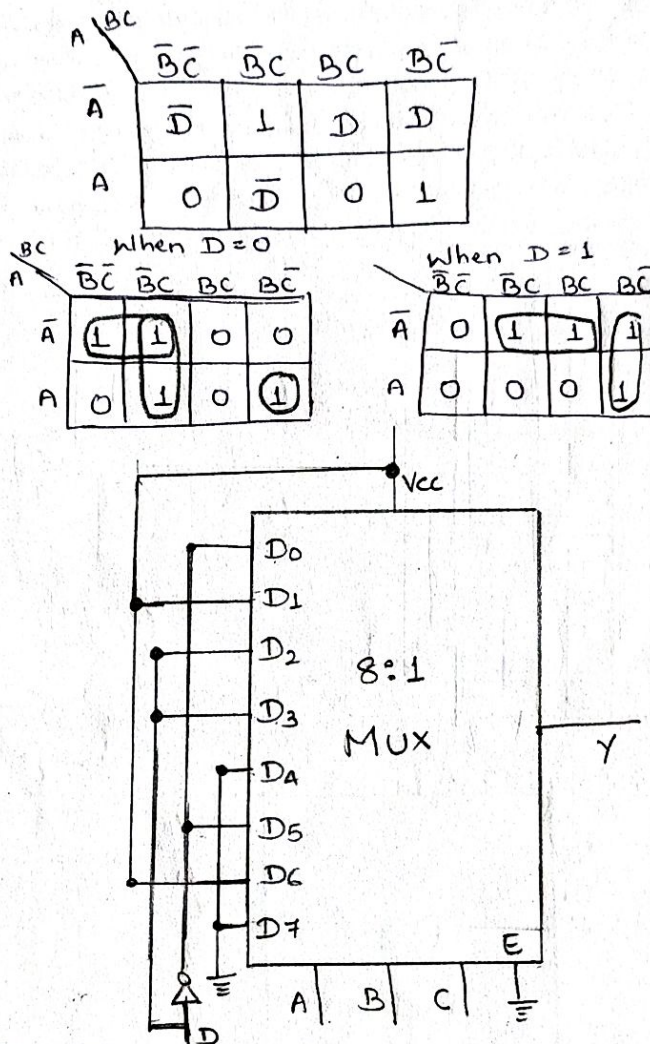
1+2+
1+2

CO3

L3

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

A	B	C	Y
0	0	0	D'
0	0	1	1
0	1	0	D
0	1	1	D
1	0	0	0
1	0	1	D'
1	1	0	1
1	1	1	0



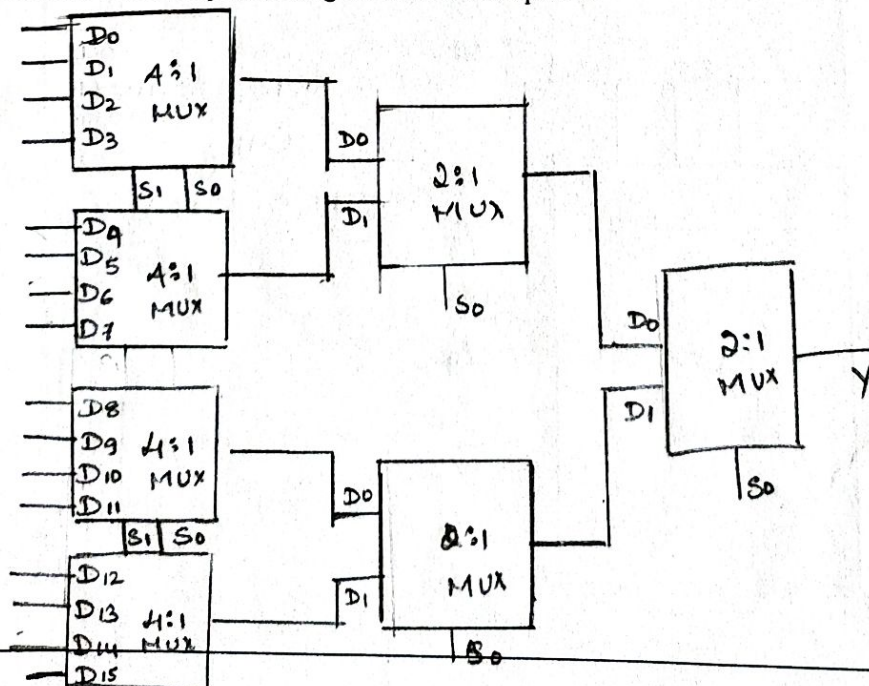
3 c

Construct 16:1 multiplexer using 4:1 and 2:1 multiplexer.

2+2

CO3

L3



4 a

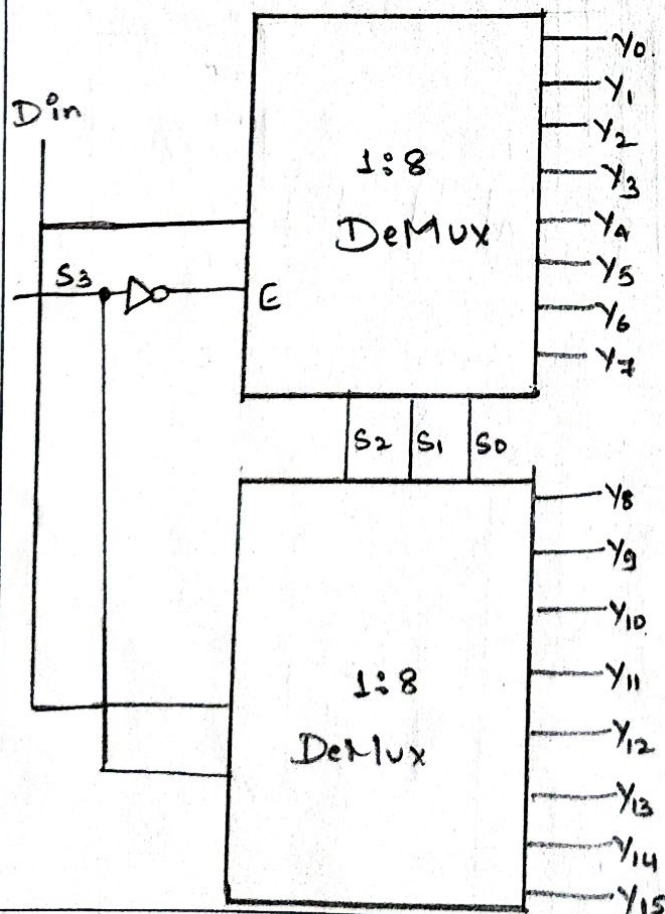
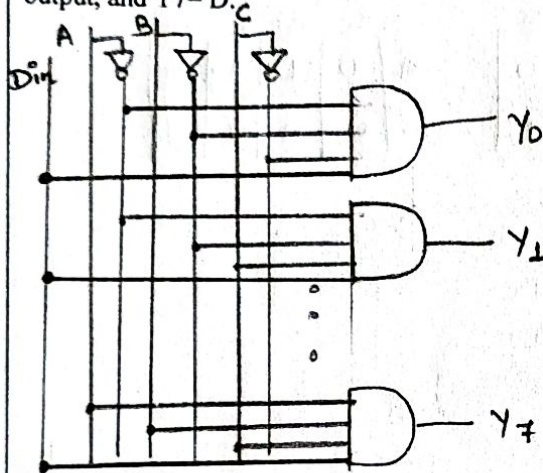
Explain 1:8 demultiplexer and show how 1:8 demultiplexer can be used to construct 1:16 demultiplexer.

3+2

CO3

L4

Figure shows a 1-to-8 demultiplexer. The input bit is labeled D. This data bit (D) is transmitted to the data bit of the output lines, this depends on the value of ABCD, the control input. When ABCD = 0000, the upper AND gate is enabled while all other AND gates are disabled. Therefore, data bit D is transmitted only to the Y_0 output, giving $Y_0 = D$. If D is low, Y_0 is low. If D is high, Y_0 is high, the value of Y_0 depends on the value of D. All other outputs are in the low state. If the control nibble is changed to ABCD = 1111, all gates are disabled except the bottom AND gate. Then, D is transmitted only to the Y_7 output, and $Y_7 = D$.



1:16 Demux
using
1:8 Demux

4 b

What is Magnitude comparator? Construct 2-bit comparator truth table and draw logic circuit diagram for simplified outputs.

Magnitude comparator is a combinational circuit which takes 2 n bit word as input and produces 3 outputs namely $X > Y$, $X < Y$, $X = Y$.

A1	A0	B1	B0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

	B1'B0'	B1'B0	B1B0	B1B0'
A0'A1'	0	0	0	0
A0'A1	1	0	0	0
A0A1	1	1	0	1
A0A1'	1	1	0	0

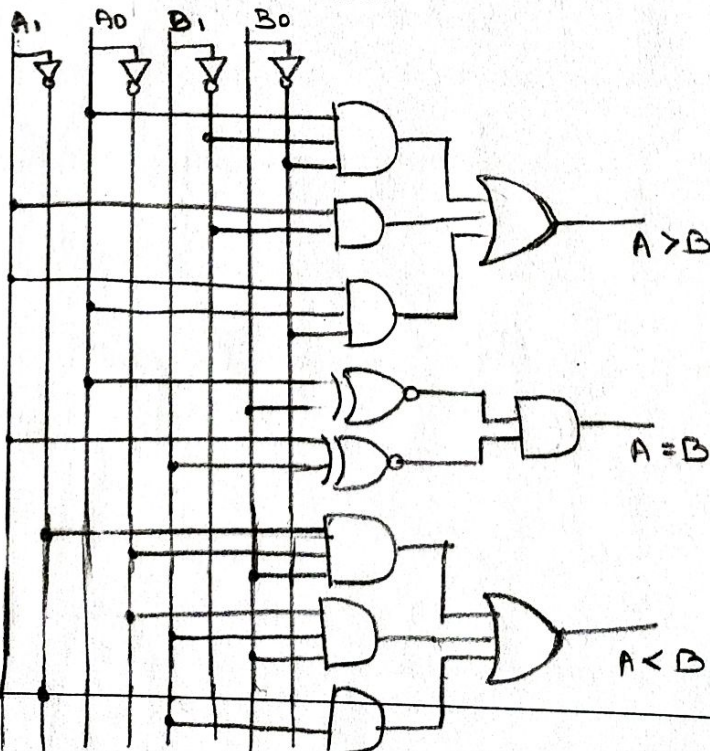
$$A > B = A0B1'B01 + A1B1' + A1A0B0'$$

	B1'B0'	B1'B0	B1B0	B1B0'
A0'A1'	1	0	0	0
A0'A1	0	1	0	0
A0A1	0	0	1	0
A0A1'	0	0	0	1

$$(A = B) = (A0 \oplus B0)'(A1 \oplus B1)'$$

	B1'B0'	B1'B0	B1B0	B1B0'
A0'A1'	0	1	1	1
A0'A1	0	0	1	1
A0A1	0	0	0	0
A0A1'	0	0	1	0

$$A < B = A1'A0'B0 + A0'B1B0 + A1'B1$$

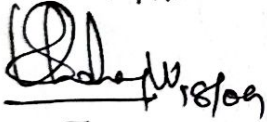
1+1+2
+2

CO3

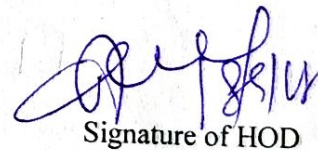
L3

4 c	Write a verilog code for Full adder circuit and Full subtractor circuit.	2+2	CO3	L3
	Module fulladder (A, B, C, Sum, Carry) Input: A, B, C; Output: Sum, Carry; Wire: P, Q, R; xor(Sum, A, B, C); and (P, A, B); and (Q, A, C); and (R, B, C); or (Carry, P, Q, R); end module OR Module fulladder (A, B, C, Sum, Carry) Input: A, B, C; Output: Sum, Carry; assign Sum= (A ^ B ^ C); assign Carry= ((A&B) (A&C) (B&C)); end module	Module fullsubtractor (A, B, C, Diff, Br) Input: A, B, C; Output: Sum, Carry; Wire: P, Q, R; xor(Diff, A, B, C); and (P, ~A, B); and (Q, ~A, C); and (R, B, C); or (Br, P, Q, R); end module OR Module fullsubtractor (A, B, C, Diff, Br) Input: A, B, C; Output: Sum, Carry; assign Diff= (A ^ B ^ C); assign Br= ((~A&B) (~A&C) (B&C)); end module		

18/9/18



Signature of the Faculty



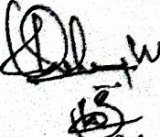
Signature of HOD

Semester: 3-CBCS 2017
Subject: ANALOG AND DIGITAL ELECTRONICS(17CS32)
Faculty: Ms. Shilpa
Mr. Vasudev S Shahpur

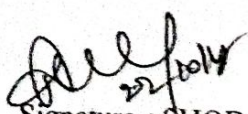
Date: 25 Oct 2018
Time: 03:00 PM - 04:30 PM
Max Marks: 30

Answer any 2 question(s)

Q.No		Marks	CO	BT/CL
1	a What is PLA? Design 7-segment decoder using PLA.	5	CO3	L6
	b Derive the Characteristic equation , excitation table and state diagram for JK flip flop and D flip flop.	6	CO4	L6
	c What is decoder? Realize the following function using 3:8 decoder. $f_1(A,B,C)=\sum m(1,2,3,4)$ and $f_2(A,B,C)=\sum m(3,5,7)$.	4	CO3	L2
OR				
2	a Write a Verilog code for the following. i) 3:8 Decoder. ii) SR flip flop.	5	CO3	L6
	b With neat logic diagram and truth table, explain the working of JK master slave flip flop.	6	CO4	L2
	c Distinguish between PLA and PAL.	4	CO3	L4
3	a List the different types of shift registers. With an example explain 4 bit Serial In Serial Out (SISO) register using negative edge triggered D flip flop.	5	CO4	L2
	b Design Synchronous MOD-7 JK flip flop counter using synthesization along with the timing diagram.	6	CO4	L6
	c Distinguish between combinational circuit and sequential circuit.	4	CO4	L4
OR				
4	a Explain 3 bit binary Ripple up counter with its block diagram, truth table and output waveform.	5	CO4	L2
	b Design Synchronous counter for the sequences $0 \rightarrow 4 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 0$, using D flip flop.	6	CO4	L6
	c Explain Ring counter and Johnson counter.	4	CO4	L2


Signature of the faculty


Signature of IQAC member


Signature of HOD

Semester: 3-CBCS 2017
Subject: ANALOG AND DIGITAL ELECTRONICS(17CS32)
Faculty: Ms. Shilpa
Mr. Vasudev S Shahpur

Date: 25 Oct 2018
Time: 03:00 PM - 04:30 PM

Max Marks: 30

Answer any 2 question(s)

Q.No		Marks	CO	BT/CI																																																																																																																									
1	a	5	CO3	L6																																																																																																																									
	What is PLA? Design 7-segment decoder using PLA. A programmable logic array (PLA) is a kind of programmable logic device used to implement combinational logic circuits. The PLA has a set of programmable AND gate planes, which link to a set of programmable OR gate planes. <table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>C</th> <th>D</th> <th>a</th> <th>b</th> <th>c</th> <th>d</th> <th>e</th> <th>f</th> <th>g</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> </tbody> </table>	A	B	C	D	a	b	c	d	e	f	g	0	0	0	0	1	1	1	1	1	1	0	0	0	0	1	0	1	1	0	0	0	0	0	0	1	0	1	1	0	1	1	0	1	0	0	1	1	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	1	1	0	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	0	1	1	1M	4M	
A	B	C	D	a	b	c	d	e	f	g																																																																																																																			
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0	0	0	1	0	1	1	0	0	0	0																																																																																																																			
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0	1	1	0	1	0	1	1	1	1	1																																																																																																																			
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1	0	0	0	1	1	1	1	1	1	1																																																																																																																			
1	0	0	1	1	1	1	1	0	1	1																																																																																																																			

b Derive the Characteristic equation , excitation table and state diagram for JK flip flop and D flip flop.

6 CO4 L6

Characteristic table of JK flip flop

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

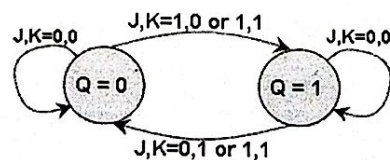
	$J'K'$	$J'K$	JK	JK'
Q_n'	0	0	1	1
Q_n	1	0	0	1

$$Q_{n+1} = J Q_n' + K' Q_n$$

Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

State Diagram



3M

Characteristic table of D flip flop

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

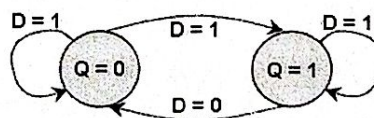
	D'	D
Q_n'	0	1
Q_n	0	1

$$Q_{n+1} = D$$

Excitation Table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

State Diagram



3M

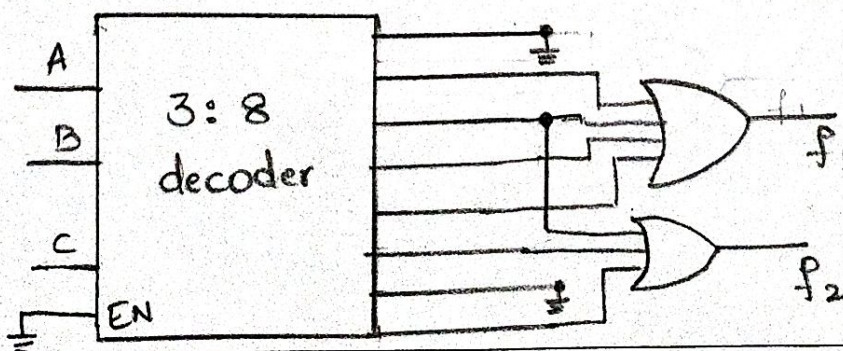
What is decoder? Realize the following function using 3:8 decoder.

c $f_1(A,B,C) = \sum m(1,2,3,4)$ and $f_2(A,B,C) = \sum m(3,5,7)$.

4 CO3 L2

In digital electronics, a binary decoder is a combinational logic circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs.

1M



3M

OR

Write a Verilog code for the following.
i) 3:8 Decoder.

5

CO3

L6

2.5M

```
module
decoder(a,b,c,d0,d1,d2,d3,d4,d5,d6,d7);
  input a,b,c;
  output d0,d1,d2,d3,d4,d5,d6,d7;
  assign d0=(~a&~b&~c),
  assign d1=(~a&~b&c),
  assign d2=(~a&b&~c),
  assign d3=(~a&b&c),
  assign d4=(a&~b&~c),
  assign d5=(a&~b&c),
  assign d6=(a&b&~c),
  assign d7=(a&b&c);
endmodule
```

```
module decoder (a,b,c,d0,d1,d2,d3,d4,
d5,d6,d7);
  input a,b,c;
  output d0,d1,d2,d3,d4,d5,d6,d7;
  reg d0,d1,d2,d3,d4,d5,d6,d7;
  always @(a or b or c)
  case ({a,b,c})
  0: Y0=1;
  1: Y1=1;
  2: Y2=1;
  3: Y3=1;
  4: Y4=1;
  5: Y5=1;
  6: Y6=1;
  7: Y7=1;
  endcase
endmodule
```

ii) SR flip flop.

2.5M

```
module SRFF( clk, clr, Q)
  inputs Clk, clr;
  outputs Q;
  reg Q;
  always @(negedge clk or posedge clk)
  Q= S | (R' & ~ Q)
endmodule
```

With neat logic diagram and truth table, explain the working of JK master slave flip flop.

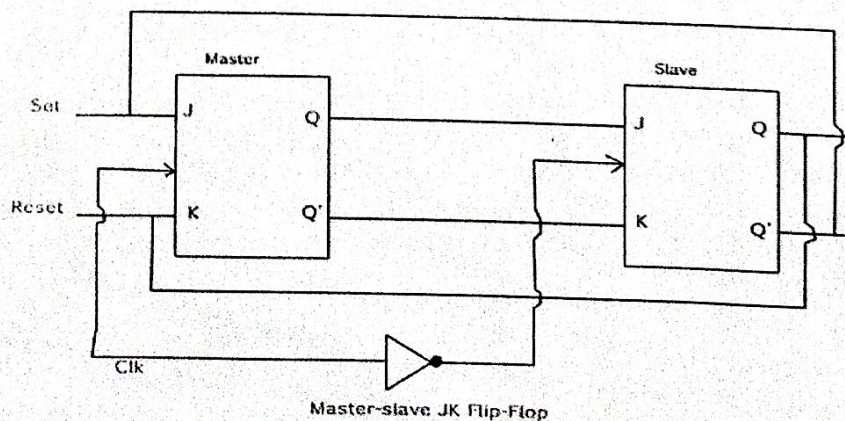
6

CO4

L2

2M

The Master-Slave Flip-Flop is basically a combination of two JK flip-flops connected together in a series configuration. Out of these, one acts as the "master" and the other as a "slave". The output from the master flip flop is connected to the two inputs of the slave flip flop whose output is fed back to inputs of the master flip flop. In addition to these two flip-flops, the circuit also includes an inverter. The inverter is connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip-flop. I



1M

Working of a master slave flip flop –

1. When the clock pulse goes to 1, the slave is isolated; J and K inputs may affect the state of the system. The slave flip-flop is isolated until the CP goes to 0. When the CP goes back to 0, information is passed from the master flip-flop to the slave and output is obtained.
2. Firstly the master flip flop is positive level triggered and the slave flip flop is negative level triggered, so the master responds before the slave.
3. If J=0 and K=1, the high Q' output of the master goes to the K input of the slave and the clock forces the slave to reset, thus the slave copies the master.
4. If J=1 and K=0, the high Q output of the master goes to the J input of the slave and the Negative transition of the clock sets the slave, copying the master.
5. If J=1 and K=1, it toggles on the positive transition of the clock and thus the slave toggles on the negative transition of the clock.
6. If J=0 and K=0, the flip flop is disabled and Q remains unchanged.

2M

Truth table

J	K	Q	Q'	Description
0	0	0	0	No change
0	0	0	1	
0	1	1	0	Reset Q=0
0	1	0	1	
1	0	0	1	Set Q=1
1	0	1	0	
1	1	0	1	Toggle
1	1	1	0	

1M

c Distinguish between PLA and PAL.

4

CO3

L4

PLA	PAL
PLA has both AND gate plane and OR gate planes are fusible links.	PAL has only AND gate plane is fixed and OR gate planes is fusible links.
Less flexibility in logic circuit function implementation.	More flexibility in logic circuit function implementation.
It is difficult to manufacture.	Simple to manufacture.
PLA reduced speed performance	PAL has good speed performance.
The PLA devices are manufacture in larger size	PAL devices are manufactured in smaller size.

3 a List the different types of shift registers. With an example explain 4 bit Serial In Serial Out (SISO) register using negative edge triggered D flip flop.

5

CO4

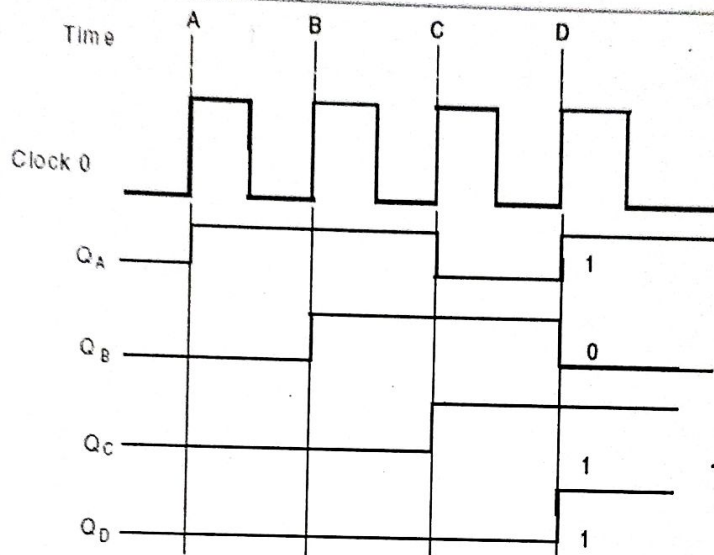
L2

The different types of shift registers are Serial In Serial Out, Serial In Parallel Out, Parallel In Serial Out, Parallel In Parallel Out.
Serial shift registers can be implemented using any type of flip flops. A serial shift register implemented using D flip-flops with the serial data applied at the D input of the first flip flop and serial data out obtained at the Q output of the last flip-flop. At each clock transition 1 bit of serial data is shifted in and at the same instant 1 bit of serial data is shifted out. For a 4-bit shift register, 8 clock transitions are required to shift in 4-bit data and completely shift out the 4-bit data.

2M

Example:

Timing pulse	Q_A	Q_B	Q_C	Q_D	Serial output at Q_D
Initial value	0	0	0	0	0
After 1 st clock pulse	1	0	0	0	0
After 2 nd clock pulse	1	1	0	0	0
After 3 rd clock pulse	0	1	1	0	0
After 4 th clock pulse	1	0	1	1	1

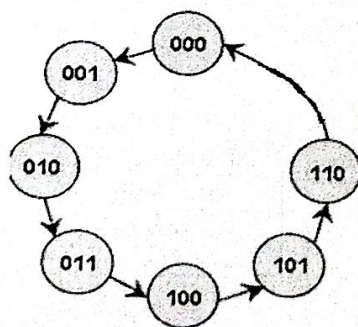


2M

1M

b Design Synchronous MOD-7 JK flip flop counter using synthesization along with the timing diagram

6 CO4 L6



Present State			Next State								
Q_c	Q_b	Q_a	Q_{c+1}	Q_{b+1}	Q_{a+1}	J_c	K_c	J_b	K_b	J_a	K_a
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	x	x	x	X	X	X	X	X	X

	$Q_b^1 Q_a^1$	$Q_b^1 Q_a$	$Q_b Q_a$	$Q_b Q_a^1$
Q_c^1	0	0	1	0
Q_c	X	X	X	X

$J_c = Q_b Q_a$

	$Q_b^1 Q_a^1$	$Q_b^1 Q_a$	$Q_b Q_a$	$Q_b Q_a^1$
Q_c^1	X	X	X	X
Q_c	0	0	X	1

$K_c = Q_b$

	$Q_b^1 Q_a^1$	$Q_b^1 Q_a$	$Q_b Q_a$	$Q_b Q_a^1$
Q_c^1	0	1	1	X
Q_c	0	1	X	X

$J_b = Q_a$

	$Q_b^1 Q_a^1$	$Q_b^1 Q_a$	$Q_b Q_a$	$Q_b Q_a^1$
Q_c^1	X	X	1	0
Q_c	X	X	X	1

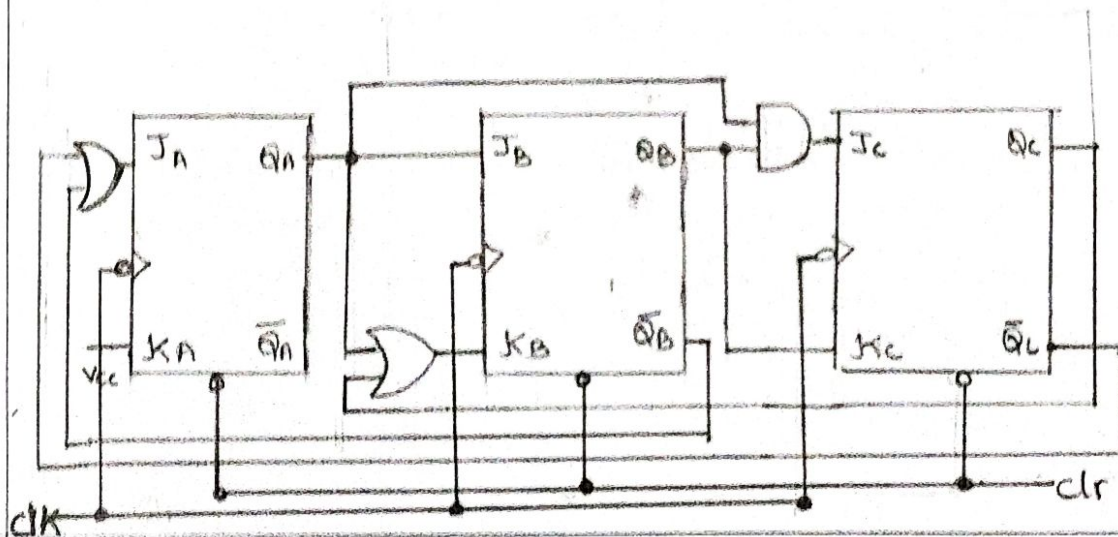
$K_b = Q_a + Q_c$

	$Q_b^1 Q_a^1$	$Q_b^1 Q_a$	$Q_b Q_a$	$Q_b Q_a^1$
Q_c^1	1	X	X	1
Q_c	1	X	X	0

$J_A = Q_c^1 + Q_b^1$

	$Q_b^1 Q_a^1$	$Q_b^1 Q_a$	$Q_b Q_a$	$Q_b Q_a^1$
Q_c^1	X	1	1	X
Q_c	X	1	X	X

$K_a = 1$



c Distinguish between combinational circuit and sequential circuit.

4 CO4 L4

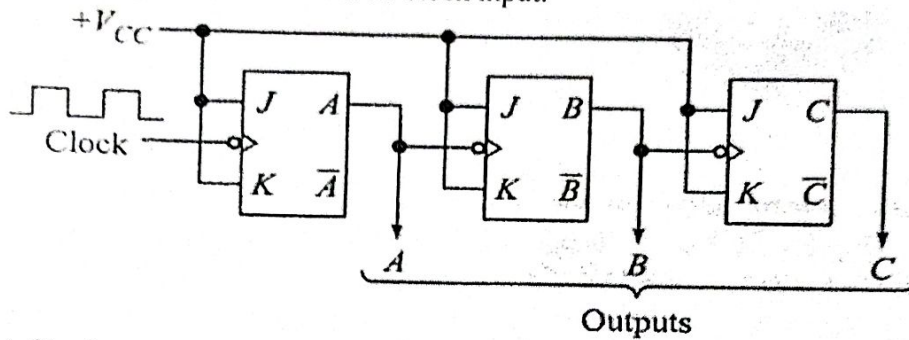
Combinational Circuit	Sequential circuit
The digital logic circuit whose outputs can be determined using the logic function of the current state inputs	The digital logic circuits whose outputs can be determined using the logic function of the current state inputs and past state inputs as well.
This circuit doesn't have the capability to store a state inside them.	This circuit is capable to retain the earlier state of the system based on the current inputs and earlier states.
The combinational circuit doesn't contain any memory element.	The sequential circuit contains memory elements which are capable of storing data in a digital circuit.
These circuits are independent of the clock	These circuits use a clock for triggering the flip-flops.
The combinational circuits don't require any feedbacks.	The sequential circuits utilize the feedback from the outputs to inputs.

4M

4 a Explain 3 bit binary Ripple up counter with its block diagram, truth table and output waveform.

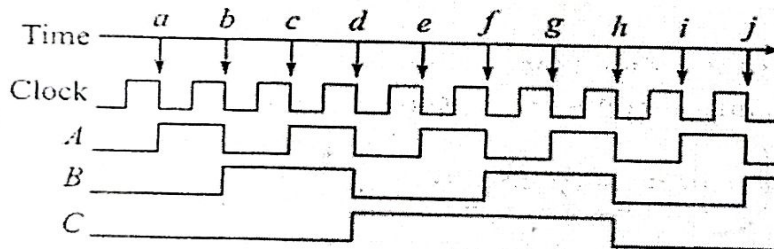
5 CO4 L2

A binary ripple counter can be constructed using clocked JK flip-flops. Figure shows three negative edge-triggered, JK flip-flops connected in cascade. The system clock, a square wave, drives flip-flop A. The output of A drives B, and the output of B drives flip-flop C. All the J and K inputs are tied to $+V_{cc}$. This means that each flip-flop will change state (toggle) with a negative transition at its clock input.



The A flip-flop must change state before it can trigger the B flip-flop, and the B flip-flop has to change state before it can trigger the C flip-flop. The triggers move through the flip-flops like a ripple in water. Because of this, the overall propagation delay time is the sum of the individual delays.

Timing Diagram

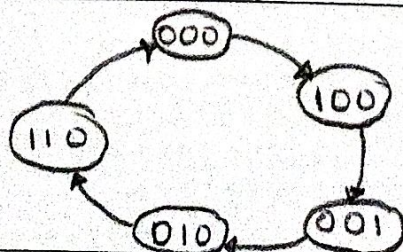


Truth Table

Negative clock	C	B	A	Count
--	0	0	0	0
a	0	0	1	1
b	0	1	0	2
c	0	1	1	3
d	1	0	0	4
e	1	0	1	5
f	1	1	0	6
g	1	1	1	7
h	0	0	0	0

b Design Asynchronous counter for the sequences 0--> 4--> 1--> 2--> 6--> 0, using D flip flop.

6 CO4 L6



Present State			Next State					
Q_c	Q_b	Q_a	Q_{c+1}	Q_{b+1}	Q_{a+1}	D_c	D_b	D_a
0	0	0	1	0	0	1	0	0
0	0	1	0	1	0	0	1	0
0	1	0	1	1	0	1	1	0
0	1	1	X	X	X	X	X	X
1	0	0	0	0	1	0	0	1
1	0	1	X	X	X	X	X	X
1	1	0	0	0	0	0	0	0
1	1	1	X	X	X	X	X	X

	$Q_b^1 Q_a^1$	$Q_b^1 Q_a$	$Q_b Q_a$	$Q_b Q_a^1$
Q_c^1	1	0	X	1
Q_c	0	X	X	0

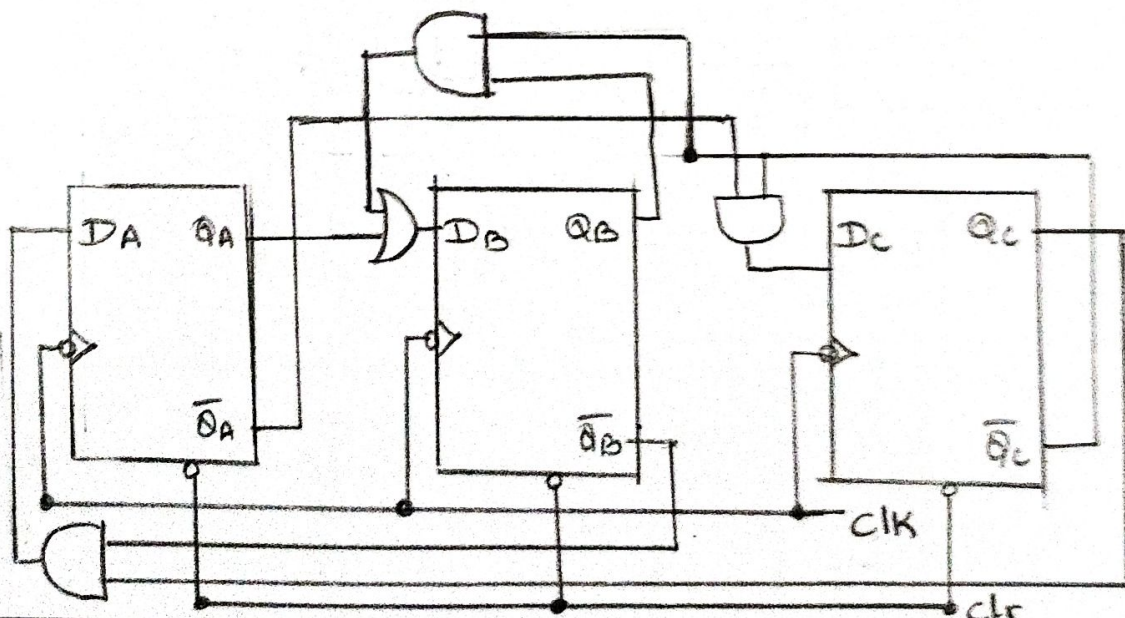
$$D_c = Q_c^1 Q_a^1$$

	$Q_b^1 Q_a^1$	$Q_b^1 Q_a$	$Q_b Q_a$	$Q_b Q_a^1$
Q_c^1	0	1	X	1
Q_c	0	X	X	0

$$D_b = Q_a^1 + Q_c^1 Q_b$$

	$Q_b^1 Q_a^1$	$Q_b^1 Q_a$	$Q_b Q_a$	$Q_b Q_a^1$
Q_c^1	0	0	X	0
Q_c	1	X	X	0

$$D_a = Q_c Q_b^1$$



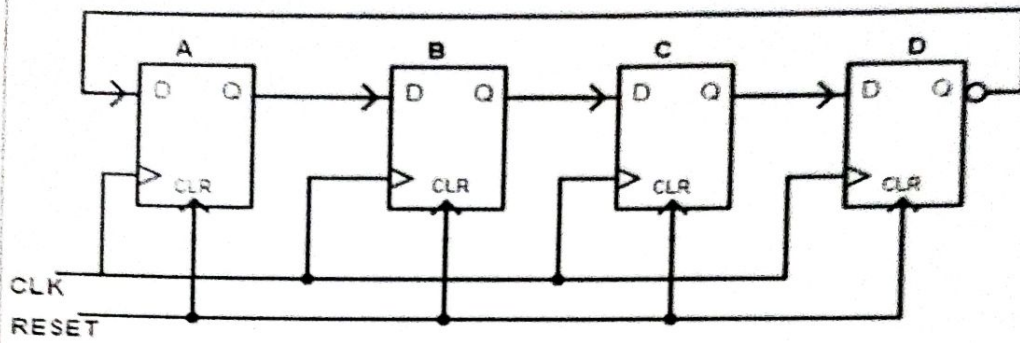
c Explain Ring counter and Johnson counter.

4 CO4 L2

Ring Counter

The ring counter is a cascaded connection of flip flops, in which the output of last flip flop is connected to input of first flip flop. In ring counter if the output of any stage is 1, then its remainder is 0. The Ring counters transfers the same output throughout the circuit. That means if the output of the first flip flop is 1, then this is transferred to its next stage i.e. 2nd flip flop. By transferring the output to its next stage, the output of first flip flop becomes 0. And this process continues for all the stages of a ring counter.

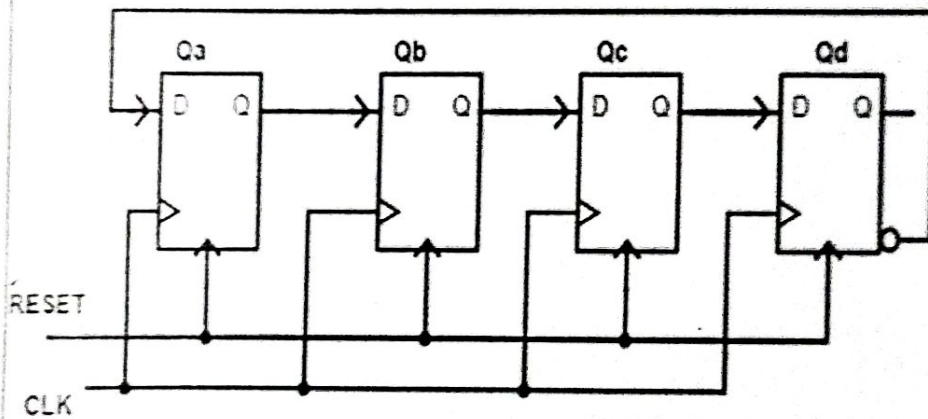
2M



Johnson Counter

The Johnson counter is a modification of ring counter. In this the inverted output of the last stage flip flop is connected to the input of first flip flop. If we use n flip flops to design the Johnson counter, it is known as $2n$ bit Johnson counter or Mod $2n$ Johnson counter. This is an advantage of the Johnson counter that it requires only half number of flip flops that of a ring counter uses, to design the same Mod. The Johnson counter is also known as Twisted Ring Counter.

2M



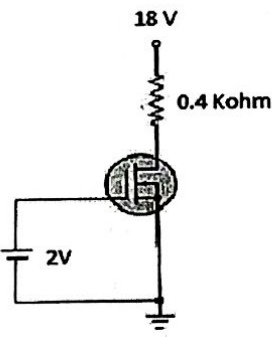
Vasudev. S
Shilpa
Name & Signature of the Faculty

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Signature of HOD

Semester: 3-CBCS 2017
Subject: ANALOG AND DIGITAL ELECTRONICS(17CS32)
Faculty: Ms Shilpa & Mr. Vasudev S Shahapur

Date: 26 Nov 2018
Time: 03:00 PM - 04:30 PM
Max Marks: 30

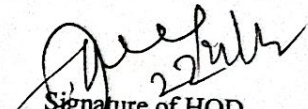
Answer any 2 question(s)

Q.No		Marks	CO	BT/CL
1	a	5	CO5	L2
	b	6	CO1	L2
	c	4	CO1	L1
OR				
2	a	5	CO5	L2
	b	6	CO1	L2
	c	4	CO1	L3
Figure (a), shows a biasing configuration using DE-MOSFET. Given the saturation drain current is 8mA and the pinchoff voltage is -2V, determine the value of drain source volatge, drain current. 				
3	a	5	CO5	L2
	b	6	CO1	L2
	c	4	CO1	L1
OR				

4	a	Explain successive approximation converter with its block diagram. Give example for 4 bits.	5	CO5	L2
	b	Explain with schematics operation of relaxation oscillator with relevant waveforms.	6	CO1	L2
	c	What are active filters? Explain first order low pass active filters.	4	CO1	L2

 Vasudev. S.
 Shilpa
 Signature of Faculty


 Signature of IQAC


 Signature of HOD

Semester: 3-CBCS 2017

Subject: ANALOG AND DIGITAL ELECTRONICS(17CS32)

Faculty: Ms. Shilpa

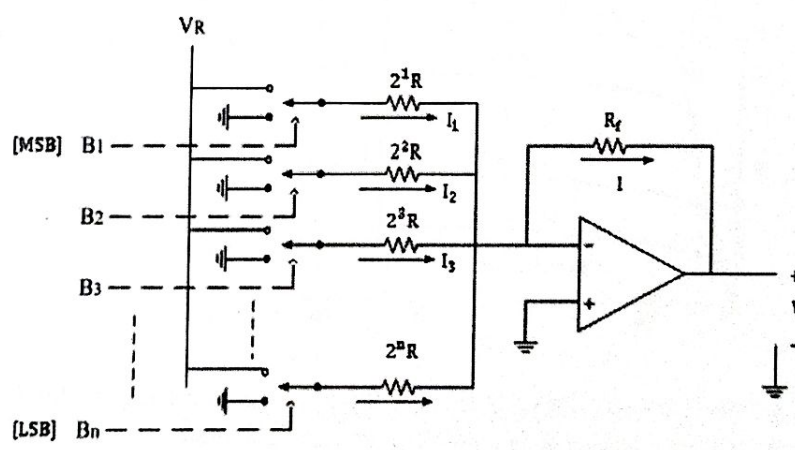
Mr. Vasudev S Shahapur

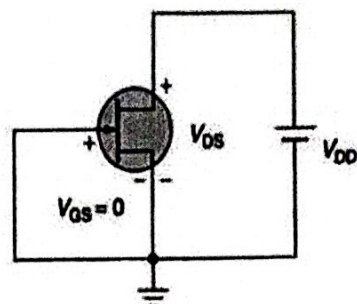
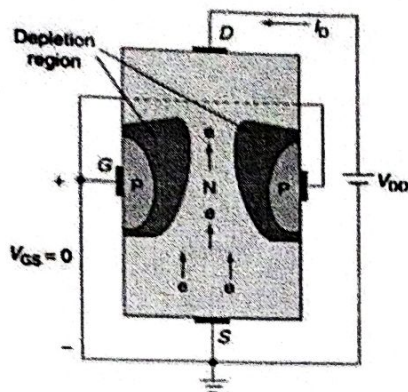
Date: 26 NOV 2018

Time:03:00PM-04:30PM

Max Marks:30

Answer any 2 question(s)

Q.No		Marks	CO	BT/CL
1 a	Explain binary weighted resistor D/A converter. Mention its drawback. The value assigned to each bit in a digital number, expressed as a fraction of the total. The values are assigned in binary fashion according to sequence 1,2,4,8, ... ,2ⁿ (n = total no. of bits). Assume we want to convert a 3-bit digital input into an analog output. The smallest number represented is 000; let us make this equal to 0V. The largest number is 111; let us make this equal to +7V. Between 000 and 111, there are 7 discrete levels to be defined. Therefore, the analog signal can be divided into 7 levels. The smallest incremental change in digital signal is represented by LSB=20. In general, the binary equivalent weight assigned to the LSB is given by $\text{LSB weight} = \frac{1}{(2^n - 1)}$ where n = number of bits. The remaining weights are found by multiplying by 2, 4, 8, and so on.  Drawbacks • When number of binary input increases, it is not easy to maintain the resistance ratio. • Very wide ranges of different values of resistors are required. For high accuracy of conversion, the values of resistances must be accurate. • Different current flows through resistors, so their wattage ratings are also different.	3+1+1	CO5	L2
1 b	Explain the operation and characteristics of N-Channel JFET. Principal of Operation: The operation of JFET is studied by applying external potential to the terminals. Here gate-source terminals are act as input terminal and drain-source terminals act as output terminal to the JFET.	2+2+2	CO1	L2



Case $V_{GS}=0$ Volts: Shorting gate & source terminals we get $V_{GS}=0$ Volts. When a positive bias is applied at drain-source terminals (V_{DS}) both P-N junction will become reverse biased. By increasing V_{DS} , electrons in N-channel are attracted by drain terminal establishing flow of drain current (I_D).

Case $V_{GS}=-ve$ Volts: When a negative bias is applied to the gate terminal, there is an increase in the width of depletion layer. Therefore, for lower values of V_{DS} pinch-off condition occurs. Also the saturation drain current decreases. As the value of V_{GS} becomes more negative, I_D becomes lesser. When V_{GS} equals to $-V_P$, I_D becomes zero which is referred to as gate-source cut-off voltage ($V_{GS(OFF)}$).

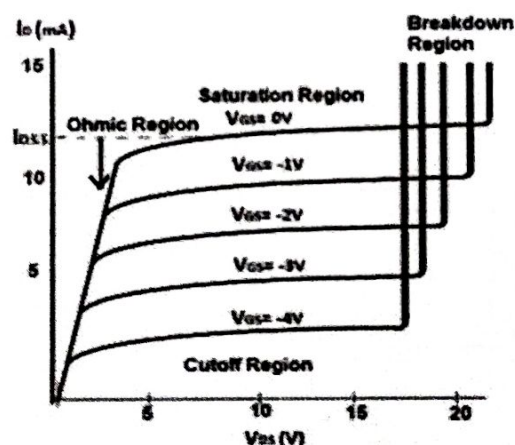


Figure shows the output characteristics of N-channel JFET. In the ohmic region, JFET acts as variable resistor whose resistance is controlled by V_{GS} . The drain resistance (r_d) is given by,

$$r_d = \frac{r_0}{(1 - V_{GS}/V_P)^2}$$

Where r_0 is the resistance when $V_{GS}=0$.

The relation between input voltage V_{GS} and output current I_D is given by the Shockley's equation, $I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$

JFET	MOSFET
JFETs operate in depletion mode only	MOSFETs operate in both depletion & enhancement mode.
Higher drain resistance between $100\text{K}\Omega$ to $1\text{M}\Omega$	Lesser drain resistance between 1 to $50\text{K}\Omega$
Characteristic curves are more flat	Characteristic curves are less flat
Leakage gate current is high	Leakage gate current is less
5 Input impedance is near $10^9 \Omega$	Input impedance is high near $10^{13} \Omega$

OR

2a

What is binary ladder? Explain the binary ladder with digital input 1000.

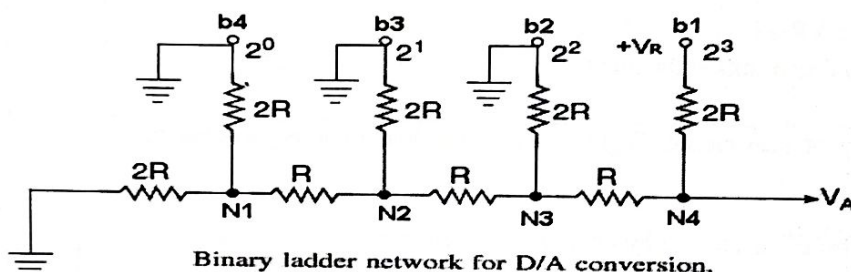
2+2+1

CO5

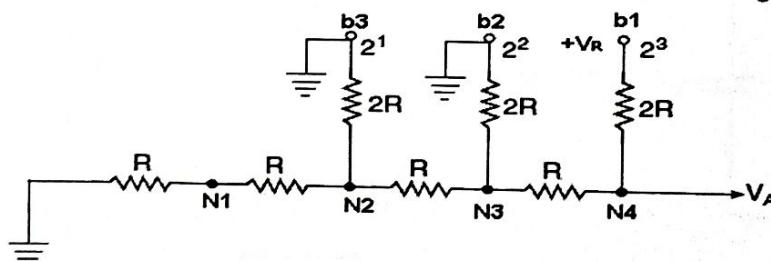
L2

The binary ladder is a resistive network whose output voltage is a properly weighted sum of the digital inputs.

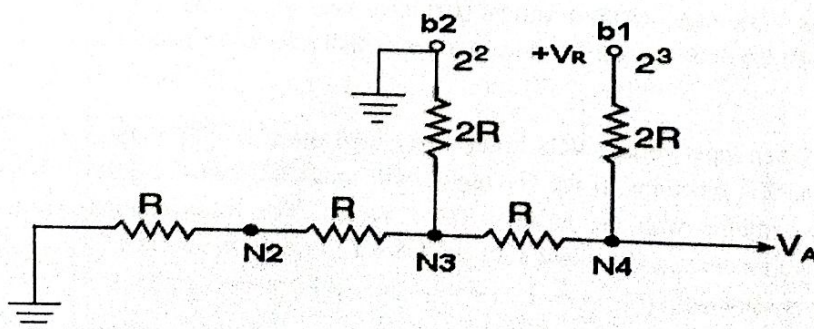
In ladder circuit the output voltage is also weighted sum of the corresponding digital input. Consider the example 1000 the circuit will be as shown below



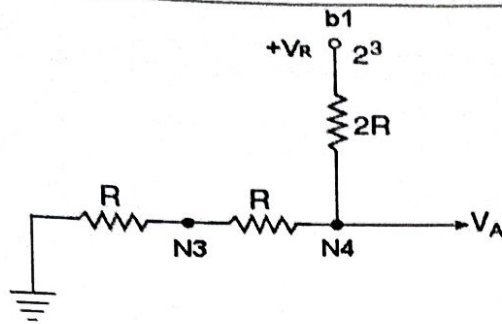
Now see at node1 (N1) resistor 2R connecting in b4 parallel with resistor 2R. And those 2R parallel 2R resistors make equivalent register of R shown in bellow diagram.



Now for N2 same thing happen B3 series with 2R and parallel with R + R resistors. It will also make equivalent resistor R at N3.



Repeating the same process we got equivalent of R resistor at N4.



Now at N4, if we calculate the output analog equivalent voltage then we will get

$$V_A = \frac{V_R \cdot 2R}{(R+R+2R)} \\ = V_R/2$$

Thus when bit 1000 the output is $V_R/2$. Similarly it can be found that using above process for bit 0100 the output will be $V_R/4$, for bit 0010 output will be $V_R/8$ and for bit 0001 output will be $V_R/16$.

By using superposition theorem we can find in any n-bit ladder network the output voltage will be

$$V_A = V_R/2^1 + V_R/2^2 + V_R/2^3 + \dots + V_R/2^n$$

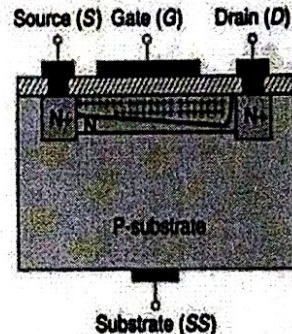
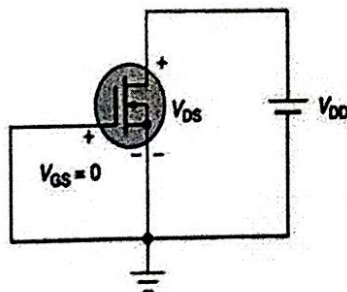
Where n is the total number of bits at the input.

D

2 b

Explain with the help of neat circuit diagram and characteristic curves working of N-channel De MOSFET

Operation of DE-MOSFET is studied by applying different biases at input like $V_{GS}=0$, $V_{GS}=+/-ve$ Volts.



Case $V_{GS}=0$ Volts: When input gate voltage (V_{GS}) is zero that is gate-source terminals are shorted and a positive voltage is applied between source-drain terminals (V_{DS}), electrons are attracted by positive polarity of drain due to which flow of current in the N-channel is observed. As V_{DS} increases drain current (I_D) increases. When V_{DS} reaches to pinch-off voltage (V_P) the drain current becomes constant which referred as saturation drain current (I_{DSS})

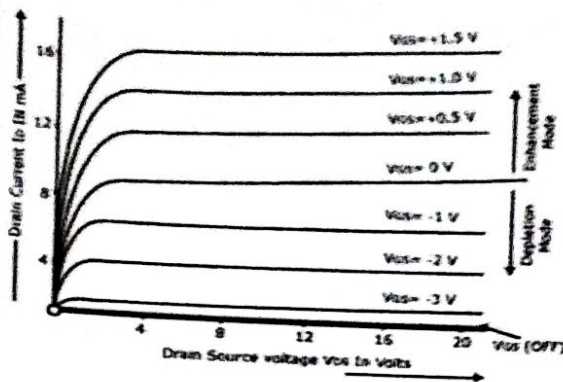
Case $V_{GS}=-ve$ Volts: When input voltage V_{GS} is negative biased and a positive V_{DS} is applied to the DE-MOSFET, electrons in the N^+ region will move towards P region. These electrons will recombine with the holes in the P region. The recombination phenomenon increases with more negative input voltage V_{GS} which results in decrease in the flow of current between drain-source.

Case $V_{GS}=+ve$ Volts: When input voltage V_{GS} is positive biased and a positive V_{DS} is applied to the DE-MOSFET, minority carriers (electrons) in the P region will move towards N^+ region of drain. These electrons in the source terminal will move towards drain terminal through the N-channel. Output drain current (I_D) increases with increase in

1

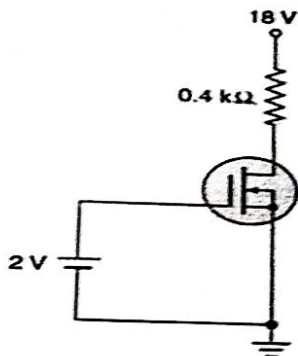
the positive input voltage V_{GS} .

Figure shows the output characteristics of N-channel DE-MOSFET.



2 c

Figure (a), shows a biasing configuration using DE-MOSFET. Given the saturation drain current is 8mA and the pinchoff voltage is -2V, determine the value of drain source voltage, drain current.



Given that, $I_{DSS}=8\text{mA}$, $V_{GS}=2\text{V}$, applied input bias (V_{GG})= 2V and $V_P=-2\text{V}$. $V_{GS}=?$, $I_D=?$ and $V_{DS}=?$

When input current ($I_G=0$) is zero $V_{GS} = 2\text{V}$

We know that, drain current is given by,

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

Substituting all values we get,

$$I_D = 8 \times 10^{-3} \times (1 - (2/(-2)))^2 = 32 \times 10^{-3}$$

$$I_D = 32\text{mA}$$

Applying KVL

$$V_{CC} - I_D R_D - V_{DS} = 0$$

Substituting all values we get,

$$18 - 32 \times 10^{-3} \times 0.4 \times 10^3 - V_{DS} = 0$$

$$V_{DS} = 18 - 12.8$$

$$V_{DS} = 5.2\text{V}$$

2+2

CO1

L3

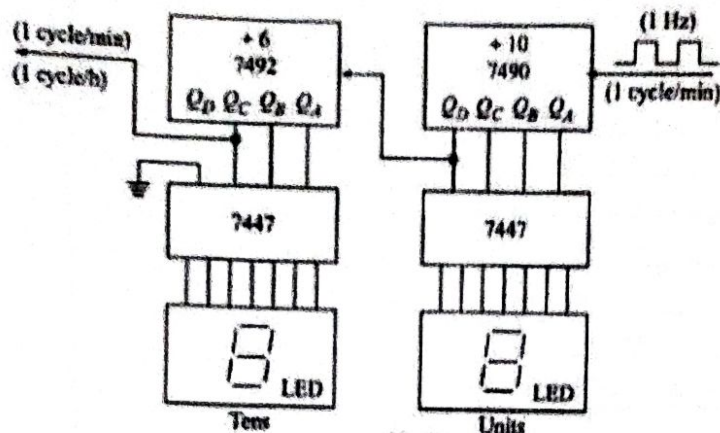
Explain digital clock with its block diagram.

3 a

2+3

CO5

L2



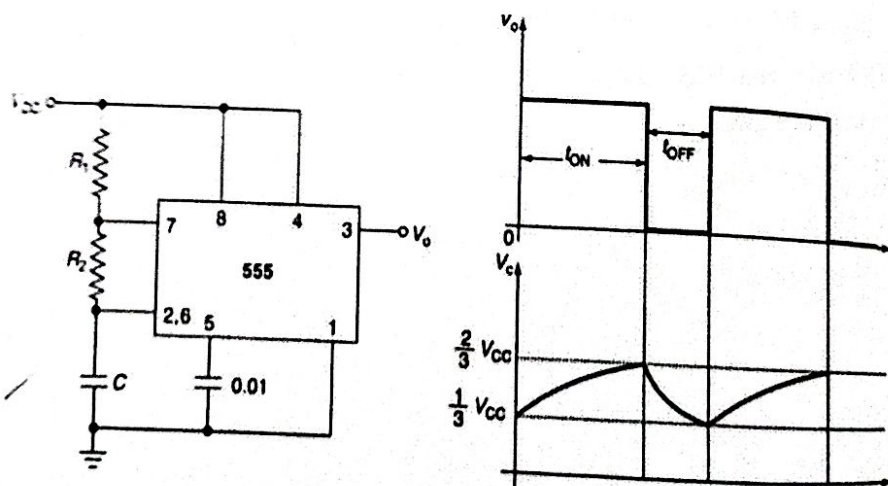
7490 decade counter can be used as a divide-by-10 counter and the 7492 can be used as a divide-by-6 counter. Cascading these two counters will provide a divide-by-60 counter. The amplifier at the input provides a 60Hz square wave of the proper amplitude to drive the 7490. The 7492 is connected as a divide-by-12 counter, but only outputs QA, QB & QC are used. In this fashion, the 7492 operates essentially as a divide-by-6 counter. For decoding 'seconds counter' to represent each of the 60s in 1min, we construct a mod-10 counter in series with a mod-6 counter.

The mod-10 counter can then be decoded to represent the units digit of seconds, and the mod-6 counter can be decoded to represent the tens digits of seconds. Since both the 7490 & 7492 count in the straight 8421, a 7447 decoder-driver can be used with each to drive two 7-segment indicators.

3 b

With the block diagram, explain the operation of a Astable multivibrator using IC555 timer.

Figure shows the circuit diagram of IC 555 timer as astable multivibrator and the output waveform with charging and discharging capacitor (C).



Principal of operation:

Assume initially Output is HIGH state, Capacitor voltage is zero due to complete discharge and therefore no current flows through the IC. When we observe the astable circuit with these assumptions, we find that the current from applied power supply (+VCC) is going to flow through R1, R2 and Capacitor (C) to reach the ground terminal. Due to current flow in the capacitor (C), capacitor voltage (VC) goes on increases. When the capacitor voltage reaches $\frac{2}{3}$ value of VCC ($V_C = \frac{2}{3} V_{CC}$), output goes to LOW

2+2
+2

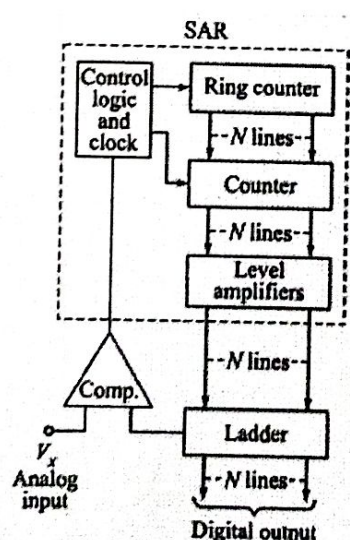
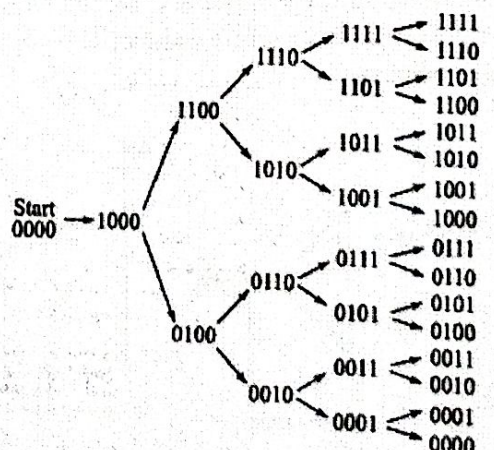
CO1

L2

	state. When output is LOW, all the current from power supply flow through the IC and capacitor start discharging, hence capacitor voltage decreases. When the capacitor voltage decreases to $\frac{1}{3}$ value of V_{CC} ($V_C = \frac{1}{3} V_{CC}$), output goes to HIGH state. This phenomenon will be continued for charging and discharging of capacitor (C) to asatble the output between HIGH & LOW states. Timing period (T) of astable states are given by, HIGH state period = $t_{ON} = 0.69 \times (R_1 + R_2)C$ LOW state period = $t_{OFF} = 0.69 \times R_2C$ Therefore total time period and frequency of output waveform is given by, Time period = $T = t_{ON} + t_{OFF} = 0.69 \times (R_1 + 2R_2)C$ Frequency = $F = 1/T = 1/(0.69 \times (R_1 + 2R_2)C)$			
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3 c	Define the following terms. i) CMRR Common mode rejection ratio (CMRR) is defined as the ratio of the desired differential gain (A_d) to the undesired common mode gain (A_c). ii) Slew rate Slew rate is defined as the rate of change of output voltage with time. Slew rate limits the high frequency bandwidth. iii) PSRR Power supply rejection ratio (PSRR) is defined as the ratio of change in the power supply voltage to the corresponding change in the output voltage iv) Open-loop gain. Open-loop gain is the ratio of amplifier gain (A) to the differential gain (A_d) without feedback. It is also defined as ratio of single ended output to the differential input.	1+1+ 1+1	CO1	L1
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OR

4 a	Explain successive approximation converter with its block diagram. Give example for 4 bits. If multiplexing is required, the successive-approximation converter is most useful. The block diagram for this type of converter is as shown below.  (a)  (b)	1+2 +2	CO5	L2
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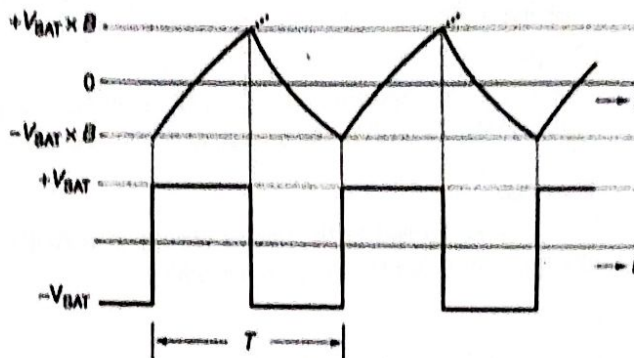
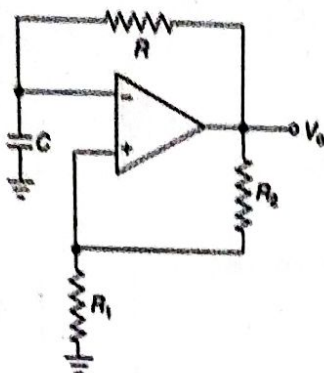
The converter operates by successively dividing the voltage ranges in half. The counter is first reset to all 0s, and the MSB is then set. The MSB is then left in or taken out (by resetting the MSB flip-flop) depending on the output of the comparator. Then the second MSB is set in, and a

comparison is made to determine whether to reset the second MSD flip-flop. The process is repeated down to the LSD, and at this time the desired number is in the counter. Since the conversion involves operating on one flip-flop at a time, beginning with the MSD, a ring counter may be used for flip-flop selection. The successive-approximation method thus is the process of approximating the analog voltage by trying 1 bit at a time beginning with the MSD.

4 b

Explain with schematics operation of relaxation oscillator with relevant waveforms.

Relaxation oscillator is a circuit which produces non-sinusoidal waves at output whose time period is dependent on the charging time of capacitor used in the circuit. Figure 1.43 shows circuit connection of the relaxation oscillator using opamp with waveforms.



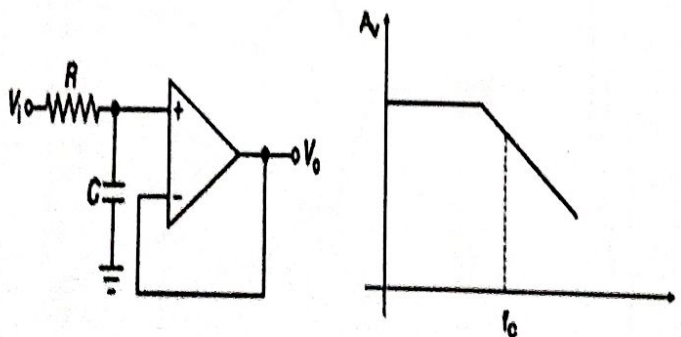
Operation: Let us assume that, Initially output is HIGH state, Voltage at non-inverting terminal is $+V_P = +V_{SAT} \times R_1 / (R_1 + R_2)$ and Capacitor voltage is zero due to complete discharge. These conditions will force the output to stay in HIGH state. Now, Capacitor (C) starts charging towards $+V_{SAT}$ through resistor (R). The moment the capacitor voltage exceeds the voltage $+V_P$, output switches to LOW state. Now, voltage at non-inverting terminal is $-V_P = -V_{SAT} \times R_1 / (R_1 + R_2)$. It results in discharging of capacitor towards $-V_{SAT}$. As soon as capacitor voltage less than the $-V_P$, output switches back to HIGH state. This phenomenon will be continued to get rectangular waves at the output due to charging and discharging of capacitor.

4 c

What are active filters? Explain first order low pass active filters.

Active filters are the electronic circuits which are used to suppress or remove unwanted frequency signals which are above or below the selected (cut-off) frequency.

First order filters are designed using single R-C section with opamp. Figure shows the circuit diagram of first order low-pass filter, where resistor (R) is connected in between input signal and non-inverting terminal of opamp.



Operation of filter is depending on the operation of the capacitor (C). The capacitive reactance is given by, $X_C = 1 / 2\pi f C$. Above equation clears that capacitive reactance (resistance of capacitor) is indirectly proportional to frequency of the input signal. For low frequencies, capacitive reactance is high and for high frequencies it is low. The cut-off frequency is given by, $f_c = 1 / 2\pi R C$.

2+2

+2

CO1

L2

4

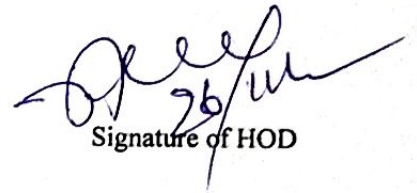
CO1

L2

	When the frequency of input signal is less than the cut-off frequency capacitor shows high reactance. Therefore output of the opamp is equal to the input. When the frequency of input signal is more than the cut-off frequency capacitor shows low reactance. Therefore output of the opamp is equal to zero.			
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Signature of faculty



Signature of HOD



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I Internal Assessment Test- Attendance

Subject Code:	Subject Name:	Date:
17CS32	Analog and Digital Electronics	17/9/2018

III Semester CSE A-Section

S. No	USN	Name of the Student	Signature of the Student
1.	4AL15CS050	Kiran A S	
2.	4AL16CS047	Madushree R	
3.	4AL16CS078	Harshith S	
4.	4AL16CS114	THOKCHOM SANJIT	
5.	4AL17CS002	Ajeyashree K	
6.	4AL17CS003	Akshat Khandelwal	
7.	4AL17CS004	Akshata Narayana Hegde	
8.	4AL17CS005	Amrutha M	
9.	4AL17CS006	Anilkumar B N	
10.	4AL17CS007	Anusha	
11.	4AL17CS008	Anvitha Poojary	
12.	4AL17CS009	Anvitha U	
13.	4AL17CS010	Apeksha Rajendra Rane	
14.	4AL17CS011	Apoorva H P	
15.	4AL17CS012	Apoorva K N	
16.	4AL17CS013	Aruna K	
17.	4AL17CS015	Asha Rudrappa Totagi	
18.	4AL17CS016	Ashika	
19.	4AL17CS017	Ashwini	
20.	4AL17CS018	Ashwini Shekarappa Jadamali	
21.	4AL17CS019	Bhramari P Shetty	
22.	4AL17CS020	Chandana Patil	
23.	4AL17CS021	Chetana H	
24.	4AL17CS022	Chethana J	
25.	4AL17CS024	D Jasmine Joyline	
26.	4AL17CS025	Datta Kiran A B	
27.	4AL17CS027	Dhanya Bhat	
28.	4AL17CS028	Dheeraj Krishna Devadig	



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29.	4AL17CS029	Dsouza Elston Ronald	<i>Elston</i>
30.	4AL17CS030	Gayatri V Kamat	<i>Kamat</i>
31.	4AL17CS031	Gowda Roshni Shivprakash	<i>Roshni</i>
32.	4AL17CS032	Harshith C P	<i>Harshith</i>
33.	4AL17CS033	Hemalatha S	<i>Hemalatha</i>
34.	4AL17CS034	Jagath Haren	<i>Jagath Haren</i>
35.	4AL17CS035	Jayalakshmi M	<i>J. M. L.</i>
36.	4AL17CS036	Jayraj ChiragKumar shah	<i>J. Chirag</i>
37.	4AL17CS037	John Alsten Tauro	<i>Tauro</i>
38.	4AL17CS038	K Thrishul	<i>Thrishul</i>
39.	4AL17CS039	Kanaka B S	<i>Kanaka</i>
40.	4AL17CS040	Kavana V	<i>Kavana V.</i>
41.	4AL17CS041	Kavya	<i>Kavya</i>
42.	4AL17CS042	Kavya R Shetty	<i>Kavya</i>
43.	4AL17CS044	Koushik S N	<i>K. S. N.</i>
44.	4AL17CS045	Lathik Moger	<i>Lathik</i>
45.	4AL17CS046	Likitha M	<i>Likitha</i>
46.	4AL17CS047	M C Suchithra Heggade	<i>M. C. Suchithra</i>
47.	4AL17CS048	Madan G Gudigar	<i>Madan G. Gudigar</i>
48.	4AL17CS049	Madan Gowda V	<i>Madan Gowda V.</i>
49.	4AL17CS050	Mhaske Pooja Sambhaji	<i>Pooja</i>
50.	4AL17CS051	Mahek Sabha	<i>Mahek</i>
51.	4AL17CS052	Nagashree Arun M	<i>Nagall</i>
52.	4AL17CS053	Naik Nayana Ganapati	<i>Naik</i>
53.	4AL17CS054	Nanditha R Shetty	<i>Nanditha</i>
54.	4AL17CS055	Netra Suresh Gudagamnala	<i>Netra</i>
55.	4AL17CS056	Pallavi	<i>Pallavi</i>
56.	4AL17CS057	Pavana P	<i>Pavana</i>
57.	4AL17CS059	Prajna	<i>Prajna</i>
58.	4AL17CS096	Soundarya R	<i>Soundarya</i>
59.	4AL17CS097	Spoorthi M S	<i>Spoorthi</i>
60.	4AL17CS098	Spoorthi Balaji	<i>Spoorthi</i>
61.	4GW17CS050	Niriksha A	<i>Niriksha</i>

15/10/18

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DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
Academic Year 2018-19

II Internal Assessment Test- Attendance

Subject Code:	Subject Name:	Date:
17CS32	Analog and Digital Electronics	25/10/18

III Semester CSE A-Section

S. No	USN	Name of the Student	Signature of the Student
1.	4AL15CS050	Kiran A S	Kiran A S
2.	4AL16CS047	Madushree R	Madhu Shree R
3.	4AL16CS078	Harshith S	- ABSENT -
4.	4AL16CS114	THOKCHOM SANJIT	Thokchom Sanjit
5.	4AL17CS002	Ajeyashree K	Ajeyashree K
6.	4AL17CS003	Akshat Khandelwal	Akshat
7.	4AL17CS004	Akshata Narayana Hegde	Akshata
8.	4AL17CS005	Amrutha M	Amrutha M
9.	4AL17CS006	Anilkumar B N	- ABSENT -
10.	4AL17CS007	Anusha	Anusha
11.	4AL17CS008	Anvitha Poojary	Anvitha
12.	4AL17CS009	Anvitha U	Anvitha U
13.	4AL17CS010	Apeksha Rajendra Rane	Apeksha
14.	4AL17CS011	Apoorva H P	Apoorva H P
15.	4AL17CS012	Apoorva K N	Apoorva K N
16.	4AL17CS013	Aruna K	Aruna K
17.	4AL17CS015	Asha Rudrappa Totagi	Asha
18.	4AL17CS016	Ashika	Ashika
19.	4AL17CS017	Ashwini	Ashwini
20.	4AL17CS018	Ashwini Shekarappa Jadamali	Ashwini
21.	4AL17CS019	Bhramari P Shetty	Bhramari
22.	4AL17CS020	Chandana Patil	Chandana
23.	4AL17CS021	Chetana H	Chetana
24.	4AL17CS022	Chethana J	Chethana
25.	4AL17CS024	D Jasmine Joyline	Joyline
26.	4AL17CS025	Datta Kiran A B	Datta Kiran A B
27.	4AL17CS027	Dhanya Bhat	Dhanya Bhat
28.	4AL17CS028	Dheeraj Krishna Devadig	Dheeraj



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29.	4AL17CS029	Dsouza Elston Ronald	<i>Dsouza</i>
30.	4AL17CS030	Gayatri V Kamat	<i>Kamat</i>
31.	4AL17CS031	Gowda Roshni Shivprakash	<i>Roshni</i>
32.	4AL17CS032	Harshith C P	<i>Harshith</i>
33.	4AL17CS033	Hemalatha S	<i>Hemalatha S</i>
34.	4AL17CS034	Jagath Haren	<i>Jagath Haren</i>
35.	4AL17CS035	Jayalakshmi M	<i>J. M.</i>
36.	4AL17CS036	Jayraj ChiragKumar shah	<i>Jalal</i>
37.	4AL17CS037	John Alsten Tauro	<i>Tauro</i>
38.	4AL17CS038	K Thrishul	<i>Thrishul</i>
39.	4AL17CS039	Kanaka B S	<i>Kanaka B S</i>
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42.	4AL17CS042	Kavya R Shetty	<i>Kavya R Shetty</i>
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44.	4AL17CS045	Lathik Moger	<i>Lathik Moger</i>
45.	4AL17CS046	Likitha M	<i>Likitha M</i>
46.	4AL17CS047	M C Suchithra Heggade	<i>ABSENT</i>
47.	4AL17CS048	Madan G Gudigar	<i>Gudigar</i>
48.	4AL17CS049	Madan Gowda V	<i>Madan Gowda V</i>
49.	4AL17CS050	Mhaske Pooja Sambhaji	<i>Pooja</i>
50.	4AL17CS051	Mahek Sabha	<i>Mahek</i>
51.	4AL17CS052	Nagashree Arun M	<i>Nagashree</i>
52.	4AL17CS053	Naik Nayana Ganapati	<i>Naik</i>
53.	4AL17CS054	Nanditha R Shetty	<i>Nanditha R Shetty</i>
54.	4AL17CS055	Netra Suresh Gudagamnala	<i>ABSENT</i>
55.	4AL17CS056	Pallavi	<i>Pallavi</i>
56.	4AL17CS057	Pavana P	<i>Pavana</i>
57.	4AL17CS059	Prajna	<i>Prajna</i>
58.	4AL17CS096	Soundarya R	<i>Soundarya R</i>
59.	4AL17CS097	Spoorthi M S	<i>Spoorthi</i>
60.	4AL17CS098	Spoorthi Balaji	<i>Spoorthi</i>
61.	4GW17CS050	Niriksha A	<i>Niriksha A</i>

25/10/18

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III Internal Assessment Test- Attendance

Subject Code:	Subject Name:	Date:
17CS32	Analog and Digital Electronics	26/11/18

III Semester CSE A-Section

S. No	USN	Name of the Student	Signature of the Student
1.	4AL15CS050	Kiran A S	Kiran A S
2.	4AL16CS047	Madushree R	Madushree R
3.	4AL16CS078	Harshith S	Harshith S
4.	4AL16CS114	THOKCHOM SANJIT	Th. Sanjit
5.	4AL17CS002	Ajeyashree K	Ajeyashree K
6.	4AL17CS003	Akshat Khandelwal	Akshat
7.	4AL17CS004	Akshata Narayana Hegde	Akshata
8.	4AL17CS005	Amrutha M	Amrutha M
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11.	4AL17CS008	Anvitha Poojary	Anvitha
12.	4AL17CS009	Anvitha U	Anvitha U
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26.	4AL17CS025	Datta Kiran A B	Datta Kiran A B
27.	4AL17CS027	Dhanya Bhat	Dhanya Bhat
28.	4AL17CS028	Dheeraj Krishna Devadig	Dheeraj Krishna Devadig
29.	4AL17CS029	Dsouza Elston Ronald	Dsouza Elston Ronald
30.	4AL17CS030	Gayatri V Kamat	Gayatri V Kamat



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31.	4AL17CS031	Gowda Roshni Shivprakash	<i>Roshi</i>
32.	4AL17CS032	Harshith C P	<i>Harshith</i>
33.	4AL17CS033	Hemalatha S	<i>Hemalatha S</i>
34.	4AL17CS034	Jagath Haren	<i>Jagath Haren</i>
35.	4AL17CS035	Jayalakshmi M	<i>J.M.</i>
36.	4AL17CS036	Jayraj ChiragKumar shah	<i>Jshah</i>
37.	4AL17CS037	John Alsten Tauro	<i>Tatauro</i>
38.	4AL17CS038	K Thrishul	<i>Krishul</i>
39.	4AL17CS039	Kanaka B S	<i>Kanaka B.S</i>
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41.	4AL17CS041	Kavya	<i>Kavya</i>
42.	4AL17CS042	Kavya R Shetty	<i>K.R. Shetty</i>
43.	4AL17CS044	Koushik S N	<i>Koushik S.N</i>
44.	4AL17CS045	Lathik Moger	<i>Lathik Moger</i>
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46.	4AL17CS047	M C Suchithra Heggade	<i>M.C. Suchithra Heggade</i>
47.	4AL17CS048	Madan G Gudigar	<i>Madan G Gudigar</i>
48.	4AL17CS049	Madan Gowda V	<i>Madan Gowda V</i>
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60.	4AL17CS098	Spoorthi Balaji	<i>Spoorthi</i>
61.	4GW17CS050	Niriksha A	<i>Niriksha A</i>

I.A. Test Coordinator

Dept. Of Computer Science & Engineering
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Department of Computer Science and Engineering

4	a	Explain 1:8 Demultiplexer and show how 1:8 demultiplexer can be used to construct 1:16 demultiplexer.	5	3	L4
4	b	What is magnitude comparator? Construct 2-bit comparator truth table and draw logic circuit diagram for simplified outputs.	6	3	L3
4	c	Write a verilog code for Full adder circuit and Full subtractor circuit.	4	3	L3

Evaluation

USN	Name	Present (P)/ Absent (Ab)	Q1			Q2			Q3			Q4			Total Score	BT/CL
			a	b	c	a	b	c	a	b	c	a	b	c		
4AL17CS034	Jagath Haren	P	5	6	4	3	0	1	5	6	4	0	0	0	30	Apply
4AL17CS003	Akshat Khandelwal	P	5	5	3	0	0	0	5	6	4	0	0	0	28	Apply
4AL17CS007	Anusha	P	4	6	4	0	0	0	0	0	0	4	5	3	26	Apply
4AL17CS039	Kanaka B S	P	5	5	2	0	0	0	0	3	2	0	0	0	17	Apply
4AL17CS050	Mhaske Pooja Sambhaji	P	3	6	3	0	0	0	4	5	1	0	0	0	22	Apply
4AL17CS031	Gowda Roshni Shivprakash	P	3	2	4	0	0	0	2	4	1	2	0	0	16	Apply
4AL16CS114	THOKCHOM SANJIT	P	4	4	2	0	0	0	3	5	2	0	0	0	20	Apply
4AL17CS016	Ashika	P	3	3	3	0	0	0	1	5	1	0	1	0	16	Apply
4AL17CS044	Koushik S N	P	3	4	2	0	0	0	0	4	2	0	0	0	15	Apply
4AL17CS027	Dhanya Bhat	P	5	6	4	0	0	0	3	6	3	3	5	1	27	Apply
4AL17CS010	Apeksha Rajendra Rane	P	2	3	4	0	0	0	5	6	4	0	0	0	24	Apply
4AL17CS042	Kavya R Shetty	P	4	5	2	3	2	0	0	6	2	0	0	0	19	Apply
4AL17CS052	Nagashree Arun M	P	5	5	4	0	0	0	4	6	2	0	0	0	26	Apply
4AL17CS056	Pallavi	P	5	6	3	0	0	0	4	5	3	0	0	0	26	Apply
4AL17CS036	Jayraj ChiragKumar Shah	P	2	6	2	0	0	0	5	6	3	0	0	0	24	Apply
4AL17CS035	Jayalakshmi M	P	5	5	4	0	0	0	4	6	4	0	0	0	28	Apply
4AL17CS004	Akshata Narayana Hegde	P	5	6	3	0	0	0	4	6	3	0	0	0	27	Apply
4AL17CS008	Anvitha Poojary	P	5	6	4	0	0	0	4	6	3	0	0	0	28	Apply
4AL15CS050	Kiran A S	P	2	3	0	0	0	0	1	3	0	0	0	0	9	Apply
4AL17CS032	Harshith C P	P	2	3	2	0	0	0	4	5	0	0	0	0	16	Apply
4AL17CS097	Spoorthi M S	P	5	1	2	0	0	0	0	6	1	1	0	0	15	Apply
4AL17CS114	NIRIKSHA A	P	3	5	3	3	0	2	5	6	3	0	0	0	25	Apply
4AL17CS013	Aruna K	P	4	5	4	0	0	0	3	5	3	0	0	0	24	Apply

USN	Name	Present (P) Absent (Ab)	Q1			Q2			Q3			Q4			Total Score	BT/CL
			a	b	c	a	b	c	a	b	c	a	b	c		
4AL17CS017	Ashwini	P	5	6	4	0	0	0	5	6	4	0	0	0	30	Apply
4AL17CS046	Likitha M	P	5	0	0	5	4	3	2	6	2	0	0	0	22	Apply
4AL17CS028	Dheeraj Krishna Devadig	P	5	1	3	0	0	0	0	6	1	0	0	0	16	Apply
4AL17CS011	Apoorva H P	P	5	6	3	0	0	0	0	0	0	3	3	0	20	Apply
4AL17CS020	Chandana Patil	P	5	4	0	0	0	0	0	6	1	0	0	0	16	Apply
4AL17CS024	D Jasmine Joyline	P	5	6	4	5	1	3	5	6	3	0	0	0	29	Apply
4AL17CS048	Madan G Gudigar	P	5	6	2	0	0	0	5	5	3	0	0	0	26	Apply
4AL17CS053	Naik Nayana Ganapati	P	5	6	4	0	0	0	5	6	4	0	0	0	30	Apply
4AL17CS057	Pavana P	P	3	2	3	0	0	0	0	0	0	0	2	1	11	Apply
4AL17CS045	Lathik Moger	P	4	2	1	0	0	0	0	0	0	1	5	1	14	Apply
4AL17CS005	Amrutha M	P	5	6	4	0	0	0	0	6	3	2	4	2	24	Apply
4AL17CS009	Anvitha U	P	4	6	2	0	0	0	0	0	0	1	5	2	20	Apply
4AL17CS037	John Alsten Tauro	P	5	6	3	0	0	0	4	6	3	0	0	0	27	Apply
4AL17CS002	Ajeyashree K	P	3	6	4	0	5	0	1	5	3	0	2	0	22	Apply
4AL17CS018	Ashwini Shekarappa Jadamali	P	3	6	3	0	0	0	0	0	0	3	3	0	18	Apply
4AL17CS047	M C Suchithra Heggade	P	4	3	4	0	0	0	5	2	3	0	0	0	21	Analyze
4AL17CS096	Soundarya R	P	3	5	2	0	0	0	0	0	0	3	5	0	18	Apply
4AL17CS029	Dsouza Elston Ronald	P	0	0	0	4	3	4	4	6	4	0	0	0	25	Apply
4AL17CS012	Apoorva K N	P	4	5	3	0	0	0	5	6	3	0	0	0	26	Apply
4AL17CS040	Kavana V	P	5	2	4	0	0	0	1	2	1	0	0	0	15	Apply
4AL16CS047	Madhushree R	P	3	3	0	0	0	0	0	3	1	0	0	0	10	Apply
4AL17CS021	Chetana H	P	3	2	3	0	0	0	0	6	2	0	2	0	16	Apply
4AL17CS025	Datta Kiran A B	P	4	2	3	0	0	0	5	6	3	0	0	0	23	Apply
4AL17CS054	NANDITHA R SHETTY	P	5	6	4	0	0	0	3	6	3	0	0	0	27	Apply
4AL17CS033	Hemalatha S	P	3	2	2	0	0	0	0	4	3	0	0	0	14	Apply
4AL17CS006	Anilkumar B N	P	2	6	1	0	0	0	0	0	0	0	4	1	14	Apply
4AL17CS038	K Thrishul	P	4	6	4	0	0	0	5	6	4	0	0	0	29	Apply
4AL17CS019	Bhramari P Shetty	P	4	6	4	0	0	0	5	6	3	0	0	0	28	Apply
4AL17CS030	Gayatri V Kamat	P	3	2	0	0	0	0	0	4	2	0	0	0	11	Apply
4AL16CS078	S Harshith	P	3	3	2	0	0	0	2	5	1	0	0	0	16	Apply
4AL17CS015	Asha Rudrappa Totagi	P	0	0	0	5	6	4	0	0	0	5	5	4	29	Apply
4AL17CS049	Madan Gowda V	P	3	5	1	0	0	0	0	0	0	0	0	0	9	Understand
4AL17CS041	Kavya	P	5	2	2	0	0	0	0	6	4	0	0	0	19	Apply

USN	Name	Present (P)/ Absent (Ab)	Q1			Q2			Q3			Q4			Total Score	BT/CL
			a	b	c	a	b	c	a	b	c	a	b	c		
4AL17CS098	Spoorthi Dalaji	P	2	6	3	0	0	0	4	3	4	0	0	0	21	Apply
4AL17CS022	Chethana J	P	6	2	3	0	0	0	1	1	2	0	0	0	14	Apply
4AL17CS051	Mahek Sabha	P	4	3	2	0	0	0	3	3	1	0	0	0	16	Apply
4AL17CS055	Netra Suresh Gudagamnala	P	6	6	4	0	0	0	4	6	4	0	0	0	29	Apply
4AL17CS059	Prajna	P	4	6	2	0	0	0	4	6	0	0	0	0	22	Apply

Internal : 2

Semester:3-CBCS 2017

Date : 25/10/2018

Subject : ANALOG AND DIGITAL ELECTRONICS (17CS32)

Time : 15:00 - 16:30

Faculty : Shilpa

Max Marks: 30

Answer Any 2 Questions

Q.No			Max Marks	CO	BT/CL
1	a	What is PLA? Design 7-segment decoder using PLA.	5	3	L6
1	b	Derive the Characteristic equation, excitation table and state diagram for JK flip flop and D flip flop.	6	4	L6
1	c	What is decoder? Realize the following function using 3:8 decoder. $f_1(A,B,C)=\sum m(1,2,3,4)$ and $f_2(A,B,C)=\sum m(3,5,7)$.	4	3	L2
OR					
2	a	Write a Verilog code for the following. i) 3:8 Decoder. ii) SR flip flop.	5	3	L6
2	b	With neat logic diagram and truth table, explain the working of JK master slave flip flop.	6	4	L2
2	c	Distinguish between PLA and PAL.	4	3	L4
3	a	List the different types of shift registers. With an example explain 4 bit Serial In Serial Out (SISO) register using negative edge triggered D flip flop.	5	4	L2
3	b	Design Synchronous MOD-7 JK flip flop counter using synthesization along with the timing diagram.	6	4	L6

3	c	Distinugish between combinational circuit and sequential circuit.	4	4	L4
OR					
4	a	Explain 3 bit binary Ripple up counter with its block digarm, truth table and output waveform.	5	4	L2
4	b	Design Synchronous counter for the sequences 0--> 4-->1-->2-->6-->0, using D flip flop.	6	4	L6
4	c	Explain Ring counter and Johnson counter.	4	4	L2

Evaluation

USN	Name	Present (P)/ Absent (Ab)	Q1			Q2			Q3			Q4			Total Score	BT/CL
			a	b	c	a	b	c	a	b	c	a	b	c		
4AL17CS034	Jagath Haren	P	5	6	4	0	0	0	4	5	4	0	0	0	28	Create
4AL17CS003	Akshat Khandelwal	P	5	5	4	0	0	0	4	2	4	0	0	0	24	Create
4AL17CS007	Anusha	P	5	6	4	0	0	0	5	6	4	0	0	0	30	Create
4AL17CS039	Kanaka B S	P	5	5	3	0	0	0	0	0	0	5	2	4	24	Create
4AL17CS050	Mhaske Pooja Sambhaji	P	5	6	3	0	0	0	3	3	4	0	0	0	24	Create
4AL17CS031	Gowda Roshni Shivprakash	P	5	2	3	3	5	3	2	0	4	2	0	3	17	Create
4AL16CS114	THOKCHOM SANJIT	P	4	4	3	0	0	0	1	0	4	0	0	0	16	Create
4AL17CS016	Ashika	P	5	5	3	0	0	0	0	0	0	2	2	3	20	Create
4AL17CS044	Koushik S N	P	5	2	3	0	0	0	5	2	3	0	0	0	20	Create
4AL17CS027	Dhanya Bhat	P	5	6	4	5	0	4	4	4	4	0	0	0	27	Create
4AL17CS010	Apeksha Rajendra Rane	P	5	6	4	0	0	0	5	3	4	0	0	0	27	Create
4AL17CS042	Kavya R Shetty	P	4	2	3	1	0	0	3	2	4	0	0	0	18	Create
4AL17CS052	Nagashree Arun M	P	5	6	4	0	0	0	5	3	4	0	0	0	27	Create
4AL17CS056	Pallavi	P	5	6	4	0	0	0	5	4	4	1	0	0	28	Create
4AL17CS036	Jayraj ChiragKumar Shah	P	5	6	3	0	0	0	0	0	0	5	2	4	25	Create
4AL17CS035	Jayalakshmi M	P	0	0	0	4	5	4	5	6	4	0	0	0	28	Create
4AL17CS004	Akshata Narayana Hegde	P	5	6	4	0	0	0	5	6	4	0	0	0	30	Create
4AL17CS008	Anvitha Poojary	P	5	6	4	0	0	0	5	5	4	0	0	0	29	Create
4AL15CS050	Kiran A S	P	1	0	3	0	0	0	0	1	2	0	0	3	7	Analyze
4AL17CS032	Harshith C P	P	5	5	3	0	0	0	2	2	3	0	0	0	20	Create
4AL17CS097	Spoorthi M S	P	5	4	3	4	3	2	3	2	4	0	0	0	21	Create

Department of Computer Science and Engineering

USN	Name	Present (P)/ Absent (Ab)	Q1			Q2			Q3			Q4			Total Score	BT/CL
			a	b	c	a	b	c	a	b	c	a	b	c		
4AL17CS114	NIRIKSHA A	P	5	5	3	0	0	0	5	3	3	0	0	0	24	Create
4AL17CS013	Aruna K	P	5	4	0	0	0	0	3	2	4	0	0	0	18	Create
4AL17CS017	Ashwini	P	0	0	0	5	6	4	5	5	4	0	0	0	29	Create
4AL17CS046	Likitha M	P	2	5	3	0	0	0	3	0	4	0	0	0	17	Create
4AL17CS028	Dheeraj Krishna Devadig	P	4	2	3	0	0	0	3	0	4	0	0	0	16	Create
4AL17CS011	Apoorva H P	P	5	4	3	0	0	0	5	2	4	0	0	0	23	Create
4AL17CS020	Chandana Patil	P	4	5	3	2	5	3	5	0	3	0	0	0	20	Create
4AL17CS024	D Jasmine Joyline	P	5	6	4	0	0	0	0	0	0	5	6	4	30	Create
4AL17CS048	Madan G Gudigar	P	0	5	0	3	6	4	5	5	4	0	0	0	27	Create
4AL17CS053	Naik Nayana Ganapati	P	5	6	4	0	0	0	5	6	4	0	0	0	30	Create
4AL17CS057	Pavana P	P	5	6	3	0	0	0	0	0	0	3	2	2	21	Create
4AL17CS045	Lathik Moger	P	5	6	4	0	0	0	3	1	4	0	0	0	23	Create
4AL17CS005	Amrutha M	P	5	5	4	0	0	0	5	6	4	1	2	0	29	Create
4AL17CS009	Anvitha U	P	5	6	4	0	0	0	5	5	4	0	0	0	29	Create
4AL17CS037	John Alsten Tauro	P	5	6	4	5	0	4	0	0	0	4	6	4	29	Create
4AL17CS002	Ajeayashree K	P	5	5	4	5	1	0	5	2	4	0	0	0	25	Create
4AL17CS018	Ashwini Shekarappa Jadamali	P	0	0	0	3	6	4	0	0	0	4	1	4	22	Create
4AL17CS047	M C Suchithra Heggade	P	5	4	3	0	0	0	3	4	4	0	0	0	23	Create
4AL17CS096	Soundarya R	P	5	5	3	0	0	0	2	6	4	0	0	0	25	Create
4AL17CS029	Dsouza Elston Ronald	P	5	6	4	0	0	0	4	6	4	0	0	0	29	Create
4AL17CS012	Apoorva K N	P	5	4	4	0	0	0	5	6	4	0	0	0	28	Create
4AL17CS040	Kavana V	P	5	5	3	0	0	0	2	2	4	1	0	0	21	Create
4AL16CS047	Madhushree R	P	5	0	3	3	2	1	3	3	3	0	0	0	17	Create
4AL17CS021	Chetana H	P	5	4	3	0	0	0	0	0	0	4	2	4	22	Create
4AL17CS025	Datta Kiran A B	P	5	5	3	0	0	0	3	2	3	0	0	0	21	Create
4AL17CS054	NANDITHA R SHETTY	P	5	6	4	0	0	0	3	0	4	4	3	4	26	Create
4AL17CS033	Hemalatha S	P	5	6	4	0	0	0	5	3	4	0	0	0	27	Create
4AL17CS006	Anilkumar B N	P	4	2	4	0	0	0	0	3	3	0	0	0	16	Create
4AL17CS038	K Thrishul	P	5	6	4	0	0	0	5	6	4	0	0	0	30	Create
4AL17CS019	Bhramari P Shetty	P	5	4	4	0	0	0	5	4	4	0	0	0	26	Create
4AL17CS030	Gayatri V Kamat	P	5	5	3	0	0	0	3	0	4	0	0	0	20	Create
4AL16CS078	S Harshith	P	4	6	4	0	0	0	5	5	4	0	0	0	28	Create
4AL17CS015	Asha Rudrappa Totagi	P	0	0	0	5	6	4	5	2	4	0	0	0	26	Create

USN	Name	Present (P)/ Absent (Ab)	Q1			Q2			Q3			Q4			Total Score	BT/CL
			a	b	c	a	b	c	a	b	c	a	b	c		
4AL17CS049	Madan Gowda V	P	5	6	3	0	0	0	2	1	3	0	0	0	20	Create
4AL17CS041	Kavya	P	0	0	0	3	6	4	2	6	4	5	0	4	26	Create
4AL17CS098	Spoorthi Balaji	P	5	6	3	0	0	0	0	0	0	0	2	4	20	Create
4AL17CS022	Chethana J	P	5	4	3	4	5	1	3	2	4	0	0	0	21	Create
4AL17CS051	Mahek Sabha	P	5	5	3	0	0	0	0	0	0	5	0	4	22	Create
4AL17CS055	Netra Suresh Gudagamnala	P	0	0	0	5	6	3	5	4	3	0	0	0	26	Create
4AL17CS059	Prajna	P	5	4	4	0	0	0	3	3	3	0	0	0	22	Create

Internal : 3

Semester:3-CBCS 2017

Date : 26/11/2018

Subject : ANALOG AND DIGITAL ELECTRONICS (17CS32)

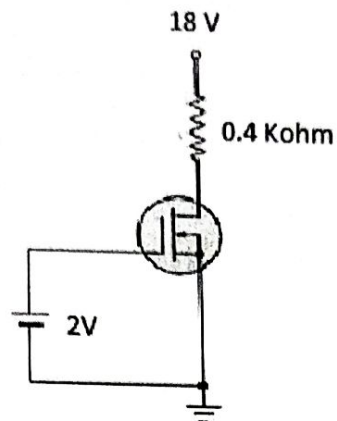
Time : 15:00 - 16:30

Faculty : Shilpa

Max Marks: 30

Answer Any 2 Questions

Q.No			Max Marks	CO	BT/CL
1	a	Explain binary weighted resistor D/A converter. Mention its drawback.	5	5	L2
1	b	Explain the operation and characteristics of N-Channel JFET.	6	1	L2
1	c	Differentiate between JFET and MOSFET.	4	1	L1
OR					
2	a	What is binary ladder? Explain the binary ladder with digital input 1000.	5	5	L2
2	b	Explain with the help of neat circuit diagram and characteristic curves working of N-channel DE-MOSFET.	6	1	L2
2	c	Figure (a), shows a biasing configuration using DE-MOSFET. Given the saturation drain current is 8mA and the pinchoff voltage is -2V, determine the value of drain source voltage, drain current.	4	1	L3



3	a	Explain digital clock with its block diagram.	5	5	L2
3	b	With the block diagram, explain the operation of a Astable multivibrator using IC555 timer.	6	1	L2
3	c	Define the following terms. i) CMRR ii) Slew rate iii) PSRR iv) Open-loop gain.	4	1	L1
OR					
4	a	Explain successive approximation converter with its block diagram. Give example for 4 bits.	5	5	L2
4	b	Explain with schematics operation of relaxation oscillator with relevant waveforms.	6	1	L2
4	c	What are active filters? Explain first order low pass active filters.	4	1	L2

Evaluation

USN	Name	Present (P)/ Absent (Ab)	Q1			Q2			Q3			Q4			Total Score	BT/CL
			a	b	c	a	b	c	a	b	c	a	b	c		
4AL17CS034	Jagath Haren	P	0	0	0	5	6	4	0	0	0	5	6	4	30	Apply
4AL17CS003	Akshat Khandelwal	P	5	6	4	0	0	0	5	5	4	0	0	0	29	Understand
4AL17CS007	Anusha	P	5	6	4	0	0	0	5	6	4	0	0	0	30	Understand
4AL17CS039	Kanaka B S	P	5	6	4	0	0	0	0	0	0	5	6	4	30	Understand
4AL17CS050	Mhaske Pooja Sambhaji	P	5	6	4	0	0	0	5	5	4	5	6	4	30	Understand

USN	Name	Present (P)/ Absent (Ab)	Q1			Q2			Q3			Q4			Total Score	BT/CL
			a	b	c	a	b	c	a	b	c	a	b	c		
4AL17CS031	Gowda Roshni Shivrakash	P	5	0	4	5	6	4	5	5	4	0	0	0	29	Apply
4AL16CS114	THOKCHOM SANJIT	P	1	4	3	0	0	0	0	0	0	4	5	0	17	Understand
4AL17CS016	Ashika	P	4	5	4	0	0	0	0	0	0	5	4	4	26	Understand
4AL17CS044	Koushik S N	P	5	0	4	0	0	0	5	6	0	0	0	0	20	Understand
4AL17CS027	Dhanya Bhat	P	0	0	0	5	6	2	3	6	1	0	0	0	23	Apply
4AL17CS010	Apeksha Rajendra Rane	P	0	0	0	5	6	3	4	6	4	0	0	0	28	Apply
4AL17CS042	Kavya R Shetty	P	0	6	4	2	0	2	4	6	0	1	0	0	20	Apply
4AL17CS052	Nagashree Arun M	P	5	6	4	0	0	0	5	6	4	0	0	0	30	Understand
4AL17CS056	Pallavi	P	5	6	4	0	0	0	3	6	4	0	0	0	28	Understand
4AL17CS036	Jayraj ChiragKumar Shah	P	4	6	4	0	0	0	5	6	4	0	0	0	29	Understand
4AL17CS035	Jayalakshmi M	P	4	6	2	0	0	0	5	6	0	0	0	0	23	Understand
4AL17CS004	Akshata Narayana Hegde	P	0	0	0	4	6	3	0	0	0	5	5	4	27	Apply
4AL17CS008	Anvitha Poojary	P	4	6	4	0	0	0	0	0	0	5	6	4	29	Understand
4AL15CS050	Kiran A S	P	1	2	4	0	0	0	4	3	1	0	0	0	15	Understand
4AL17CS032	Harshith C P	P	0	4	4	0	0	0	4	4	0	2	0	0	16	Understand
4AL17CS097	Spoorthi M S	P	3	4	4	0	0	0	0	0	0	2	0	2	15	Understand
4AL17CS114	NIRIKSHA A	P	4	0	4	0	0	0	5	2	0	0	0	0	15	Understand
4AL17CS013	Aruna K	P	4	3	4	0	0	0	0	0	0	4	6	4	25	Understand
4AL17CS017	Ashwini	P	4	6	4	0	0	0	0	0	0	5	6	4	29	Understand
4AL17CS046	Likitha M	P	2	6	4	0	0	0	0	0	0	4	2	2	20	Understand
4AL17CS028	Dheeraj Krishna Devadig	P	4	2	4	0	0	0	2	2	0	0	0	0	14	Understand
4AL17CS011	Apoorva H P	P	5	6	4	0	0	0	0	0	0	5	5	4	29	Understand
4AL17CS020	Chandana Patil	P	4	2	4	0	0	0	0	0	0	2	0	4	16	Understand
4AL17CS024	D Jasmine Joyline	P	4	6	4	0	0	0	5	6	4	0	0	0	29	Understand
4AL17CS048	Madan G Gudigar	P	4	6	4	0	0	0	0	0	0	4	6	4	28	Understand
4AL17CS053	Naik Nayana Ganapati	P	0	0	0	5	6	4	4	6	3	0	0	0	28	Apply
4AL17CS057	Pavana P	P	5	6	4	0	0	0	4	6	0	0	0	0	25	Understand
4AL17CS045	Lathik Moger	P	0	0	0	4	1	4	0	0	0	5	6	4	24	Apply
4AL17CS005	Amrutha M	P	5	6	4	0	0	0	0	0	0	5	6	4	30	Understand
4AL17CS009	Anvitha U	P	4	5	4	0	0	0	0	0	0	5	5	2	25	Understand
4AL17CS037	John Alsten Tauro	P	0	0	0	4	6	2	4	6	0	0	0	0	22	Apply
4AL17CS002	Ajeayashree K	P	4	6	4	0	0	0	0	0	0	4	6	4	28	Understand
4AL17CS018	Ashwini Shekarappa Jadamall	P	0	0	0	3	4	4	0	0	0	5	5	4	25	Apply

USN	Name	Present (P) Absent (Ab)	Q1			Q2			Q3			Q4			Total Score	BT/CL
			a	b	c	a	b	c	a	b	c	a	b	c		
4AL17CS047	M C Suchithra Heggade	P	4	3	4	0	0	0	4	6	4	0	0	0	25	Understand
4AL17CS096	Soundarya R	P	5	0	4	0	0	0	0	0	0	1	6	4	20	Understand
4AL17CS029	Dsouza Elston Ronald	P	0	0	0	5	6	4	5	6	4	0	0	0	30	Apply
4AL17CS012	Apoorva K N	P	0	6	4	0	0	0	0	0	0	5	6	4	25	Understand
4AL17CS040	Kavana V	P	5	5	4	0	0	0	4	5	4	0	0	0	27	Understand
4AL16CS047	Madhushree R	P	3	4	3	0	0	0	0	0	0	0	4	0	14	Understand
4AL17CS021	Chetana H	P	0	0	0	1	5	2	0	0	0	5	5	4	22	Apply
4AL17CS025	Datta Kiran A B	P	5	4	4	0	0	0	4	6	1	0	0	0	24	Understand
4AL17CS054	NANDITHA R SHETTY	P	5	6	4	4	6	4	4	6	4	0	0	0	29	Apply
4AL17CS033	Hemalatha S	P	5	6	4	0	0	0	5	6	0	0	0	0	26	Understand
4AL17CS006	Anilkumar B N	P	4	0	4	0	0	0	4	2	0	0	0	0	14	Understand
4AL17CS038	K Thrishul	P	0	0	0	5	6	4	5	5	4	2	1	2	29	Apply
4AL17CS019	Bhramari P Shetty	P	5	6	4	0	0	0	5	6	4	0	0	0	30	Understand
4AL17CS030	Gayatri V Kamat	P	4	3	4	0	0	0	2	2	1	0	0	0	16	Understand
4AL16CS078	S Harshith	P	0	0	0	4	5	0	0	0	0	5	1	4	19	Understand
4AL17CS015	Asha Rudrappa Totagi	P	4	6	4	0	0	0	0	0	0	5	6	4	29	Understand
4AL17CS049	Madan Gowda V	P	0	0	4	0	0	2	0	4	0	0	0	0	8	Apply
4AL17CS041	Kavya	P	0	0	0	2	6	4	4	6	3	0	0	0	25	Apply
4AL17CS098	Spoorthi Balaji	P	0	0	0	5	6	4	5	6	0	0	0	0	26	Apply
4AL17CS022	Chethana J	P	3	1	3	0	0	0	2	5	2	2	2	2	16	Understand
4AL17CS051	Mahek Sabha	P	2	6	4	0	0	0	3	4	0	0	0	0	19	Understand
4AL17CS055	Netra Suresh Gudagamnala	P	5	6	4	0	0	0	5	6	4	0	0	0	30	Understand
4AL17CS059	Prajna	P	0	0	3	4	5	4	3	6	0	0	0	0	22	Apply

HOD
26/04/2024
Department of Computer Science & Engineering

PRINCIPAL
Alva's Institute of Engg. & Technology
Mijan, 580001-574 223
PRINCIPAL



Alva's Institute of Engineering & Technology

Shobhavana Campus, Mijar, Moodbidri, D.K – 574225

Phone: 08258-262725, Fax: 08258-262726

Third Semester B.E. (CSE)

17CS32 – ANALOG AND DIGITAL ELECTRONICS

Assignment-1

NOTE: LAST DATE FOR SUBMISSION IS: 29/09/2018

1. Explain and show how basic gates can be implemented using universal gates.
2. Solve the following using K-map.
 - i) $F(A,B,C,D) = \sum m(1,4,7,11,15) + d(3,6,10,14)$
 - ii) $F(A,B,C,D) = \prod M(2,3,4,5,12,13,14) + d(0,6,8,9,10)$
3. Solve the boolean function $F(A,B,C,D) = \sum m(1,3,8,9,10,11,15) + d(0,2,6)$ using Quine-McClusky method.
4. What is multiplexer? Explain 1:4 multiplexer with its truth table and logic circuit. Design and Implement the boolean expression using 1:8 multiplexer.
 $Y = A'B'C'D' + A'BC'D' + AB'C'D' + A'BC'D + AB'C'D + ABCD' + ABCD$
5. Show how using 3:8 decoder and multi input OR gates, following Boolean expression can be realized simultaneously.
 $F1(A,B,C) = \sum m(0,4,6)$ $F2(A,B,C) = \sum m(0,5)$ $F3(A,B,C) = \sum m(1,2,3,7)$
6. Write the Verilog code for the following.
 - i) Half adder and Full subtractor.
 - ii) 16:1 multiplexer.
7. What is magnitude comparator? Explain 1 bit magnitude comparator.
8. Design 7 segment display decoder using PLA.



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Third Semester B.E. (CSE)

17CS32 – ANALOG AND DIGITAL ELECTRONICS

Assignment-2

NOTE: LAST DATE FOR SUBMISSION IS: 31/10/2018

1. Obtain the characteristic equation, excitation table, state diagram for D flip flop and J K flip flop.
2. With a neat logic diagram and truth table explain the working of JK master slave flip flop along with its implementation using NAND gates.
3. What is register? Explain the working of parallel in serial out shift register with timing waveform.
4. Explain the working of universal shift register with its truth table.
5. What is counter? Explain 3 bit binary ripple up counter along with its block diagram, truth table and timing diagram.
6. Design synchronous Mod-6 Counter using JK Flip flop.
7. Design asynchronous counter for the sequence $0 \rightarrow 4 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 0 \rightarrow 4$ using SR flip flop.
8. List the different application of shift registers and explain any 2 applications.



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Third Semester B.E. (CSE)

17CS32 – ANALOG AND DIGITAL ELECTRONICS

Assignment-3

NOTE: LAST DATE FOR SUBMISSION IS: 19/11/2018

1. Explain binary weighted resistor D/A converter. Mentions its drawbacks.
2. What is binary ladder? Explain the binary ladder with digital input 1000.
3. Explain with block diagram operation of successive approximation converter.
4. Explain counter type A/D converter with block diagram.
5. Explain dual slope A/D converter with its slope waveform.
6. What is MOSFET. Explain the construction of n-channel E-MOSFET and DE-MOSFETS.
7. List and explain any two applications of FET's
8. Explain with schematics operation of relaxation oscillator with relevant waveforms.
9. What is multivibrator? Explain the operation of Astable multivibrator using IC555 timer.
10. What are active filters? Explain active low pass filter.

5. Course Information

5.3 Other Assessment

ASSIGNMENT

Title of the Course: ANALOG AND DIGITAL ELECTRONICS

Course Code: 17CS32

Assignment # : 1

Max Marks : 10

Start Date : 2018-09-17

End Date : 2018-09-29

Course Outcomes : 2, 3

Blooms Level : Apply

Description : Answer all the questions

Evaluation

USN	Name	Score
4AL17CS034	Jagath Haren	9
4AL17CS003	Akshat Khandelwal	10
4AL17CS007	Anusha	9
4AL17CS039	Kanaka B S	9
4AL17CS050	Mhaske Pooja Sambhaji	8
4AL17CS031	Gowda Roshni Shivprakash	8
4AL16CS114	THOKCHOM SANJIT	8
4AL17CS016	Ashika	9
4AL17CS044	Koushik S N	8
4AL17CS027	Dhanya Bhat	9
4AL17CS010	Apeksha Rajendra Rane	8
4AL17CS042	Kavya R Shetty	8
4AL17CS052	Nagashree Arun M	9
4AL17CS056	Pallavi	9
4AL17CS036	Jayraj ChiragKumar Shah	10
4AL17CS035	Jayalakshmi M	8
4AL17CS004	Akshata Narayana Hegde	9
4AL17CS008	Anvitha Poojary	8
4AL15CS050	Kiran A S	8

Department of Computer Science and Engineering

USN	Name	Score
4AL17CS032	Harshith C P	8
4AL17CS097	Spoorthi M S	8
4AL17CS114	NIRIKSHA A	9
4AL17CS013	Aruna K	8
4AL17CS017	Ashwini	9
4AL17CS046	Likitha M	8
4AL17CS028	Dheeraj Krishna Devadig	8
4AL17CS011	Apoorva H P	8
4AL17CS020	Chandana Patil	8
4AL17CS024	D Jasmine Joyline	9
4AL17CS048	Madan G Gudigar	10
4AL17CS053	Naik Nayana Ganapati	9
4AL17CS057	Paavana P	9
4AL17CS045	Lathik Moger	8
4AL17CS005	Amrutha M	8
4AL17CS009	Anvitha U	8
4AL17CS037	John Alsten Tauro	9
4AL17CS002	Ajeyashree K	8
4AL17CS018	Ashwini Shekarappa Jadamali	9
4AL17CS047	M C Suchithra Heggade	8
4AL17CS096	Soundarya R	8
4AL17CS029	Dsouza Elston Ronald	9
4AL17CS012	Apoorva K N	8
4AL17CS040	Kavana V	8
4AL16CS047	Madhushree R	7
4AL17CS021	Chetana H	8
4AL17CS025	Datta Kiran A B	10
4AL17CS054	NANDITHA R SHETTY	9
4AL17CS033	Hemalatha S	9

USN	Name	Score
4AL17CS006	Anilkumar B N	9
4AL17CS038	K Thrishul	10
4AL17CS019	Bhramari P Shetty	8
4AL17CS030	Gayatri V Kamat	8
4AL16CS078	S Harshith	10
4AL17CS015	Asha Rudrappa Totagi	9
4AL17CS049	Madan Gowda V	8
4AL17CS041	Kavya	9
4AL17CS098	Spoorthi Balaji	8
4AL17CS022	Chethana J	8
4AL17CS051	Mahek Sabha	9
4AL17CS055	Netra Suresh Gudagamnala	9
4AL17CS059	Prajna	9

Assignment # : 2**Max Marks : 10****Start Date : 2018-10-16****End Date : 2018-10-31****Course Outcomes : 4 , 5****Blooms Level : Apply****Description : Answer all the Questions****Evaluation**

USN	Name	Score
4AL17CS034	Jagath Haren	10
4AL17CS003	Akshat Khandelwal	10
4AL17CS007	Anusha	10
4AL17CS039	Kanaka B S	9
4AL17CS050	Mhaske Pooja Sambhaji	10
4AL17CS031	Gowda Roshni Shivprakash	10
4AL16CS114	THOKCHOM SANJIT	9
4AL17CS016	Ashika	9
4AL17CS044	Koushik S N	9

USN	Name	Score
4AL17CS027	Dhanya Bhat	10
4AL17CS010	Apeksha Rajendra Rane	10
4AL17CS042	Kavya R Shetty	10
4AL17CS052	Nagashree Arun M	10
4AL17CS056	Pallavi	10
4AL17CS036	Jayraj ChiragKumar Shah	9
4AL17CS035	Jayalakshmi M	10
4AL17CS004	Akshata Narayana Hegde	9
4AL17CS008	Anvitha Poojary	10
4AL15CS050	Kiran A S	9
4AL17CS032	Harshith C P	9
4AL17CS097	Spoorthi M S	9
4AL17CS114	NIRIKSHA A	8
4AL17CS013	Aruna K	8
4AL17CS017	Ashwini	9
4AL17CS046	Likitha M	10
4AL17CS028	Dheeraj Krishna Devadig	8
4AL17CS011	Apoorva H P	10
4AL17CS020	Chandana Patil	10
4AL17CS024	D Jasmine Joyline	10
4AL17CS048	Madan G Gudigar	9
4AL17CS053	Naik Nayana Ganapati	10
4AL17CS057	Pavana P	10
4AL17CS045	Lathik Moger	10
4AL17CS005	Amrutha M	10
4AL17CS009	Anvitha U	9
4AL17CS037	John Alsten Tauro	10
4AL17CS002	Ajeyashree K	10
4AL17CS018	Ashwini Shekarappa Jadamali	10

USN	Name	Score
4AL17CS047	M C Suchithra Heggade	10
4AL17CS096	Soundarya R	10
4AL17CS029	Dsouza Elston Ronald	10
4AL17CS012	Apoorva K N	10
4AL17CS040	Kavana V	10
4AL16CS047	Madhushree R	10
4AL17CS021	Chetana H	10
4AL17CS025	Datta Kiran A B	9
4AL17CS054	NANDITHA R SHETTY	10
4AL17CS033	Hemalatha S	10
4AL17CS006	Anilkumar B N	8
4AL17CS038	K·Thrishul	10
4AL17CS019	Bhramari P Shetty	10
4AL17CS030	Gayatri V Kamat	9
4AL16CS078	S Harshith	10
4AL17CS015	Asha Rudrappa Totagi	10
4AL17CS049	Madan Gowda V	8
4AL17CS041	Kavya	10
4AL17CS098	Spoorthi Balaji	10
4AL17CS022	Chethana J	9
4AL17CS051	Mahek Sabha	10
4AL17CS055	Netra Suresh Gudagamnala	10
4AL17CS059	Prajna	10

Assignment # : 3

Start Date : 2018-11-13

Course Outcomes : 1 , 5

Description : Answer all the questions

Max Marks : 10

End Date : 2018-11-19

Blooms Level : Understand

Evaluation

USN	Name	Score
4AL17CS034	Jagath Haren	10
4AL17CS003	Akshat Khandelwal	9
4AL17CS007	Anusha	10
4AL17CS039	Kanaka B S	10
4AL17CS050	Mhaske Pooja Sambhaji	10
4AL17CS031	Gowda Roshni Shivprakash	10
4AL16CS114	THOKCHOM SANJIT	9
4AL17CS016	Ashika	10
4AL17CS044	Koushik S N	9
4AL17CS027	Dhanya Bhat	10
4AL17CS010	Apeksha Rajendra Rane	10
4AL17CS042	Kavya R Shetty	10
4AL17CS052	Nagashree Arun M	9
4AL17CS056	Pallavi	10
4AL17CS036	Jayraj ChiragKumar Shah	10
4AL17CS035	Jayalakshmi M	10
4AL17CS004	Akshata Narayana Hegde	10
4AL17CS008	Anvitha Poojary	10
4AL15CS050	Kiran A S	9
4AL17CS032	Harshith C P	10
4AL17CS097	Spoorthi M S	9
4AL17CS114	NIRIKSHA A	9
4AL17CS013	Aruna K	9
4AL17CS017	Ashwini	10
4AL17CS046	Likitha M	9
4AL17CS028	Dheeraj Krishna Devadig	9
4AL17CS011	Apoorva H P	10
4AL17CS020	Chandana Patil	10

USN	Name	Score
4AL17CS024	D Jasmine Joyline	10
4AL17CS048	Madan G Gudigar	10
4AL17CS053	Naik Nayana Ganapati	10
4AL17CS057	Pavana P	10
4AL17CS045	Lathik Moger	9
4AL17CS005	Amrutha M	9
4AL17CS009	Anvitha U	10
4AL17CS037	John Alsten Tauro	10
4AL17CS002	Ajeyashree K	10
4AL17CS018	Ashwini Shekarappa Jadamali	10
4AL17CS047	M C Suchithra Heggade	9
4AL17CS096	Soundarya R	10
4AL17CS029	Dsouza Elston Ronald	10
4AL17CS012	Apoorva K N	10
4AL17CS040	Kavana V	9
4AL16CS047	Madhushree R	9
4AL17CS021	Chetana H	9
4AL17CS025	Datta Kiran A B	10
4AL17CS054	NANDITHA R SHETTY	10
4AL17CS033	Hemalatha S	10
4AL17CS006	Anilkumar B N	9
4AL17CS038	K Thrishul	10
4AL17CS019	Bhramari P Shetty	9
4AL17CS030	Gayatri V Kamat	10
4AL16CS078	S Harshith	9
4AL17CS015	Asha Rudrappa Totagi	10
4AL17CS049	Madan Gowda V	8
4AL17CS041	Kavya	10
4AL17CS098	Spoorthi Balaji	10



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DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Academic year 2018-2019

Rubrics used for assignment evaluation

Parameters	Not submitted	Incomplete Assignment	Correctness of the problem/ Program	Timely submitted with Correctness of the problem/ Program
Marks allocation	0	1-4	5-9	10

to
faculty

Arjun
HOD

CBCS Scheme

USN

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15CS32

Third Semester B.E. Degree Examination, June/July 2018 Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

- 1 a. What is MOSFET? Name its types. Explain the construction of n-channel E-MOSFET. (06 Marks)
b. Compare JFET and MOSFET. (05 Marks)
c. Explain self-bias circuit for JFET. (05 Marks)

OR

- 2 a. Define i) CMRR ii) Slew rate iii) PSRR iv) Bandwidth pertaining to OPAMP. (06 Marks)
b. Explain with schematics operation of relaxation oscillator with relevant waveforms. (05 Marks)
c. What are active filters? Explain active low pass filter. (05 Marks)

Module-2

- 3 a. Using Q-M method, simplify the expression $f(A, B, C, D) = \sum(0, 3, 5, 6, 7, 11, 14)$. (06 Marks)
b. Explain about positive and negative logic prove that positive 'OR' is equal to negative 'AND'. (05 Marks)
c. What are Hazards? Briefly describe about designing Hazard free circuit. (05 Marks)

OR

- 4 a. Give Sum-Of-Product (SOP) and Product-Of-Sum (POS) circuit for $f(A, B, C, D) = \sum m(6, 8, 9, 10, 11, 12, 13, 14, 15)$. (06 Marks)
b. Explain the verilog program structure. (05 Marks)
c. Design a logic circuit to provide an output when any two or three of four switches are closed. (05 Marks)

Module-3

- 5 a. Implement the following Boolean function using 4:1 multiplexer $F(A, B, C, D) = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$. (06 Marks)
b. Construct 16:1 multiplexer using 4:1 and 2:1 multiplexer. (05 Marks)
c. What is a decoder? Give the circuit for 3:8 decoder. (05 Marks)

OR

- 6 a. What is a magnitude comparator? Explain a 1-bit comparator with truth table and circuit diagram. (06 Marks)
b. Briefly explain about parity generators and checkers. For a 3 bit message, give the expression for even parity bit. (05 Marks)
c. Compare and contrast PLA and PAL. (05 Marks)

Module-4

- 7 a. Explain the working of JK master slave flip-flop with a sketch, truth table and symbol. (06 Marks)
b. Give a brief account on flip flop as finite state machine. (05 Marks)
c. Briefly describe about sequential logic circuit. (05 Marks)

OR

- 8 a. Enumerate different types of shift registers. Explain Serial In Serial Out (SISO) register. (06 Marks)
b. Mention the applicators of shift registers. (05 Marks)
c. Using behavioral model write Verilog HDL code for a 'D' flipflop with reset input. (05 Marks)

Module-5

- 9 a. Explain digital clock with block diagram. (06 Marks)
b. Design a 3 bit synchronous binary counter using JK flip flop. (05 Marks)
c. Mention different types of A/D converters and test its specifications. (05 Marks)

OR

- 10 a. Explain binary weighted resistor D/A converter. Mention its drawbacks. (06 Marks)
b. Describe about successive approximation type ADC. (05 Marks)
What is the resolution of a 12 bit D/A converter which uses a binary ladder, if the full scale output is +10V? (05 Marks)

CBCS Scheme

USN

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15CS32

Third Semester B.E. Degree Examination, Dec.2017/Jan.2018

Analog and Digital Electronics (ADE)

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

- 1 a. Explain the operation and characteristics of N-channel JFET. (08 Marks)
- b. With block diagram, explain the operation of a Astable multivibrator using IC 555. (08 Marks)

OR

- 2 a. With circuit diagram, explain the operation of a Relaxation oscillator. (06 Marks)
- b. Fig. Q2(b), shows a Biasing configuration using DEMOSFET given that the saturation drain current is 8mA and the pinch off voltage is -2V.

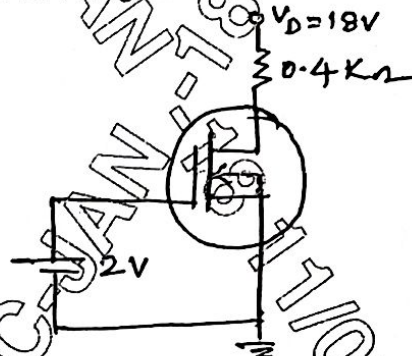


Fig. Q2(b)

- c. Determine the value of gate source voltage drain current of drain source voltage. (06 Marks)
- d. Write the advantages of MOSFET over JFET. (04 Marks)

Module-2

- 3 a. Give the simplest logic circuit for following logic equation where d represents don't care condition for following locations:

$$F(A, B, C, D) = \sum m(7) + d(10, 11, 12, 13, 14, 15).$$
 (06 Marks)
- b. Simplify the following Boolean function by using Quine – McClusky method.

$$F(A, B, C, D) = \sum m(0, 2, 3, 6, 7, 8, 10, 12, 13).$$
 (10 Marks)

OR

- 4 a. What are Hazards? Explain the types of Hazards and it covers. (08 Marks)
- b. Discuss Briefly an HDL Implementation models. (04 Marks)
- c. Explain the concept of Duality in Digital circuits. (04 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.



15CS32

Module-3

- 5 a. What is multiplexer? Design a 32:1 multiplexer using 16:1 MUX and one 2:1 multiplexer. (05 Marks)
- b. Show how using a 3 to 8 Decoder and multi input OR Gates following Boolean Expressions can be realized simultaneously. (06 Marks)
- $F(A, B, C) = \sum m(0, 4, 6)$
 $F(A, B, C) = \sum m(1, 2, 3, 7)$
 $F(A, B, C) = \sum m(0, 5)$
- c. Show how two 1 to 16 DEMUX can be connected to get 1 to 32 DEMUX. (05 Marks)

OR

- 6 a. Explain parity Generators and checkers using suitable examples. (05 Marks)
- b. What is Magnitude Comparator? Explain 1 bit magnitude comparator. (05 Marks)
- c. What is PLA? Design seven segment Display using PLA. (06 Marks)

Module-4

- 7 a. Explain 4 bit serial in parallel out register. (04 Marks)
- b. Explain a 3 bit binary Ripple up counter. Give the block diagram, truth table and output waveforms. (06 Marks)
- c. Explain the working of JK master slave Flip Flop along with implementation using NAND Gates. (06 Marks)

OR

- 8 a. Design synchronous MOD -6 counter with truth table and state diagram. (06 Marks)
- b. What is universal shift Register? Explain any one application of universal shift register with block diagram and truth table. (06 Marks)
- c. Write the comparison between Synchronous and Asynchronous counter. (04 Marks)

Module-5

- 9 a. Explain 5 bit Resistive divider with diagram. (06 Marks)
- b. Explain with neat diagram the working principle of Digital clock. (05 Marks)
- c. Explain the terms Accuracy and Resolution for D/A converter. (05 Marks)

OR

- 10 a. Explain with Block diagram the operation of successive approximation converter. (08 Marks)
- b. Explain counter type A/D converter with diagram. (08 Marks)

CBCS Scheme

USN

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15CS32

Third Semester B.E. Degree Examination, June/July 2017 Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

- 1 a. Explain with help of a circuit diagram and characteristic curves working of N-channel DE MOSFET. (12 Marks)
- b. List and explain any one application of FET and its working with circuit Diagram. (04 Marks)

OR

- 2 a. Explain the performance parameters of operational amplifier. (08 Marks)
- b. Mention and explain the working of any two applications of operational amplifier. (08 Marks)

Module-2

- 3 a. What is a logical gate? Realize $((A + B) \cdot C)D$ using only NAND Gates. (04 Marks)
- b. Describe positive and Negative logic. List the equivalences between them. (04 Marks)
- c. Find the minimal SOP (sum of product) for the following Boolean functions using K-map
 - i) $f(a, b, c, d) = \sum m(6, 7, 9, 10, 13) + d(1, 4, 5, 11)$
 - ii) $f(a, b, c, d) = \pi M(1, 2, 3, 4, 10) + d(0, 15)$ (08 Marks)

OR

- 4 a. Using Quine – McClusky Method simplify the following Boolean equation.
 $f(a, b, c, d) = \sum m(0, 1, 2, 3, 10, 11, 12, 13, 14, 15)$. (10 Marks)
- b. Define Hazard. Explain Different Types of Hazards. (06 Marks)

Module-3

- 5 a. What is multiplexer? Design a 32 to 1 multiplexer (MUX) using two 16 to 1 MUX and one 2 to 1 MUX. (04 Marks)
- b. Show How using 3 to 8 Decoder and multi input OR gates, following Boolean Expressions can be realized simultaneously
 $F_1(a, b, c) = \sum m(0, 4, 6)$, $F_2(a, b, c) = \sum m(0, 5)$, $F_3(a, b, c) = \sum m(1, 2, 3, 7)$ (05 Marks)
- c. Design 7 segment Decoder using PLA. (07 Marks)

OR

- 6 a. Implement the Boolean function expressed by SOP $f(a, b, c, d) = \sum m(1, 2, 5, 6, 9, 12)$ using 8 : 1 MUX. (04 Marks)
- b. What is magnitude comparator? Design and explain 2 bit magnitude comparator. (08 Marks)
- c. Differentiate between combinational and sequential circuit. (04 Marks)

Module-4

- 7 a. With a neat logic diagrams and truth table. Explain the working of JK master slave Flip-Flop along with its implementation using NAND Gates. (10 Marks)
- b. Derive the characteristic equation for SR, D and JK Flip-Flop. (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and/or equations written eg. 42+8 = 50, will be treated as malpractice.

OR

- 8 a. Using Negative Edge triggered D-Flip Flop. Draw a Logic diagram of 4 bit serial in serial out (SISO) Register. Draw the waveform to shift Binary number 1010 into this register. (06 Marks)
- b. Explain with neat diagram How shift Register can be applied for serial addition. (07 Marks)
- c. Differentiate between synchronous and Asynchronous counter. (03 Marks)

Module-5

- 9 a. Design Asynchronous counter for the sequences $0 \rightarrow 4 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 0 \rightarrow 4$. Using S. R Flip-Flop. (12 Marks)
- b. With neat diagram. Explain Digital Clock. (04 Marks)

OR

- 10 a. Explain 2 bit simultaneous A/D converter. (10 Marks)
- b. What is Binary Ladder? Explain the Binary Ladder with Digital input of 1000. (06 Marks)



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Third Semester B.E. Degree Examination, Dec.2016/Jan.2017
Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 80

Note: Answer FIVE full questions, choosing one full question from each module.

Module-1

- 1 a. Explain the working of N-channel DE-MOSFET, with the help of neat diagram. (08 Marks)
- b. With circuit diagram, explain any two application of FET. (06 Marks)
- c. How CMOS can be used as inverting switch? (02 Marks)

OR

- 2 a. Design a voltage divider bias network using a DEMOSFET with supply voltage $V_{DD} = 16V$, $I_{DSS} = 10mA$ and $V_p = 5V$ to have a quiescent drain current of $5mA$ and gate voltage of $4V$. (Assume the drain resistor R_D to be four times the source resistor R_S and $R_2 = 1k\Omega$). (08 Marks)
- b. Explain the performance parameters of Op-amp. (08 Marks)

Module-2

- 3 a. Minimize the following Boolean function using K-map method
 $f(a, b, c, d) = \sum m(5, 6, 7, 12, 13) + \sum d(4, 9, 14, 15)$. (06 Marks)
- b. Apply Quine Mc-Clusky method to find the essential prime implicants for the Boolean expression $f(a, b, c, d) = \sum m(1, 3, 6, 7, 9, 10, 12, 13, 14, 15)$. (10 Marks)

OR

- 4 a. A digital system is to be designed in which the month of the year is given as input is four bit form. The month January is represented as '0000', February as '0001' and so on. The output of the system should be '1' corresponding to the input of the month containing 31 days or otherwise it is '0'. Consider the excess number in the input beyond '1011' as don't care conditions for the system of four variables. (ABCD) find the following :
 i) Write truth table and Boolean expression in SOP $\sum m$ and POS $\prod M$ form.
 ii) Using K-map simplify the Boolean expression of canonical mini term form.
 iii) Using Basic gates implement logical circuit. (10 Marks)
- b. What is Hazard? List the type of hazards and explain static 0 and static - 1 hazard. (06 Marks)

Module-3

- 5 a. Implement the following function using 8:1 multiplexer $f(a, b, c, d) = \sum m(0, 1, 5, 6, 8, 10, 12, 15)$. (06 Marks)
- b. Realize the following function using 3:8 decoder
 i) $f(a, b, c) = \sum m(1, 2, 3, 4)$ ii) $f(a, b, c) = \sum m(3, 5, 7)$. (04 Marks)
- c. What is Magnitude Comparator? Explain 1 bit magnitude comparator. (06 Marks)

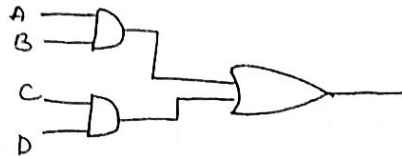
OR

- 6 a. Design 7-segment decoder using PLA. (08 Marks)
- b. Differentiate between Combinational and Sequential circuit. (04 Marks)

- c. Write VHDL code for given circuit.

(04 Marks)

Fig.Q6(c)



Module-4

- 7 a. What is Race around condition? With block diagram and truth table, explain the working of JK master – slave flip – flop. (10 Marks)
 b. Give State transition diagram and characteristics equation for JK and SR Flip Flop. (06 Marks)

OR

- 8 a. With neat diagram, explain Ring counter. (04 Marks)
 b. What is Shift Register? With neat diagram, explain 4 bit parallel in serial out shift registers. (08 Marks)
 c. Compare Synchronous and Asynchronous counter. (04 Marks)

Module-5

- 9 a. Define Counter. Design A synchronous counter for the sequence $0 \rightarrow 4 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 0 \rightarrow 4$ using JK Flip – Flop. (12 Marks)
 b. Explain Digital clock, with neat diagram. (04 Marks)

OR

- 10 a. Explain the Binary ladder with Digital input of 1000. (06 Marks)
 b. Explain 2 bit simultaneous A/D converter. (10 Marks)



ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

Shobhavana Campus, Mijar, Moodbidri, D.K - 574225

Phone: 08258-262725, Fax: 08258-262726

LIST OF WEAK STUDENTS

Academic Year: 2018-2019 (ODD)

Degree: B.E.

Department: Department of Computer Science & Engineering

Semester: 3rd Section: A

Scheme: CBCS

Sl. No	USN	Names
1.	4AL15CS050	Kiran A S
2.	4AL16CS047	Madushree R
3.	4AL16CS078	Harshith S
4.	4AL16CS114	Thokchom Sanjit
1.	4AL17CS021	Chetana H
2.	4AL17CS022	Chethana J
3.	4AL17CS030	Gayatri V Kamat
4.	4AL17CS032	Harshith C P
5.	4AL17CS040	Kavana V
6.	4AL17CS049	Madan Gowda V
7.	4AL17CS097	Spoorthi M S

Faculty

Army
HOD



ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

Shobhavana Campus, Mijar, Moodbidri, D.K – 574225

Phone: 08258-262725, Fax: 08258-262726

LIST OF BRIGHT STUDENTS

Academic Year: 2018-2019 (ODD)

Degree: B.E.

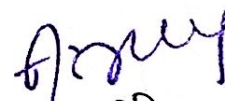
Department: Department of Computer Science & Engineering

Semester: 3rd Section: A

Scheme: CBCS

SL. NO	USN	NAME
1	4AL17CS007	Anusha
2	4AL17CS008	Anvitha Poojary
3	4AL17CS015	Asha Rudrappa Totagi
4	4AL17CS017	Ashwini
5	4AL17CS024	D Jasmine Joyline
6	4AL17CS029	Dsouza Elston Ronald
7	4AL17CS034	Jagath Haren
8	4AL17CS038	K Thrishul
9	4AL17CS052	Nagashree Arun M
10	4AL17CS053	Naik Nayana Ganapati


Faculty


HOD

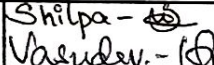
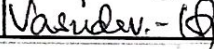
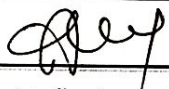
COURSE OUTCOMES (COs) ASSESSMENT MATRIX					
Alva's Institute of Engineering and Technology, Moodbidri					
Department of Computer Science and Engineering					
Academic Year:		2018-2019		CO Attainment Indirect	CO Attainment
Course Name & Course Code		Analog and Digital Electronics/17CS32			
Faculty Name:		Ms. Shilpa & Mr. Vasudev Shahapur			
CO Attainment - Direct					
Cos	Formative Assessment	Summative Assessment	Total Attainment		
17CS32.1	3	3	3.00	3	3
17CS32.2	3	3	3.00	3	3
17CS32.3	3	3	3.00	3	3
17CS32.4	3	3	3.00	3	3
17CS32.5	3	3	3.00	3	3
17CS32.6					
Average			3.00	3	3

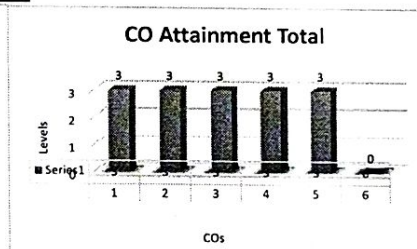
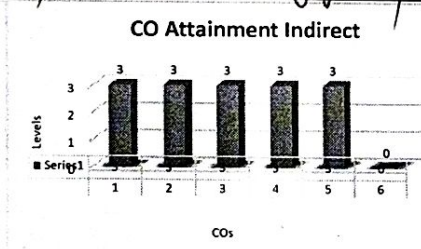
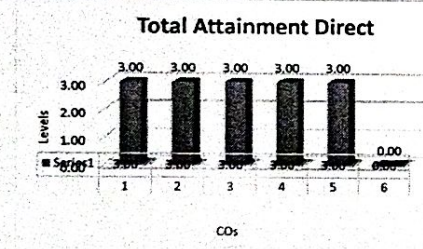
Attainment Level 1: 50% students rated more than or equal to 50% of maximum marks
 Attainment Level 2: 60% students rated more than or equal to 50% of maximum marks
 Attainment Level 3: 70% students rated more than or equal to 50% of maximum marks

Note:

Total Attainment Direct = (Weightage*Formative Assessment)+(Weightage*Summative Assessment) Weightage for Formative Assessment = 50%; Weightage for Summative Assessment = 50%

CO Attainment = (Weightage*Total Attainment Direct)+(Weightage*CO Attainment Indirect) Weightage for Total Attainment Direct = 98%; Weightage for CO Attainment Indirect = 02%

Faculty Name & Signature:	Shilpa -  Vasudev - 	HOD Signature:	
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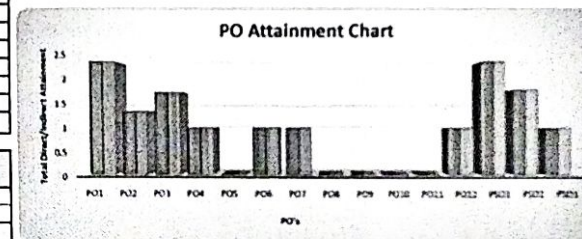
PROGRAMME OUTCOME & PROGRAMME SPECIFIC OUTCOME ASSESSMENT MATRIX
Alva's Institute of Engineering and Technology, Moodbidri
Department of Computer Science and Engineering

Department of Computer Science and Engineering															
Academic Year:		2018-2019													
Course Name:		Analog and Digital Electronics													
Course Code:		17CS32													
Faculty Name:		Ms. Shilpa & Mr. Vasudev Shahapur													
CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
17CS32.1	2	1											2	1	
17CS32.2	2	1	2	1									2	2	1
17CS32.3	3		2	1		1	1						3	2	1
17CS32.4	3	2	1	1		1	1					1	3	2	1
17CS32.5	2		2										2	2	
17CS32.6															
AVG	2.4	1.34	1.75	1		1	1					1	2.4	1.8	1

Key Words (POs)	Apply Knowledge	Solve Problems	Design/Development of Solution	Conduct Investigation	Use Modern Tools	Engineer and Society	Environment and Sustainability	Professional Ethics	Individual and Team Work	Communicate Effectively	Project Management and Finance	Life-long Learning	PO1	PO2	PO3
17CS32 Direct (D)	2.4	1.34	1.75	1		1	1					1	2.4	1.8	1
17CS32 Indirect (I)	2.4	1.34	1.75	1		1	1					1	2.4	1.8	1
Attainment Level	2.4	1.34	1.75	1		1	1					1	2.4	1.8	1

PO Attainment Calculation Direct																
COs	CO Attainment Grade	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
17CS32.1	3.00	2	1	0	0	0	0	0	0	0	0	0	0	2	1	0
17CS32.2	3	2	1	2	1	0	0	0	0	0	0	0	0	2	2	1
17CS32.3	3	3	0	2	1	0	1	1	0	0	0	0	0	3	2	1
17CS32.4	3	3	2	1	1	0	1	1	0	0	0	0	1	3	2	1
17CS32.5	3	2	0	2	0	0	0	0	0	0	0	0	0	2	2	0
17CS32.6																
	Weighted Sum -->	12	4	7	3	0	2	2	0	0	0	0	1	12	9	3
	Max Weight -->	12	4	7	3	0	2	2	0	0	0	0	1	12	9	3
PO Attainment in percentage		100.00	100.00	100.00	100.00	0.00	100.00	100.00	0.00	0.00	0.00	0.00	100.00	100.00	100.00	100.00
	PO Attained Grade	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
		2.4	1.34	1.75	1		1	1					1	2.4	1.8	1

PO Attainment Calculation Indirect																
COs	CO Attainment Grade	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
17CS32.1	3	2	1	0	0	0	0	0	0	0	0	0	0	2	1	0
17CS32.2	3	2	1	2	1	0	0	0	0	0	0	0	0	2	2	1
17CS32.3	3	3	0	2	1	0	1	1	0	0	0	0	0	3	2	1
17CS32.4	3	3	2	1	1	0	1	1	0	0	0	0	0	3	2	1
17CS32.5	3	2	0	2	0	0	0	0	0	0	0	0	0	2	2	0
17CS32.6																
	Weighted Sum -->	12	4	7	3	0	2	2	0	0	0	0	1	12	9	3
	Max Weight -->	12	4	7	3	0	2	2	0	0	0	0	1	12	9	3
PO Attainment in percentage		100.00	100.00	100.00	100.00	0.00	100.00	100.00	0.00	0.00	0.00	0.00	100.00	100.00	100.00	100.00
	PO Attained Grade	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
		2.4	1.34	1.75	1		1	1					1	2.4	1.8	1



Faculty Name & Signature: Shilpa - AS
Vasudev - AS

HOD Signature: [Signature]

ALVA'S INSTITUTE OF ENGINEERING AND TECHNOLOGY

MIJAR, MOODBIDRI - 574 225

Class : III sem 'A' sec
Subject : Analog and Digital Electronics
No. of Classes held :

ATTENDANCE CUM INTERNAL

Subject : Analog and Digital Electronics

No. of Classes held :			Date / Month																														
Sl. No.	U.S.N.	Name	1/8	2/8	3/8	3/8	4/8	4/8	08/8	09/8	10/8	10/8	11/8	11/8	12/8	12/8	21/8	21/8	22/8	22/8	23/8	23/8	24/8	24/8	25/8	25/8	26/8	26/8	27/8	27/8	11/8	12/8	
1	HALITCS050	KIRAN A S							1	2	3	4	5	6	7	A	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
2	HALITCS047	MADHUSHREE R	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	A	24	25	26	27	A	28	
3	HALITCS078	HARSHITH S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
4	HALITCS114	THOKCHOM SANTIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	A	A	22	23	24	25	26	27	28	
5	HALITCS002	AJEYASHREE K	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	A	24	25	26	27	28	29	
6	HALITCS003	AKSHAT KHADELWAL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	A	24	25	26	27	28	29	
7	HALITCS004	AKSHATA NARAYANA H	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
8	HALITCS005	AMRUTHA M	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
9	HALITCS006	ANILKUMAR B N	1	2	3	A	A	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
10	HALITCS007	ANUSHA	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
11	HALITCS008	ANVITHA POOJARY	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
12	HALITCS009	ANVITHA U	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
13	HALITCS010	APEKSHA RATENDRA	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
14	HALITCS011	APOORVA H P	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
15	HALITCS012	APOORVA K N	1	A	2	3	A	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	A	A	
16	HALITCS013	ARUNA K	1	2	3	A	A	4	5	6	7	8	A	A	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
17	HALITCS015	ASHA RUDRAPPA T	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
18	HALITCS016	ASHIKA	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
19	HALITCS017	ASHWINI	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
20	HALITCS018	ASHWINI SHEKARAPPA	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
21	HALITCS019	BHRAMARI P SHETTY	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
22	HALITCS020	CHANDANA PATIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	A	A	24	25	26	27	28	
23	HALITCS021	CHETANA H	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	A	A	24	25	26	27	28	
24	HALITCS022	CHETHANA J	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	A	A	23	24	25	26	27	A	
25	HALITCS024	D JASMINE JOYLINE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	A	21	22	23	24	25	26	27	28	29	
26	HALITCS025	DATTA KIRAN A B	1	2	3	4	5	6	7	8	9	10	11	12	13	14	A	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
27	HALITCS027	DHANYA BHAT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
28	HALITCS028	DHEERAT KRISHNA	1	2	A	A	3	4	5	6	7	A	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
29	HALITCS029	DSOUZA ELSTON R	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
30	HALITCS030	GAYATRI V KAMAT	1	2	3	4	5	6	7	8	9	A	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
Staff Initials																																	

Sl. No.	No. of Class Attended	% of Attendance	Internal Assessment (25)			Average Marks
			I	II	III	
60	60	86%	9	7	15	20
61	61	96%	10	17	14	23
62	70	100%	16	28	19	31
63	66	94%	20	16	17	27
64	68	97%	22	25	28	35
65	68	91%	28	24	29	34
66	68	91%	27	30	27	38
67	69	99%	24	29	30	34
68	65	93%	14	16	14	24
69	70	100%	26	30	30	39
70	70	100%	28	29	29	39
71	69	99%	20	29	25	34
72	70	100%	24	27	28	37
73	67	96%	20	23	29	34
74	65	93%	26	28	25	34
75	64	91%	24	18	25	32
76	69	99%	29	26	29	38
77	69	99%	16	20	26	31
78	70	100%	30	29	29	40
79	68	97%	18	22	25	32
80	68	97%	28	26	30	37
81	65	93%	16	20	16	28
82	66	94%	16	22	22	29
83	66	94%	14	21	16	26
84	69	99%	29	30	29	40
85	66	94%	23	21	24	33
86	70	100%	27	27	23	36
87	64	91%	16	16	14	25
88	69	99%	25	29	30	38
89	66	94%	11	20	16	25
90						

ALVA'S INSTITUTE OF ENGINEERING AND TECHNOLOGY

MIJAMOODBIDRI - 574 225

Class : III sem 'A' sec
Subject : Analog and Digital Electronics
No. of Classes held :

Subject :

ents
dence

Date / Month			18	2
Sl. No.	U.S.N.	Name	1	2
1	4AL15C050	KIRAN A S		
2	4AL16C047	MADHUSHREE R		
3	4AL16C048	HARSHITH S		
4	4AL16C114	THOKCHOM SANTIT		
5	4AL17C002	AJEYASHREE K		
6	4AL17C003	AKSHAT KHADELWAL		
7	4AL17C004	AKSHATA NARAYANA H		
8	4AL17C005	AMRUTHA M		
9	4AL17C006	ANILKUMAR B N		
10	4AL17C007	ANUSHA		
11	4AL17C008	ANVITHA POOJARY		
12	4AL17C009	ANVITHA U		
13	4AL17C010	APEKSHA RAJENDRA		
14	4AL17C011	APOORVA HP		
15	4AL17C012	APOORVA K N		
16	4AL17C013	ARUNA K		
17	4AL17C015	ASHA RUDRAPPA T		
18	4AL17C016	ASHIKA		
19	4AL17C017	ASHWINI		
20	4AL17C018	ASHWINI SHEKARAPPA		
21	4AL17C019	BHRAMARI P SHETTY		
22	4AL17C020	CHANDANA PATIL		
23	4AL17C021	CHETANA H		
24	4AL17C022	CHETHANA J		
25	4AL17C024	D JASMINE JOYLINE		
26	4AL17C025	DATTA KIRAN A B		
27	4AL17C027	DHANYA BHAT		
28	4AL17C028	DHEERAT KRISHNA		
29	4AL17C029	DSOINZA ELSTON R		
30	4AL17C030	GAYATRI V KAMAT		
Staff Initials				

1/13	1/14	2/13	2/14	2/15	2/16	2/17	2/18	2/19	2/20	2/21	2/22	2/23	2/24	2/25	2/26	2/27	2/28	2/29	2/30	3/1	3/2	3/3	3/4	3/5	3/6	3/7	3/8	3/9	3/10	3/11	3/12	3/13	3/14	3/15	3/16	3/17	3/18	3/19	3/20	3/21	3/22	3/23	3/24	3/25	3/26	3/27	3/28	3/29	3/30	3/31	4/1	4/2	4/3	4/4	4/5	4/6	4/7	4/8	4/9	4/10	4/11	4/12	4/13	4/14	4/15	4/16	4/17	4/18	4/19	4/20	4/21	4/22	4/23	4/24	4/25	4/26	4/27	4/28	4/29	4/30	4/31	5/1	5/2	5/3	5/4	5/5	5/6	5/7	5/8	5/9	5/10	5/11	5/12	5/13	5/14	5/15	5/16	5/17	5/18	5/19	5/20	5/21	5/22	5/23	5/24	5/25	5/26	5/27	5/28	5/29	5/30	5/31	6/1	6/2	6/3	6/4	6/5	6/6	6/7	6/8	6/9	6/10	6/11	6/12	6/13	6/14	6/15	6/16	6/17	6/18	6/19	6/20	6/21	6/22	6/23	6/24	6/25	6/26	6/27	6/28	6/29	6/30	6/31	7/1	7/2	7/3	7/4	7/5	7/6	7/7	7/8	7/9	7/10	7/11	7/12	7/13	7/14	7/15	7/16	7/17	7/18	7/19	7/20	7/21	7/22	7/23	7/24	7/25	7/26	7/27	7/28	7/29	7/30	7/31	8/1	8/2	8/3	8/4	8/5	8/6	8/7	8/8	8/9	8/10	8/11	8/12	8/13	8/14	8/15	8/16	8/17	8/18	8/19	8/20	8/21	8/22	8/23	8/24	8/25	8/26	8/27	8/28	8/29	8/30	8/31	9/1	9/2	9/3	9/4	9/5	9/6	9/7	9/8	9/9	9/10	9/11	9/12	9/13	9/14	9/15	9/16	9/17	9/18	9/19	9/20	9/21	9/22	9/23	9/24	9/25	9/26	9/27	9/28	9/29	9/30	9/31	10/1	10/2	10/3	10/4	10/5	10/6	10/7	10/8	10/9	10/10	10/11	10/12	10/13	10/14	10/15	10/16	10/17	10/18	10/19	10/20	10/21	10/22	10/23	10/24	10/25	10/26	10/27	10/28	10/29	10/30	10/31	11/1	11/2	11/3	11/4	11/5	11/6	11/7	11/8	11/9	11/10	11/11	11/12	11/13	11/14	11/15	11/16	11/17	11/18	11/19	11/20	11/21	11/22	11/23	11/24	11/25	11/26	11/27	11/28	11/29	11/30	11/31	12/1	12/2	12/3	12/4	12/5	12/6	12/7	12/8	12/9	12/10	12/11	12/12	12/13	12/14	12/15	12/16	12/17	12/18	12/19	12/20	12/21	12/22	12/23	12/24	12/25	12/26	12/27	12/28	12/29	12/30	12/31	13/1	13/2	13/3	13/4	13/5	13/6	13/7	13/8	13/9	13/10	13/11	13/12	13/13	13/14	13/15	13/16	13/17	13/18	13/19	13/20	13/21	13/22	13/23	13/24	13/25	13/26	13/27	13/28	13/29	13/30	13/31	14/1	14/2	14/3	14/4	14/5	14/6	14/7	14/8	14/9	14/10	14/11	14/12	14/13	14/14	14/15	14/16	14/17	14/18	14/19	14/20	14/21	14/22	14/23	14/24	14/25	14/26	14/27	14/28	14/29	14/30	14/31	15/1	15/2	15/3	15/4	15/5	15/6	15/7	15/8	15/9	15/10	15/11	15/12	15/13	15/14	15/15	15/16	15/17	15/18	15/19	15/20	15/21	15/22	15/23	15/24	15/25	15/26	15/27	15/28	15/29	15/30	15/31	16/1	16/2	16/3	16/4	16/5	16/6	16/7	16/8	16/9	16/10	16/11	16/12	16/13	16/14	16/15	16/16	16/17	16/18	16/19	16/20	16/21	16/22	16/23	16/24	16/25	16/26	16/27	16/28	16/29	16/30	16/31	17/1	17/2	17/3	17/4	17/5	17/6	17/7	17/8	17/9	17/10	17/11	17/12	17/13	17/14	17/15	17/16	17/17	17/18	17/19	17/20	17/21	17/22	17/23	17/24	17/25	17/26	17/27	17/28	17/29	17/30	17/31	18/1	18/2	18/3	18/4	18/5	18/6	18/7	18/8	18/9	18/10	18/11	18/12	18/13	18/14	18/15	18/16	18/17	18/18	18/19	18/20	18/21	18/22	18/23	18/24	18/25	18/26	18/27	18/28	18/29	18/30	18/31	19/1	19/2	19/3	19/4	19/5	19/6	19/7	19/8	19/9	19/10	19/11	19/12	19/13	19/14	19/15	19/16	19/17	19/18	19/19	19/20	19/21	19/22	19/23	19/24	19/25	19/26	19/27	19/28	19/29	19/30	19/31	20/1	20/2	20/3	20/4	20/5	20/6	20/7	20/8	20/9	20/10	20/11	20/12	20/13	20/14	20/15	20/16	20/17	20/18	20/19	20/20	20/21	20/22	20/23	20/24	20/25	20/26	20/27	20/28	20/29	20/30	20/31	21/1	21/2	21/3	21/4	21/5	21/6	21/7	21/8	21/9	21/10	21/11	21/12	21/13	21/14	21/15	21/16	21/17	21/18	21/19	21/20	21/21	21/22	21/23	21/24	21/25	21/26	21/27	21/28	21/29	21/30	21/31	22/1	22/2	22/3	22/4	22/5	22/6	22/7	22/8	22/9	22/10	22/11	22/12	22/13	22/14	22/15	22/16	22/17	22/18	22/19	22/20	22/21	22/22	22/23	22/24	22/25	22/26	22/27	22/28	22/29	22/30	22/31	23/1	23/2	23/3	23/4	23/5	23/6	23/7	23/8	23/9	23/10	23/11	23/12	23/13	23/14	23/15	23/16	23/17	23/18	23/19	23/20	23/21	23/22	23/23	23/24	23/25	23/26	23/27	23/28	23/29	23/30	23/31	24/1	24/2	24/3	24/4	24/5	24/6	24/7	24/8	24/9	24/10	24/11	24/12	24/13	24/14	24/15	24/16	24/17	24/18	24/19	24/20	24/21	24/22	24/23	24/24	24/25	24/26	24/27	24/28	24/29	24/30	24/31	25/1	25/2	25/3	25/4	25/5	25/6	25/7	25/8	25/9	25/10	25/11	25/12	25/13	25/14	25/15	25/16	25/17	25/18	25/19	25/20	25/21	25/22	25/23	25/24	25/25	25/26	25/27	25/28	25/29	25/30	25/31	26/1	26/2	26/3	26/4	26/5	26/6	26/7	26/8	26/9	26/10	26/11	26/12	26/13	26/14	26/15	26/16	26/17	26/18	26/19	26/20	26/21	26/22	26/23	26/24	26/25	26/26	26/27	26/28	26/29	26/30	26/31	27/1	27/2	27/3	27/4	27/5	27/6	27/7	27/8	27/9	27/10	27/11	27/12	27/13	27/14	27/15	27/16	27/17	27/18	27/19	27/20	27/21	27/22	27/23	27/24	27/25	27/26	27/27	27/28	27/29	27/30	27/31	28/1	28/2	28/3	28/4	28/5	28/6	28/7	28/8	28/9	28/10	28/11	28/12	28/13	28/14	28/15	28/16	28/17	28/18	28/19	28/20	28/21	28/22	28/23	28/24	28/25	28/26	28/27	28/28	28/29	28/30	28/31	29/1	29/2	29/3	29/4	29/5	29/6	29/7	29/8	29/9	29/10	29/11	29/12	29/13	29/14	29/15	29/16	29/17	29/18	29/19	29/20	29/21	29/22	29/23	29/24	29/25	29/26	29/27	29/28	29/29	29/30	29/31	30/1	30/2	30/3	30/4	30/5	30/6	30/7	30/8	30/9	30/10	30/11	30/12	30/13	30/14	30/15	30/16	30/17	30/18	30/19	30/20	30/21	30/22	30/23	30/24	30/25	30/26	30/27	30/28	30/29	30/30	30/31	31/1	31/2	31/3	31/4	31/5	31/6	31/7	31/8	31/9	31/10	31/11	31/12	31/13	31/14	31/15	31/16	31/17	31/18	31/19	31/20	31/21	31/22	31/23	31/24	31/25	31/26	31/27	31/28	31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ALVA'S INSTITUTE OF ENGINEERING AND TECHNOLOGY

MIJAL MOODBIDRI - 574 225

ASSESSMENT STATEMENT

Class : 311 Ann 'A' BRC
Subject : Analog and Digital Electronics
No. of Classes held : 1

Signature of students
Less than 75% attendance

Date / Month			Total Class Conducted		No. of Class Attended	% of Attendance	Internal Assessment (25)			Average Marks																												
Sl. No	USN	Name	I	II			III																															
1	HALITCS005	KIRAN A S	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	12	24	36	48	60	86%	9	7	15	20	
2	HALITCS004	MADHUSHREE R	58	59	60	61	62	63	64	65	66	67												14	9	23							67	96%	10	17	14	23
3	HALITCS008	HARSHITH S	61	62	63	64	65	66	67	68	69	70												21	10	31							70	100%	16	28	19	31
4	HALITCS114	THOKCHOM SANJIT	57	58	59	60	61	62	63	64	65	66												18	9	27							66	94%	20	16	17	27
5	HALITCS002	AJEYASHREE K	59	60	61	62	63	64	65	66	67	68												25	10	35							68	97%	22	25	28	35
6	HALITCS003	AKSHAT KHANDLWAL	59	60	61	62	63	64	65	66	67	68												27	10	37							68	97%	28	24	29	37
7	HALITCS004	AKSHATA NARAYANA H	59	60	61	62	63	64	65	66	67	68												28	10	38							68	97%	27	30	27	38
8	HALITCS005	AMRUTHA M	60	61	62	63	64	65	66	67	68	69												28	9	37							69	99%	24	29	30	37
9	HALITCS006	ANILKUMAR B N	56	57	58	59	60	61	62	63	64	65												15	9	24							65	93%	14	16	14	24
10	HALITCS007	ANUSHA	61	62	63	64	65	66	67	68	69	70												29	10	39							70	100%	26	30	30	39
11	HALITCS008	ANVITHA POOJARY	61	62	63	64	65	66	67	68	69	70												29	10	39							70	100%	28	29	29	39
12	HALITCS009	ANVITHA U	60	61	62	63	64	65	66	67	68	69												25	9	34							69	99%	20	29	25	34
13	HALITCS010	APEKSHA RAJENDRA	61	62	63	64	65	66	67	68	69	70												27	10	37							70	100%	24	27	28	37
14	HALITCS011	APOORVA HP	58	59	60	61	62	63	64	65	66	67												24	10	34							67	96%	20	23	29	34
15	HALITCS012	APOORVA KN	56	57	58	59	60	61	62	63	64	65												27	10	37							65	93%	26	28	25	37
16	HALITCS013	ARUNA K	55	56	57	58	59	60	61	62	63	64												23	9	32							64	91%	24	18	25	32
17	HALITCS015	ASHA RUDRAPPA T	60	61	62	63	64	65	66	67	68	69												28	10	38							69	99%	29	26	29	38
18	HALITCS016	ASHIKA	60	61	62	63	64	65	66	67	68	69												21	10	31							69	99%	16	20	26	31
19	HALITCS014	ASHWINI	61	62	63	64	65	66	67	68	69	70												30	10	40							70	100%	30	29	29	40
20	HALITCS018	ASHWINI SHEKARAPPA	59	60	61	62	63	64	65	66	67	68												22	10	32							68	97%	18	22	25	32
21	HALITCS019	BHRAMARI P SHETTY	59	60	61	62	63	64	65	66	67	68												28	9	37							68	97%	28	26	30	37
22	HALITCS020	CHANDANA PATIL	56	57	58	59	60	61	62	63	64	65												18	10	28							65	93%	16	20	16	28
23	HALITCS021	CHETANA H	57	58	59	60	61	62	63	64	65	66												20	9	29							66	94%	16	22	22	29
24	HALITCS022	CHETHANA J	57	58	59	60	61	62	63	64	65	66												17	9	26							66	94%	14	21	16	26
25	HALITCS024	D JASMINE JOYLINE	60	61	62	63	64	65	66	67	68	69												30	10	40							69	99%	29	30	29	40
26	HALITCS025	DATTA KIRAN A B	57	58	59	60	61	62	63	64	65	66												23	10	33							66	94%	23	21	24	33
27	HALITCS027	DHANYA BHAT	61	62	63	64	65	66	67	68	69	70												26	10	36							70	100%	27	27	23	36
28	HALITCS028	DHEEPAI KRISHNA	55	56	57	58	59	60	61	62	63	64												16	9	25							64	91%	16	16	14	25
29	HALITCS029	DSOUZA ELSTON R	60	61	62	63	64	65	66	67	68	69												28	10	38							69	99%	25	29	30	38
30	HALITCS030	GAYATRI V KAMAT	57	58	59	60	61	62	63	64	65	66												16	9	25							66	94%	11	20	16	25
Staff Initials			55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90

ALVA'S INSTITUTE OF ENGINEERING AND TECHNOLOGY

MIJARI, MOODBIDRI - 574 225

ATTENDANCE CUM INTERNAL

Class : 111 Sem 'A' Sec

Subject : Analog and Digital Electronics

No. of Classes held :

Subject : Analog and Digital Electronics

Sl. No.	U.S.N.	Name	Date / Month																													
			1/8	2/8	3/8	4/8	5/8	6/8	7/8	8/8	9/8	10/8	11/8	12/8	13/8	14/8	15/8	16/8	17/8	18/8	19/8	20/8	21/8	22/8	23/8	24/8	25/8	26/8	27/8	28/8	29/8	30/8
1	HALITCS031	GOWDA ROSHNI S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
2	HALITCS032	HARSHITH C P	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
3	HALITCS033	HEMALATHA S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
4	HALITCS034	JAGATH HAREN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
5	HALITCS035	JAYALAKSHMI M	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
6	HALITCS036	JAYRAJ CHIRAG KUMAR	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
7	HALITCS037	JOHN ALSTEN TAURO	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
8	HALITCS038	K THIRSHUL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
9	HALITCS039	KANAKA B S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
10	HALITCS040	KAYANA V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
11	HALITCS041	KAYYA	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
12	HALITCS042	KAYYA R SHETTY	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
13	HALITCS044	KOUSHIK S N	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
14	HALITCS045	LATHIK MOGER	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
15	HALITCS046	LKITHA M	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
16	HALITCS047	SUCHITHRA HEGGADE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
17	HALITCS048	MADAN G GUDIGAR	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
18	HALITCS049	MADAN GOWDA V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
19	HALITCS050	MHASKE POOJA S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
20	HALITCS051	MAHEK SABHA	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
21	HALITCS052	NAGASHREE ARUN M	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
22	HALITCS053	NAIK NAYANA G	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
23	HALITCS054	NANDITHA R SHETTY	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
24	HALITCS055	NETRA SURESH G	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
25	HALITCS056	PALLAVI	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
26	HALITCS057	PAVANA P	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
27	HALITCS059	PRAJNA	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
28	HALITCS096	SOUNDARYA R	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
29	HALITCS098	SPOORTHI BALAJI	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
30	HALITCS097	SPOORTHI M S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Staff Initials			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30

Sl. No.	No. of Class Attended	% of Attendance	Internal Assessment (25)			Average Marks
			I	II	III	
68	97%	16	17	29	31	
65	93%	16	20	16	24	
65	93%	14	27	26	33	
70	100%	30	28	30	40	
68	97%	28	28	23	37	
68	97%	24	25	29	36	
69	99%	27	29	22	36	
70	100%	29	30	29	40	
69	99%	17	24	30	34	
64	91%	15	21	27	30	
69	99%	19	25	25	33	
70	100%	19	18	20	29	
65	93%	15	20	20	28	
66	94%	14	23	24	30	
66	94%	22	17	20	29	
70	100%	21	23	25	32	
68	97%	26	27	28	37	
62	87%	9	20	8	21	
69	99%	22	24	30	36	
69	99%	16	22	19	29	
70	100%	26	27	30	38	
64	91%	30	30	28	40	
69	99%	27	26	29	38	
65	93%	29	28	30	39	
70	100%	26	21	28	38	
68	97%	11	22	25	29	
69	99%	22	25	22	32	
67	96%	18	21	20	31	
66	94%	21	20	26	26	
66	94%	15	21	15	33	
66	94%	15	21	15	33	

Class : III Sem 'A' sec

Subject : Analog and Digital Electron

No. of Classes held :

Subject :

		Date / Month	1st
Sl No.	USN	Name	1
1	HALITCS031	GOWDA ROSHNI S	1
2	HALITCS032	HARSHITH C P	1
3	HALITCS033	HEMALATHA S	1
4	HALITCS034	JAGATH HAREN	1
5	HALITCS035	JAYALAKSHMI M	1
6	HALITCS036	JAYRAT CHIRAGKUMAR	1
7	HALITCS037	JOHN ALSTEN TAURO	1
8	HALITCS038	K THIRSHUL	1
9	HALITCS039	KANAKA B S	1
10	HALITCS040	KAYANA V	1
11	HALITCS041	KAVYA	1
12	HALITCS042	KAVYA R SHETTY	1
13	HALITCS043	KOUSHIK S N	1
14	HALITCS045	LATHIK MOGER	1
15	HALITCS046	LKITHA M	1
16	HALITCS047	SUCHITHRA HEGGADE	1
17	HALITCS048	MADAN G GUDIGAR	1
18	HALITCS049	MADAN GOWDA V	1
19	HALITCS050	MHASKA POOTA S	1
20	HALITCS051	MAHEK SABHA	1
21	HALITCS052	NAGASHREE ARUN M	1
22	HALITCS053	NAIK NAYANA G	A
23	HALITCS054	NANDITHA R SHETTY	1
24	HALITCS055	NETRA SURESH G	1
25	HALITCS056	PALLAVI	1
26	HALITCS057	PAVAN P	1
27	HALITCS058	PRAJNA	1
28	HALITCS059	SOUNDARYA R	1
29	HALITCS060	SPOORTHY BALAJI	A
30	HALITCS061	SPOORTHY M S	1
Staff Initials			

Sl No.	No. of Class Attended	% of Attendance	Internal Assessment (25)			Average Marks
			I	II	III	
60						
	68	97%	16	17	29	31
	65	93%	16	20	16	27
	65	93%	14	24	26	33
	70	100%	30	28	30	40
	68	97%	28	28	23	37
	68	97%	24	25	29	36
	69	99%	27	29	22	36
	70	100%	29	30	29	40
	69	99%	17	24	30	34
	64	91%	15	21	27	30
	69	99%	19	25	25	33
	70	100%	19	18	20	29
	65	93%	15	20	20	28
	66	94%	14	23	24	30
	66	94%	22	17	20	29
	70	100%	21	23	25	32
	68	97%	26	27	28	37
	62	87%	9	20	8	21
	69	99%	22	24	30	36
	69	99%	16	22	19	29
	70	100%	26	27	30	38
	64	91%	30	30	28	40
	69	99%	27	26	29	38
	65	93%	29	28	30	39
	70	100%	26	21	28	38
	68	97%	11	22	25	29
	69	99%	22	25	22	32
	67	96%	18	21	20	31
	66	94%	21	20	26	26
	66	94%	15	21	15	33

Class : III Sem 'A' Sec

Subject : Analog and Digital Electronics

No. of Classes held :

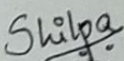
ASSESSMENT STATEMENT

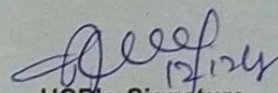
Signature of students
Less than 75% attendance

Date / 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AIET	INTERNAL EXAM RESULT ANALYSIS					Format No.	ACD 12	
						Issue No.	01	
						Rev. No.	00	
Department	Computer Science And Engineering					Semester	3 rd 'A' sec	
						Subject Code	17CS32	
Total No. of Students	61					Academic Year	2018 - 19	
Test	Date	Number of Students				Signature		Remarks
		Attended	0-13	14-20	21-26	Faculty	HOD	
T ₁	17/9/18	61	05	56				
T ₂	25/10/18	61	01	60				
T ₃	26/10/18	61	01	60				
T ₄								
T ₅								


 Signature of Staff in - charge


 HOD's Signature