COMPUTER NETWORKS LAB

Course Code : **18ECL76**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:

- Choose suitable tools to model a network and understand the protocols at various OSI reference levels.
- Design a suitable network and simulate using a Network simulator tool.
- Simulate the networking concepts and protocols using C/C++ programming.
- Model the networks for different configurations and analyze the results.

Laboratory Experiments

PART-A: Simulation experiments using NS2/ NS3/ OPNET/ NCTUNS/ NetSim/QualNet or any other equivalent tool

1. Implement a point to point network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.
2. Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent by TCP/UDP.
3. Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.
4. Implement Ethernet LAN using n nodes and assign multiple traffic to the nodes and obtain congestion window for different sources/ destinations.
5. Implement ESS with transmission nodes in Wireless LAN and obtain the performance parameters.
6. Implementation of Link state routing algorithm.

PART-B: Implement the following in C/C++

1. Write a program for a HLDC frame to perform the following.
   i) Bit stuffing
   ii) Character stuffing.
2. Write a program for distance vector algorithm to find suitable path for transmission.
3. Implement Dijkstra's algorithm to compute the shortest routing path.

4. For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify the program for the cases
   a. Without error
   b. With error
5. Implementation of Stop and Wait Protocol and Sliding Window Protocol
6. Write a program for congestion control using leaky bucket algorithm.

Course outcomes: On the completion of this laboratory course, the students will be able to:

1. Choose suitable tools to model a network.
2. Use the network simulator for learning and practice of networking algorithms.
3. Illustrate the operations of network protocols and algorithms using C programming.
4. Simulate the network with different configurations to measure the performance parameters.
5. Implement the data link and routing protocols using C programming.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination one question from software and one question from hardware or only one hardware experiments based on the complexity to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

SEMESTER – VII
COMPUTER NETWORKS

Course Code	: 18EC71	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs/module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand the layering architecture of OSI reference model and TCP/IP protocol suite.
- Understand the protocols associated with each layer.
- Learn the different networking architectures and their representations.
- Learn the functions and services associated with each layer.

Module-1

Introduction: Data communication: Components, Data representation, Data flow, Networks: Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet.
(1.1,1.2, 1.3(1.3.1to 1.3.4 of Text)
Network Models: Protocol Layering: Scenarios, Principles, Logical Connections, TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP.
(2.1, 2.2, 2.3 of Text) **L1, L2**

Module-2

Data-Link Layer: Introduction: Nodes and Links, Services, Two Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services: Framing, Flow and Error Control, Data Link Layer Protocols: Simple Protocol, Stop and Wait protocol, Piggybacking.
(9.1, 9.2(9.2.1, 9.2.2), 11.1, 11.2of Text)
Media Access Control: Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA.**(12.1 of Text)**
Wired and Wireless LANs: Ethernet Protocol, Standard Ethernet. Introduction to wireless LAN: Architectural Comparison, Characteristics, Access Control.
(13.1, 13.2(13.2.1 to 13.2.5), 15.1 of Text) **L1,L2, L3**

Module-3

Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution, Forwarding of IP Packets: Based on destination Address and Label.

(18.1, 18.2, 18.4, 18.5.1, 18.5.2 of Text)

Network Layer Protocols: Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams. **(19.1of Text).**

Unicast Routing: Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing.

(20.1, 20.2of Text) **L1,L2, L3**

Module-4

Transport Layer: Introduction: Transport Layer Services, Connectionless and Connection oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-Back-N Protocol, Selective repeat protocol. **(23.1, 23.2.1, 23.2.2, 23.2.3, 23.2.4 of Text)**

Transport-Layer Protocols in the Internet:

User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Flow control, Error control, TCP congestion control.

(24.2, 24.3.1, 24.3.2, 24.3.3, 24.3.4, 24.3.5, 24.3.6, 24.3.7, 24.3.8, 24.3.9 of Text) **L1,L2, L3**

Module-5

Application Layer: Introduction: providing services, Application- layer paradigms, Standard Client –Server Protocols: World wide web, Hyper Text Transfer Protocol, FTP: Two connections, Control Connection, Data Connection, Electronic Mail: Architecture, Wed Based Mail, Telnet: Local versus remote logging.Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS, security of DNS.

(25.1, 26.1, 26.2, 26.3, 26.4, 26.6 of Text) **L1, L2**

Course Outcomes: At the end of the course, the students will be able to:

1. Understand the concepts of networking.
2. Describe the various networking architectures.
3. Identify the protocols and services of different layers.
4. Distinguish the basic network configurations and standards associated with each network.
5. Analyze a simple network and measure its parameters.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOK:

- Behrouz A Forouzan, "Data Communications and Networking", 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.

REFERENCE BOOKS:

1. James J Kurose, Keith W Ross, "Computer Networks", Pearson Education.
2. Wayne Tomasi, "Introduction to Data Communication and Networking", Pearson Education.
3. Andrew S Tanenbaum, "Computer Networks", Prentice Hall.
4. William Stallings, "Data and Computer Communications", Prentice Hall.

DSP ALGORITHMS and ARCHITECTURE

Course Code	: 18EC734	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Figure out the knowledge and concepts of digital signal processing techniques.
- Understand the computational building blocks of DSP processors and its speed issues.
- Understand the various addressing modes, peripherals, interrupts and pipelining structure of TMS320C54xx processor.
- Learn how to interface the external devices to TMS320C54xx processor in various modes.
- Understand basic DSP algorithms with their implementation.

Module -1

Introduction to Digital Signal Processing:

Introduction, A Digital Signal – Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation.

Computational Accuracy in DSP Implementations:

Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementation.

L1,L2

Module -2

Architectures for Programmable Digital Signal – Processing Devices:

Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.

L1,L2

Module -3

Programmable Digital Signal Processors:

Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54XX, Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and

Programming, On – Chip Peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor.

L1,L2

Module -4

Implementation of Basic DSP Algorithms:

Introduction, The Q – notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case).

Implementation of FFT Algorithms:

Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit – Reversed Index. Generation & Implementation on the TMS32OC54xx.

L1,L2

Module -5

Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices:

Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA).

Interfacing and Applications of DSP Processors:

Introduction, Synchronous Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System.

L1,L2

Course Outcomes: At the end of this course, students would be able to:

1. Comprehend the knowledge and concepts of digital signal processing techniques.
2. Apply the knowledge of DSP computational building blocks to achieve speed in DSP architecture or processor.
3. Apply knowledge of various types of addressing modes, interrupts, peripherals and pipelining structure of TMS320C54xx processor.
4. Develop basic DSP algorithms using DSP processors.
5. Discuss about synchronous serial interface and multichannel buffered serial port (McBSP) of DSP device and demonstrate the programming of CODEC interfacing.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.

- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- "Digital Signal Processing", Avatar Singh and S. Srinivasan, Thomson Learning, 2004.

Reference Books:

1. "Digital Signal Processing: A practical approach", Ifeachor E. C., Jervis B. W Pearson-Education, PHI, 2002.
2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2nd, 2010
3. "Architectures for Digital Signal Processing", Peter Pirsch John Wiley, 2008

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination 2018 – 19
Outcome Based Education(OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2018 – 19)

VII SEMESTER

Sl. No.	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P					
1	PCC	18EC71	Computer Networks		3	--	--	03	40	60	100	3
2	PCC	18EC72	VLSI Design		3	--	--	03	40	60	100	3
3	PEC	18XX73X	Professional Elective - 2		3	--	--	03	40	60	100	3
4	PEC	18XX74X	Professional Elective - 3		3	--	--	03	40	60	100	3
5	OEC	18XX75X	Open Elective -B		3	--	--	03	40	60	100	3
6	PCC	18ECL76	Computer Networks Lab		--	2	2	03	40	60	100	2
7	PCC	18ECL77	VLSI Laboratory		--	2	2	03	40	60	100	2
8	Project	18ECP78	Project Work Phase - 1		--	--	2	--	100	--	100	1
9	Internship	--	Internship	(If not completed during the vacation of VI and VII semesters, it shall be carried out during the vacation of VII and VIII semesters)								
				TOTAL	15	4	6	21	380	420	800	20

Note: PCC: Professional core, PEC: Professional Elective.

Professional Elective - 2

Course code under 18XX73X	Course Title
18EC731	Real Time System
18EC732	Satellite Communication
18EC733	Digital Image Processing
18EC734	Data Structures using C++
18EC735	DSP Algorithms & Architecture

Professional Electives - 3

Course code under 18XX74X	Course Title
18EC741	IOT & Wireless Sensor Networks
18EC742	Automotive Electronics
18EC743	Multimedia Communication
18EC744	Cryptography
18EC745	Machine Learning

Open Elective –B

(i) 18EC751 Communication Theory (ii) 18EC752 Neural Networks

Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please refer to the list of open electives under 18XX75X).

Selection of an open elective shall not be allowed if,

- The candidate has studied the same course during the previous semesters of the programme.
- The syllabus content of open elective is similar to that of the Departmental core courses or professional electives.
- A similar course, under any category, is prescribed in the higher semesters of the programme.

Registration to electives shall be documented under the guidance of Programme Coordinator/ Advisor/Mentor.

Project work:

Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary project can be assigned to an individual student or to a group having not more than 4 students. In extraordinary cases, like the funded projects requiring students from different disciplines, the project student strength can be 5 or 6.

CIE procedure for Project Work Phase - 1:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work phase -1, shall be based on the evaluation of the project work phase -1 Report (covering Literature Survey, Problem identification, Objectives and Methodology), project presentation skill and question and answer session in the ratio 50:25:25. The marks awarded for the Project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable.

The CIE marks awarded for the project work phase -1, shall be based on the evaluation of project work phase -1 Report, project presentation skill and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

Internship: All the students admitted to III year of BE/B.Tech shall have to undergo mandatory internship of 4 weeks during the vacation of VI and VII semesters and /or VII and VIII semesters. A University examination shall be conducted during VIII semester and the prescribed credit shall be included in VIII semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

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IoT & WIRELESS SENSOR NETWORKS

Course Code	: 18EC741	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Describe the OSI Model for IoT/M2M Systems.
- Understand the architecture and design principles for device supporting IoT.
- Develop competence in programming for IoT Applications.
- Identify the uplink and downlink communication protocols which best suits the specific application of IoT / WSNs.

Module-1

Overview of Internet of Things: IoT Conceptual Framework, IoT Architectural View, Technology Behind IoT, Sources of IoT,M2M communication, Examples of IoT. Modified OSI Model for the IoT/M2M Systems, data enrichment, data consolidation and device management at IoT/M2M Gateway, web communication protocols used by connected IoT/M2M devices, Message communication protocols (CoAP-SMS, CoAP-MQ, MQTT,XMPP) for IoT/M2M devices. – Refer Chapter 1, 2 and 3 of Text 1.

L1, L2

Module-2

Architecture and Design Principles for IoT: Internet connectivity, Internet-based communication,IPv4, IPv6,6LoWPAN protocol, IP Addressing in the IoT, Application layer protocols: HTTP, HTTPS,FTP,TELNET and ports.

Data Collection, Storage and Computing using a Cloud Platform: Introduction, Cloud computing paradigm for data collection, storage and computing, Cloud service models, IoT Cloud- based data collection, storage and computing services using Nimbits. - Refer Chapter 4 and 6 of Text 1.

L1, L2

Module-3

Prototyping and Designing Software for IoT Applications: Introduction, Prototyping Embedded device software, Programming Embedded Device Arduino Platform using IDE, Reading data from sensors and devices, Devices, Gateways, Internet and Web/Cloud services software development.

Programming MQTT clients and MQTT server. Introduction to IoT privacy

and security. Vulnerabilities, security requirements and threat analysis, IoT Security Tomography and layered attacker model. - Refer Chapter 9 and 10 of Text 1. **L1, L2, L3**

Module-4

Overview of Wireless Sensor Networks:

Challenges for Wireless Sensor Networks, Enabling Technologies for Wireless Sensor Networks.

Architectures: Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes, Operating Systems and Execution Environments, Network Architecture-Sensor Network Scenarios, Optimization Goals and Figures of Merit, Design principles for WSNs, Service interfaces of WSNs Gateway Concepts. - Refer Chapter 1, 2, 3 of Text 2.

L1, L2, L3

Module-5

Communication Protocols:

Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Contention based protocols(CSMA,PAMAS), Schedule based protocols (LEACH, SMACS, TRAMA) Address and Name Management in WSNs, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing, Hierarchical networks by clustering. - Refer Chapter 4, 5, 7 and 11 of Text 2.

L1, L2, L3

Course Outcomes: At the end of the course, students will be able to:

1. Understand choice and application of IoT & M2M communication protocols.
2. Describe Cloud computing and design principles of IoT.
3. Relate to MQTT clients, MQTT server and its programming.
4. Describe the architectures and its communication protocols of WSNs.
5. Identify the uplink and downlink communication protocols associated with specific application of IOT / WSNs

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4sub questions.
- There will be 2 full questions from each module covering all the topics of the module.

- Students will have to answer 5full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Raj Kamal, "Internet of Things-Architecture and design principles", McGraw Hill Education.
2. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless Sensor Networks", John Wiley, 2005.

Reference Books:

1. Feng Zhao & Leonidas J. Guibas, "Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
2. Kazem Sohraby, Daniel Minoli, & Taieb Znati, "Wireless Sensor Networks- Technology, Protocols and Applications", John Wiley, 2007.
3. Anna Hac, "Wireless Sensor Network Designs", John Wiley, 2003.

NETWORK SECURITY

Course Code	: 18EC821	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Describe network security services and mechanisms.
- Understand Transport Level Security and Secure Socket Layer
- Know about Security concerns in Internet Protocol security
- Discuss about Intruders, Intrusion detection and Malicious Software
- Discuss about Firewalls, Firewall characteristics, Biasing and Configuration

Module-1

Attacks on Computers and Computer Security: Need for Security, Security Approaches, Principles of Security Types of Attacks.
(Chapter1-Text2) **L1, L2**

Module-2

Transport Level Security: Web Security Considerations, Secure Sockets Layer, Transport Layer Security, HTTPS, Secure Shell (SSH)
(Chapter15- Text1) **L1,L2**

Module-3

IP Security: Overview of IP Security (IPSec),IP Security Architecture, Modes of Operation, Security Associations (SA), Authentication Header (AH), Encapsulating Security Payload (ESP), Internet Key Exchange.
(Chapter19-Text1) **L1,L2**

Module-4

Intruders, Intrusion Detection.**(Chapter20-Text1)**
MALICIOUS SOFTWARE: Viruses and Related Threats, Virus Counter measures,
(Chapter21-Text1) **L1,L2**

Module-5

Firewalls: The Need for firewalls, Firewall Characteristics, Types of Firewalls, Firewall Biasing, Firewall location and configuration
(Chapter22-Text 1) **L1, L2**

Course Outcomes: After studying this course, students will be able to:

1. Explain network security services and mechanisms and explain security concepts
2. Understand the concept of Transport Level Security and Secure Socket Layer.
3. Explain Security concerns in Internet Protocol security
4. Explain Intruders, Intrusion detection and Malicious Software
5. Describe Firewalls, Firewall Characteristics, Biasing and Configuration

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOKS:

1. Cryptography and Network Security Principles and Practice , Pearson Education Inc., William Stallings, 5th Edition, 2014, ISBN: 978-81-317- 6166-3.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

REFERENCE BOOKS:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination 2018 – 19
Outcome Based Education(OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2018 – 19)

VIII SEMESTER

Sl. No	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P					
1	PCC	18EC81	Wireless and Cellular Communication		3	--	--	03	40	60	100	3
2	PEC	18XX82X	Professional Elective - 4		3	--	--	03	40	60	100	3
3	Project	18ECP83	Project Work Phase - 2		--	--	2	03	40	60	100	8
4	Seminar	18EC884	Technical Seminar		--	--	2	03	100	--	100	1
5	Internship	18EC885	Internship	Completed during the vacation/s of VI and VII semesters and /or VII and VIII semesters.)				03	40	60	100	3
				TOTAL	06	--	4	15	260	240	500	18

Note: PCC: Professional Core, PEC: Professional Elective

Professional Electives - 4

Course code under 18XX82X	Course Title
18EC821	Network Security
18EC822	Micro Electro Mechanical Systems
18EC823	Radar Engineering
18EC824	Optical Communication Networks
18EC825	Biomedical Signal Processing

Project Work

CIE procedure for Project Work Phase - 2:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work phase -2, shall be based on the evaluation of project work phase -2 Report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable.

The CIE marks awarded for the project work phase -2, shall be based on the evaluation of project work phase -2 Report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

SEE for Project Work Phase - 2:

(i) Single discipline: Contribution to the project and the performance of each group member shall be assessed individually in semester end examination (SEE) conducted at the department.

(ii) Interdisciplinary: Contribution to the project and the performance of each group member shall be assessed individually in semester end examination (SEE) conducted separately at the departments to which the student/s belong to.

Internship: Those, who have not pursued /completed the internship shall be declared as fail and have to complete during subsequent University examination after satisfying the internship requirements.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card. Activity points of the students who have earned the prescribed AICTE activity Points shall be sent the University along with the CIE marks of 8th semester. In case of students who have not satisfied the AICTE activity Points at the end of eighth semester, the column under activity Points shall be marked NSAP (Not Satisfied Activity Points).

D.V.

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VLSI DESIGN

Course Code	: 18EC72	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40(08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: The objectives of the course is to enable students to:

- Impart knowledge of MOS transistor theory and CMOS technologies
- Learn the operation principles and analysis of inverter circuits.
- Design Combinational, sequential and dynamic logic circuits as per the requirements
- Infer the operation of Semiconductors Memory circuits.
- Demonstrate the concepts of CMOS testing

Module-1

Introduction: A Brief History, MOS Transistors, CMOS Logic **(1.1 to 1.4 of TEXT2)**

MOS Transistor Theory: Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics **(2.1, 2.2, 2.4 and 2.5 of TEXT2).**, **L1, L2**

Module-2

Fabrication: CMOS Fabrication and Layout, VLSI Design Flow, Introduction, CMOS Technologies, Layout Design Rules, **(1.5 and 3.1 to 3.3 of TEXT2).**

MOSFET Scaling and Small-Geometry Effects, MOSFET Capacitances **(3.5 to 3.6 of TEXT1), L1, L2,**

Module-3

Delay: Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths **(4.1 to 4.5 of TEXT2, except sub-sections 4.3.7, 4.4.5, 4.4.6, 4.5.5 and 4.5.6).**

Combinational Circuit Design: Introduction, Circuit families **(9.1 to 9.2 of TEXT2, except subsection 9.2.4).**, **L1, L2, L3**

Module-4

Sequential Circuit Design: Introduction, Circuit Design for Latches and Flip-Flops **(10.1 and 10.3.1 to 10.3.4 of TEXT2)**

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques **(9.1, 9.2, 9.4 to 9.5 of TEXT1)**, **L1, L2, L3**

Module-5

Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM),
(10.1 to 10.3 of TEXT1)
Testing and Verification: Introduction, Logic Verification Principles, Manufacturing Test Principles, Design for testability
(15.1, 15.3, 15.5 15.6.1 to 15.6.3 of TEXT 2). L1, L2

Course outcomes: At the end of the course, the students will be able to:

1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
2. Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
3. Demonstrate ability to design Combinational, sequential and dynamic logic circuits as per the requirements
4. Interpret Memory elements along with timing considerations
5. Interpret testing and testability issues in VLSI Design

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOKS:

1. "CMOS Digital Integrated Circuits: Analysis and Design" - **Sung Mo Kang & Yosuf Leblebici,** Third Edition, Tata McGraw-Hill.
2. **"CMOS VLSI Design- A Circuits and Systems Perspective"-** Neil H. E. Weste and David Money Harris, 4th Edition, Pearson Education.

REFERENCE BOOKS:

1. Adel Sedra and K. C. Smith, "Microelectronics Circuits Theory and Applications", 6th or 7th Edition, Oxford University Press, International Version, 2009.
2. Douglas A Pucknell & Kamran Eshragian, "Basic VLSI Design", PHI 3rd Edition, (original Edition – 1994).
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.

VLSI LABORATORY

Course Code : **18ECL77**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:

- Design, model, simulate and verify CMOS digital circuits
- Design layouts and perform physical verification of CMOS digital circuits
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist
- Perform RTL-GDSII flow and understand the stages in ASIC design

Experiments can be conducted using any of the following or equivalent design tools: Cadence/Synopsis/Mentor Graphics/Microwind

Laboratory Experiments

Part – A

Analog Design

Use any VLSI design tools to carry out the experiments, use library files and technology files below 180 nm.

1.a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following:

i. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time period of 20ns and plot the input voltage and output voltage of designed inverter?

ii. From the simulation results compute tpHL, tpLH and td for all three geometrical settings of width?

iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter?

1. b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

2. a) Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 1. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.

2. b) Draw layout of NAND with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

3. a) Capture schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measures the Unity Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB.

3. b) Draw layout of common source amplifier, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

4.a) Capture schematic of two-stage operational amplifier and measure the following:

i. UGB
ii. dB bandwidth
iii. Gain margin and phase margin with and without coupling capacitance
iv. Use the op-amp in the inverting and non-inverting configuration and verify its functionality
v. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations.

4.b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in 4.a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

Part - B

Digital Design

Carry out the experiments using semicustom design flow or ASIC design flow, use technology library 180/90/45nm and below

Note: The experiments can also be carried out using FPGA design flow, it is required to set appropriate constraints in FPGA advanced synthesis options

1. Write verilog code for 4-bit up/down asynchronous reset counter and carry out the following:
   a. Verify the functionality using test bench
   b. Synthesize the design by setting area and timing constraint. Obtain

the gate level netlist, find the critical path and maximum frequency of operation. Record the area requirement in terms of number of cells required and properties of each cell in terms of driving strength, power and area requirement.

c. Perform the above for 32-bit up/down counter and identify the critical path, delay of critical path, and maximum frequency of operation, total number of cells required and total area.

2. Write verilog code for 4-bit adder and verify its functionality using test bench. Synthesize the design by setting proper constraints and obtain the net list. From the report generated identify critical path, maximum delay, total number of cells, power requirement and total area required. Change the constraints and obtain optimum synthesis results.
3. Write verilog code for UART and carry out the following:
   a. Perform functional verification using test bench
   b. Synthesize the design targeting suitable library and by setting area and timing constraints
   c. For various constrains set, tabulate the area, power and delay for the synthesized netlist
   d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints
4. Write verilog code for 32-bit ALU supporting four logical and four arithmetic operations, use case statement and if statement for ALU behavioral modeling.
   a. Perform functional verification using test bench
   b. Synthesize the design targeting suitable library by setting area and timing constraints
   c. For various constrains set, tabulate the area, power and delay for the synthesized netlist
   d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints

   Compare the synthesis results of ALU modeled using IF and CASE statements.
5. Write verilog code for Latch and Flip-flop, Synthesize the design and compare the synthesis report (D, SR, JK).
6. For the synthesized netlist carry out the following for any two above experiments:
   a. Floor planning (automatic), identify the placement of pads
   b. Placement and Routing, record the parameters such as no. of layers used for routing, flip method for placement of standard cells, placement of standard cells, routes of power and ground, and routing of standard cells
   c. Physical verification and record the LVS and DRC reports

d. Perform Back annotation and verify the functionality of the design
e. Generate GDSII and record the number of masks and its color composition

Course Outcomes: On the completion of this laboratory course, the students will be able to:

1. Design and simulate combinational and sequential digital circuits using Verilog HDL
2. Understand the Synthesis process of digital circuits using EDA tool.
3. Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list
4. Design and simulate basic CMOS circuits like inverter, common source amplifier and differential amplifiers.
5. Perform RTL-GDSII flow and understand the stages in ASIC design.

B. E. 2018 Scheme Eighth Semester Syllabus (EC)

Choice Based Credit System (CBCS) and Outcome Based Education (OBE)

SEMESTER – VIII

WIRELESS and CELLULAR COMMUNICATION

Course Code	: 18EC81	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs / Module)	Exam Hours	: 03
	CREDITS – 03		

Course Learning Objectives: This course will enable students to:

- Understand the concepts of propagation over wireless channels from a physics standpoint
- Application of Communication theory both Physical and networking to understand GSM systems that handle mobile telephony
- Application of Communication theory both Physical and networking to understand CDMA systems that handle mobile telephony.
- Application of Communication theory both Physical and networking to understand LTE-4G systems.

Module-1

Mobile Radio Propagation –

Large Scale Path Loss - Free Space Propagation Model, Relating Power to Electric Field, Three Basic Propagation Mechanisms – Reflection (Ground Reflection) , Diffraction, Scattering, Practical Link Budget,

(Text 1 - 2.2 and Ref1 - Chapter 4)

Fading and Multipath – Broadband wireless channel, Delay Spread and Coherence Bandwidth, Doppler Spread and Coherence Time, Angular spread and Coherence Distance **(Text 1 – 2.4)**

Statistical Channel Model of a Broadband Fading Channel

(Text 1 – 2.5.1)

The Cellular Concept – Cellular Concept , Analysis of Cellular Systems, Sectoring

(Text 1- 2.3) **L1, L2**

Module-2

GSM and TDMA Technology

GSM System overview – Introduction, GSM Network and System Architecture, GSM Channel Concept.

GSM System Operations – GSM Identities, System Operations –Traffic cases, GSM Infrastructure Communications (Um Interface)
(Text 2, Part1 and Part 2 of Chapter 5) **L1,L2,L3**

Module-3

CDMA Technology
CDMA System Overview – Introduction, CDMA Network and System Architecture
CDMA Basics – CDMA Channel Concepts, CDMA System (Layer 3) operations, 3G CDMA
(Text 2-Part 1, Part2 and Part 3 of Chapter 6) **L1,L2,L3**

Module-4

LTE – 4G
Key Enablers for LTE 4G – OFDM, SC-FDE, SC-FDMA, Channel Dependant Multiuser Resource Scheduling, Multi-Antenna Techniques, Flat IP Architecture, LTE Network Architecture. **(Text 1, Sec 1.4)**
Multi-Carrier Modulation – Multicarrier concepts, OFDM Basics, OFDM in LTE, Timing and Frequency Synchronization, Peak to Average Ration, SC-Frequency Domain Equalization, Computational Complexity Advantage of OFDM and SC-FDE.
(Text 1, Sec 3.1 – 3.7) **L1,L2,L3**

Module-5

LTE - 4G
OFDMA and SC-FDMA – Multiple Access for OFDM Systems, OFDMA, SCFDMA, Multiuser Diversity and Opportunistic Scheduling, OFDMA and SC-FDMA in LTE, OFDMA system Design Considerations.
(Text 1, Sec 4.1 – 4.6)
The LTE Standard – Introduction to LTE and Hierarchical Channel Structure of LTE, Downlink OFDMA Radio Resources, Uplink SC-FDMA Radio Resources.
(Text 1, Sec 6.1 – 6.4) **L1, L2,L3**

Course Outcomes: After studying this course, students will be able to:

1. Understand the Communication theory both Physical and networking associated with GSM, CDMA & LTE 4G systems.
2. Explain concepts of propagation mechanisms like Reflection, Diffraction, Scattering in wireless channels.
3. Develop a scheme for idle mode, call set up, call progress handling and call tear down in a GSM cellular network.

4. Develop a scheme for idle mode, call set up, call progress handling and call tear down in a CDMA cellular network.
5. Understand the Basic operations of Air interface in a LTE 4G system.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "Fundamentals of LTE" Arunabha Ghosh, Jan Zhang, Jefferey Andrews, Riaz Mohammed, Pearson education (Formerly Prentice Hall, Communications Engg and Emerging Technologies), ISBN-13: 978-0-13-703311-9.
2. "Introduction to Wireless Telecommunications Systems and Networks", Gary Mullet, First Edition, Cengage Learning India Pvt Ltd., 2006, ISBN - 13: 978-81-315-0559-5.

Reference Books:

1. "Wireless Communications: Principles and Practice" Theodore Rappaport, 2nd Edition, Prentice Hall Communications Engineering and Emerging Technologies Series, 2002, ISBN 0-13-042232-0.
2. LTE for UMTS Evolution to LTE-Advanced' Harri Holma and Antti Toskala, Second Edition - 2011, John Wiley & Sons, Ltd. Print ISBN: 9780470660003. 2