DSP ALGORITHMS and ARCHITECTURE

Course Code	: 18EC734	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Figure out the knowledge and concepts of digital signal processing techniques.
- Understand the computational building blocks of DSP processors and its speed issues.
- Understand the various addressing modes, peripherals, interrupts and pipelining structure of TMS320C54xx processor.
- Learn how to interface the external devices to TMS320C54xx processor in various modes.
- Understand basic DSP algorithms with their implementation.

Module -1
Introduction to Digital Signal Processing:
Introduction, A Digital Signal – Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation.
Computational Accuracy in DSP Implementations:
Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementation.

L1,L2

Module -2
Architectures for Programmable Digital Signal – Processing Devices:
Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.

L1,L2

Module -3
Programmable Digital Signal Processors:
Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54XX, Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and

Programming, On – Chip Peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor.

L1,L2

Module -4

Implementation of Basic DSP Algorithms:
Introduction, The Q – notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case).
Implementation of FFT Algorithms:
Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit – Reversed Index. Generation & Implementation on the TMS32OC54xx.

L1,L2

Module -5

Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices:
Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA).
Interfacing and Applications of DSP Processors:
Introduction, Synchronous Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System.

L1,L2

Course Outcomes: At the end of this course, students would be able to:
1. Comprehend the knowledge and concepts of digital signal processing techniques.
2. Apply the knowledge of DSP computational building blocks to achieve speed in DSP architecture or processor.
3. Apply knowledge of various types of addressing modes, interrupts, peripherals and pipelining structure of TMS320C54xx processor.
4. Develop basic DSP algorithms using DSP processors.
5. Discuss about synchronous serial interface and multichannel buffered serial port (McBSP) of DSP device and demonstrate the programming of CODEC interfacing.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.

- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
- "Digital Signal Processing", Avatar Singh and S. Srinivasan, Thomson Learning, 2004.

Reference Books:
1. "Digital Signal Processing: A practical approach", Ifeachor E. C., Jervis B. W Pearson-Education, PHI, 2002.
2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2nd, 2010
3. "Architectures for Digital Signal Processing", Peter Pirsch John Wiley, 2008