VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

VI Semester

VLSI Design and Testing			
Course Code	**21EC63**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Impart knowledge of MOS transistor theory and CMOS technology
- Learn the operation principles and analysis of inverter circuits.
- Infer the operation of Semiconductor memory circuits.
- Demonstrate the concept of CMOS testing.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Arrange visits to nearby PSUs and industries.
3. Show Video/animation films to explain the functioning of various fabrication & testing techniques.
4. Encourage collaborative (Group) Learning in the class
5. Topics will be introduced in multiple representations.
6. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction: A Brief History, MOS Transistors, CMOS Logic (1.1 to 1.4 of TEXT1)

MOS Transistor Theory: Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics (2.1, 2.2, 2.4 and 2.5 of TEXT1).

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, Videos on transistor working **Self-study topics**: MOSFET Scaling and Small-Geometry Effects **RBT Level:** L1, L2, L3

Module-2

Fabrication: CMOS Fabrication and Layout, Introduction, CMOS Technologies, Layout Design Rules, (1.5 and 3.1 to 3.3 of TEXT1).

Delay: Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths (4.1 to 4.5 of TEXT1, except sub-sections 4.3.7, 4.4.5, 4.4.6, 4.5.5 and 4.5.6).

Teaching-Learning Process	Chalk and talk method, Power point presentation, YouTube videos, Videos on fabrication **Self-study topics**: Layouts of complex design using Euler's method **RBT Level:** L1, L2, L3

Module-3

Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM) (10.1 to 10.6 of TEXT2)

Teaching-Learning	Chalk and talk method, PowerPoint Presentation, YouTube videos on Standard

Process	cell memory Design **Self-study topics**: Memory array design **RBT Level:** L1, L2, L3

Module-4

Faults in digital circuits: Failures and faults, Modelling of faults, Temporary faults

Test generation for combinational logic circuits: Fault diagnosis of digital circuits, test generation techniques for combinational circuits, Detection of multiple faults in combinational logic circuits.

(1.1 to 1.3, 2.1 to 2.3 of TEXT3)

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, videos on testing algorithms for test generation **Self-study topics**: Testable combinational logic circuits **RBT Level:** L1, L2, L3

Module-5

Test generation for sequential circuits: Testing of sequential circuits as iterative combinational circuits, state table verification, test generation based on circuits structure, functional fault models, test generation based on functional fault models.

Design of testable sequential circuits: Controllability and Observability, Adhoc design rules, design of diagnosable sequential circuits, The scan path technique, LSSD, Random Access scan technique, partial scan.

(4.1 to 4.5, 5.1 to 5.7 of TEXT3)

Teaching-Learning Process	Chalk and talk method/Power point presentation, YouTube videos **Self-study topics**: Memory testing techniques **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
2. Draw the basic gates using the stick and layout diagram with the knowledge of physical design aspects.
3. Interpret memory elements along with timing considerations.
4. Interpret testing and testability issues in combinational logic design.
5. Interpret testing and testability issues in combinational logic design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20**

Marks (duration 01 hours)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, and David Money Harris 4th Edition, Pearson Education.
2. "CMOS Digital Integrated Circuits: Analysis and Design", Sung Mo Kang & Yosuf Leblebici, Third Edition, Tata McGraw-Hill.
3. "Digital Circuit Testing and Testability", Lala Parag K, New York, Academic Press, 1997.

Reference Books:

1. "Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005.
2. "Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits", Vishwani D Agarwal, Springer, 2002.

Web links and Video Lectures (e-Resources)

- https://www.youtube.com/watch?v=oL8SKNxEaHs&list=PLLy_2iUCG87Bdulp9brz9AcvW_TnFCUmM
- https://www.youtube.com/watch?v=lRpt1fCHd8Y&list=PLCmoXVuSEVHlEJi3SwdyJ4EICffuyqpjk
- https://www.youtube.com/watch?v=yLqLD8Y4-Qc

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Model displayed for clear understanding of fabrication process of MOS transistor
- Practise session can be held to understand the significance of various layers in MOS process, with the help of coloured layouts

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