Electronic Devices		Semester	3
Course Code	BEC306A	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives: This course will enable students to:

- Understand the basics of semiconductor physics and electronic devices.
- Describe the mathematical models BJTs and FETs along with the constructional details.
- Understand the construction and working principles of optoelectronic devices
- Understand the fabrication process of semiconductor devices and CMOS process integration.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

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- Lecture method(L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Encourage collaborative(Group)Learning in the class.
- Ask at least three HOTS(Higher order Thinking)questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the realworld-and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.

Module-1

Semiconductors

Bonding forces in solids, Energy bands, Metals, Semiconductors and Insulators, Direct and Indirect semiconductors, Electrons and Holes, Intrinsic and Extrinsic materials, Conductivity and Mobility, Drift and Resistance, Effects of temperature and doping on mobility, Hall Effect.

(Text1:3.1.1,3.1.2,3.1.3,3.1.4,3.2.1,3.2.3,3.2.4,3.4.1,3.4.2,3.4.3,3.4.5).

Module-2

PN Junctions

Forward and Reverse biased junctions-Qualitative description of Current flow at a junction, reverse bias, Reverse bias breakdown- Zener breakdown, avalanche breakdown, Rectifiers.**(Text1:5.3.1,5.3.3,5.4,5.4.1,5.4.2,5.4.3)** Optoelectronic Devices Photodiodes: Current and Voltage in an Illuminated Junction, Solar Cells, Photodetectors. Light Emitting Diode: Light Emitting materials.

(Text1:8.1.1,8.1.2,8.1.3,8.2,8.2.1),

Module-3

Bipolar Junction Transistor

Fundamentals of BJT operation, Amplification with BJTS,BJT Fabrication, The coupled Diode model(Ebers-Moll Model),Switching operation of a transistor, Cutoff, saturation, switching cycle, specifications, Drift in the base region, Base narrowing, Avalanche breakdown.

(Text1:7.1,7.2,7.3,7.5.1,7.6,7.7.1,7.7.2, 7.7.3)

Module-4

Field Effect Transistors

Basic pn JFET Operation, Equivalent Circuit and Frequency Limitations, MOSFET-Two terminal MO Sstructure-Energy band diagram, Ideal Capacitance

-Voltage Characteristics and Frequency Effects, Basic MOSFET Operation- MOSFET structure, Current-Voltage Characteristics.

(Text2:9.1.1,9.4,9.6.1,9.6.2,9.7.1,9.7.2,9.8.1,9.8.2).

Module-5

Fabrication of p-n junctions

Thermal Oxidation, Diffusion, Rapid Thermal Processing, Ion implantation, chemical vapour deposition, photolithography, Etching, metallization. **(Text 1: 5.1)**

Integrated Circuits

Background, Evolution of ICs, CMOS Process Integration, Integration of Other Circuit Elements.**(Text 1:9.1,9.2,9.3.1,9.3.3).**

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Understand the principles of semiconductor Physics
2. Understand the principles and characteristics of different types of semiconductor devices
3. Understand the fabrication process of semiconductor devices
4. Utilize the mathematical models of semiconductor junctions for circuits and systems.
5. Identify the mathematical models of MOS transistors for circuits and systems.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. Ben. G. Streetman, Sanjay Kumar Banerjee, "Solid State Electronic Devices",7th Edition,Pearson Education,2016,ISBN978-93-325-5508-2.
2. Donald A Neamen, Dhrubes Biswas, "Semiconductor Physics and Devices", 4th Edition,McGraw **Hill** Education, 2012,ISBN 978-0-07- 107010-2.

ReferenceBooks:

3. S.M.Sze,KwokK.Ng,"PhysicsofSemiconductorDevices",3rd Edition, Wiley,2018.
4. AdirBar-Lev,"SemiconductorandElectronicDevices",3rd Edition,PHI, 1993

Web links and Video Lectures (e-Resources):

H.O.D.
Dept. Of Electronics & Communication
Institute of Engg. & Tech
Ajjar, MOODBIDRI - 574 225