Analog and Digital Electronics Circuit		Semester	III
Course Code	BAG306C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination nature (SEE)	**Theory**		

Course objectives:

1. Explain the use of photo electronics devices, 555 timer IC, Regulator ICs and uA741
2. Make use of simplifying techniques in the design of combinational circuits.
3. Illustrate combinational and sequential digital circuits
4. Demonstrate the use of flipflops and apply for registers
5. Design and test counters, Analog-to-Digital and Digital-to-Analog conversion techniques.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

BJT Biasing: Fixed bias, Collector to base Bias, voltage divider bias Operational Amplifier Application Circuits: Peak Detector, Schmitt trigger, Active Filters, Non-Linear Amplifier, Relaxation Oscillator, Current-to-Voltage and Voltage-to-Current Converter, Regulated Power Supply Parameters, adjustable voltage regulator, D to A and A to D converter.

Module-2
Karnaugh maps: minimum forms of switching functions, two and three variable Karnaugh maps, four variable Karnaugh maps, determination of minimum expressions using essential prime implicants, QuineMcClusky Method: determination of prime implicants, the prime implicant chart, Petricks method, simplification of incompletely specified functions, simplification using map-entered variables
Module-3
Combinational circuit design and simulation using gates: Review of Combinational circuit design, design of circuits with limited Gate Fan-in, Gate delays and Timing diagrams, Hazards in combinational Logic, simulation and testing of logic circuits Multiplexers, Decoders and Programmable Logic Devices: Multiplexers, three state buffers, decoders and encoders, Programmable Logic devices.
Module-4
Introduction to VHDL: VHDL description of combinational circuits, VHDL Models for multiplexers, VHDL Modules. Latches and Flip-Flops: Set Reset Latch, Gated Latches, Edge-Triggered D Flip Flop 3,SR Flip Flop, J K Flip Flop, T Flip Flop.
Module-5
Registers and Counters: Registers and Register Transfers, Parallel Adder with accumulator, shift registers, design of Binary counters, counters for other sequences, counter design using SR and J K Flip Flops.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Design and analyze application of analog circuits using photo devices, timer IC, power supply and regulator IC and op-amp.
2. Explain the basic principles of A/D and D/A conversion circuits and develop the same.
3. Simplify digital circuits using Karnaugh Map, and Quine-McClusky Methods
4. Explain Gates and flip flops and make us in designing different data processing circuits, registers and counters and compare the types.
5. Develop simple HDL programs

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.
- Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Textbooks:

1. Charles H Roth and Larry L Kinney, Raghunandan G H Analog and Digital Electronics, Cengage Learning, 2019

Reference Books:

1. Anil K Maini, Varsha Agarwal, Electronic Devices and Circuits, Wiley, 2012.
2. Donald P Leach, Albert Paul Malvino & Goutam Saha, Digital Principles and Applications, 8th Edition, Tata McGraw Hill, 2015.
3. M. Morris Mani, Digital Design, 4th Edition, Pearson Prentice Hall, 2008.
4. David A. Bell, Electronic Devices and Circuits, 5th Edition, Oxford University Press, 2008

Web links and Video Lectures (e-Resources):

1. Analog Electronic Circuits: https://nptel.ac.in/courses/108/102/108102112/
2. Digital Electronic Circuits: https://nptel.ac.in/courses/108/105/108105132/
3. Analog Electronics Lab: http://vlabs.iitkgp.ac.in/be/
4. Digital Electronics Lab: http://vlabs.iitkgp.ac.in/dec

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quizzes
- Assignments
- Seminars

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