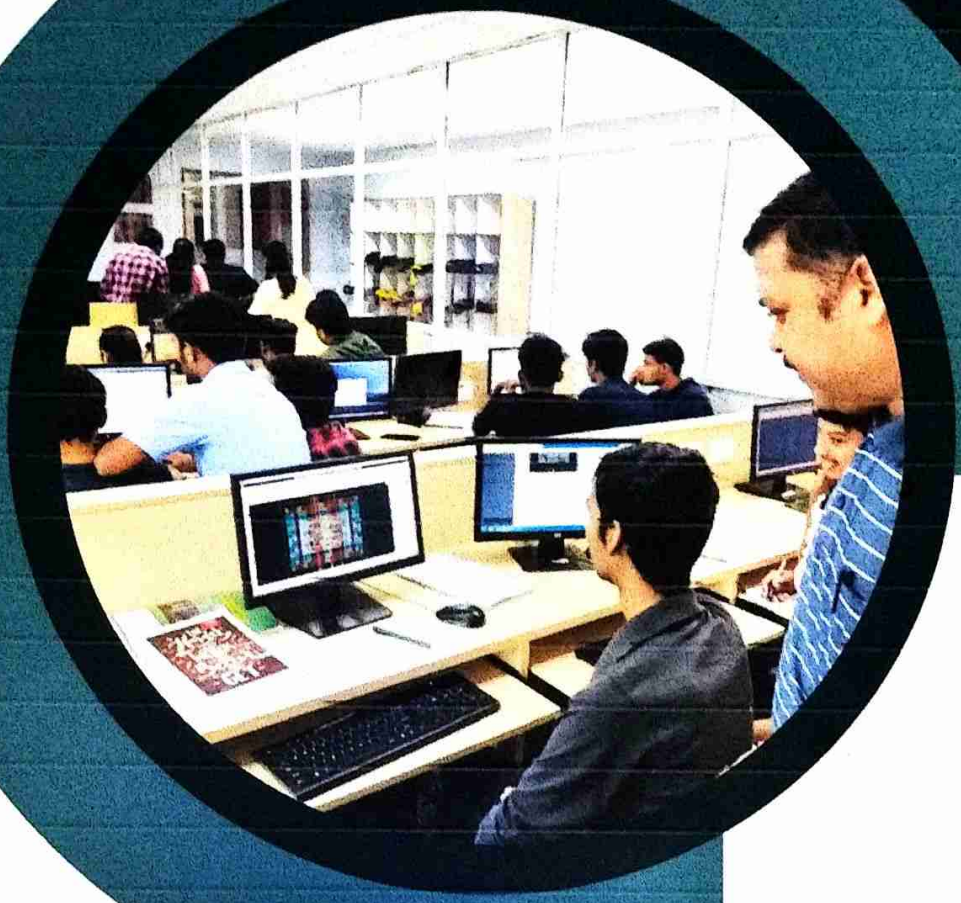
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING



REPORT ON:

VLSI TRAINING

DATE: 29/6/2023 TO 2/7/2023

VENUE: HDL LAB DPT.ECE

RESOURCE PERSON: DR.SRINIVAS RAO UDARA

INTRODUCTION TO VLSI TRAINING:

The VLSI workshop conducted by Dr. Srinivas Rao Udara was a four-day training program focused on VLSI simulation, synthesis, and physical layout design of digital circuits. Participants gained a comprehensive understanding of VLSI design using industry-standard tools and techniques.

The workshop began with an introduction to VLSI, highlighting its importance and applications. Participants were acquainted with essential tools such as Cadence, Genus, and Innovus.

The training covered simulation using Cadence tools, synthesis with the Genus tool, and physical layout design using Innovus. Participants gained hands-on experience in each area.

Dr. Udara also covered Hardware Description Languages (HDLs) like VHDL and Verilog, used in digital circuit design.

The workshop concluded with industry-level techniques and guidance on research and review paper writing.

Overall, the VLSI workshop provided participants with a practical understanding of VLSI design, empowering them to apply their knowledge effectively.

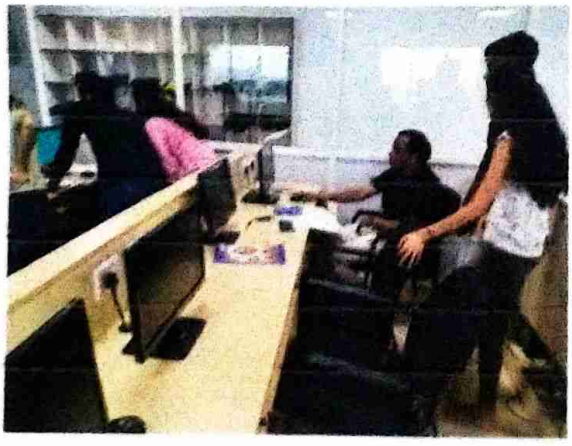
DAY 1:

- Introduction to VLSI: Dr. Srinivas Rao Udara provided a comprehensive introduction to VLSI, explaining its importance in modern electronics and its applications.

- Tools Used in VLSI: Participants were introduced to the essential tools used in VLSI design, emphasizing their roles in the design flow.

- Digital VLSI: Dr. Udara explained the fundamentals of digital VLSI, covering topics such as digital logic design, circuit elements, and Boolean algebra.

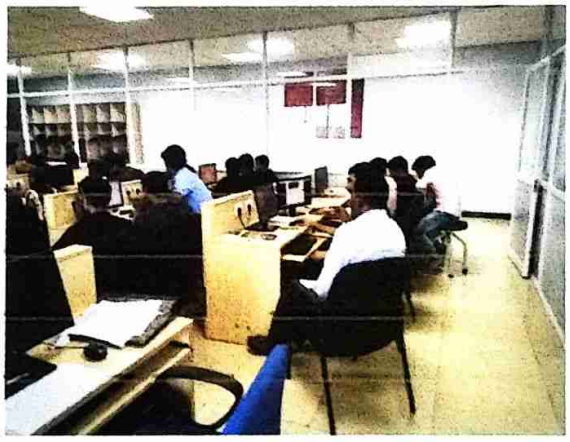
- HDL Languages: The participants were introduced to Hardware Description Languages (HDLs) commonly used in VLSI design, such as VHDL or Verilog.



DAY 2:

- Simulation using Cadence: Participants received hands-on training on using Cadence tools for simulation. They learned how to verify the functionality and performance of digital VLSI circuits through simulation.

- Synthesis using Genus: Dr. Udara guided the participants through the synthesis process using the Genus tool. They learned how to transform RTL designs into gate-level representations.



DAY 3:

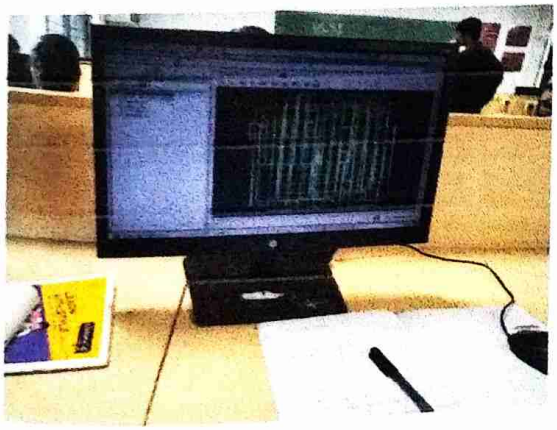
- Continued Synthesis using Genus: Participants practiced synthesis using the Genus tool, gaining further expertise in transforming RTL designs into gate-level representations.

- Physical Layout Design using Innovus: Dr. Udara introduced the participants to physical layout design using the Innovus tool. They learned how to create a physical representation of the circuit, considering various design constraints, timing optimization, and power considerations.

DAY 4:

- Industry-Level Techniques: Dr. Udara shared industry-level shortcuts and best practices for simulation, synthesis, and layout design. Participants gained insights into efficient ways of designing VLSI circuits.

- Research and Review Paper Writing: Dr. Udara provided guidance on writing research and review papers, explaining the structure, formatting, and content requirements for high-quality publications.



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