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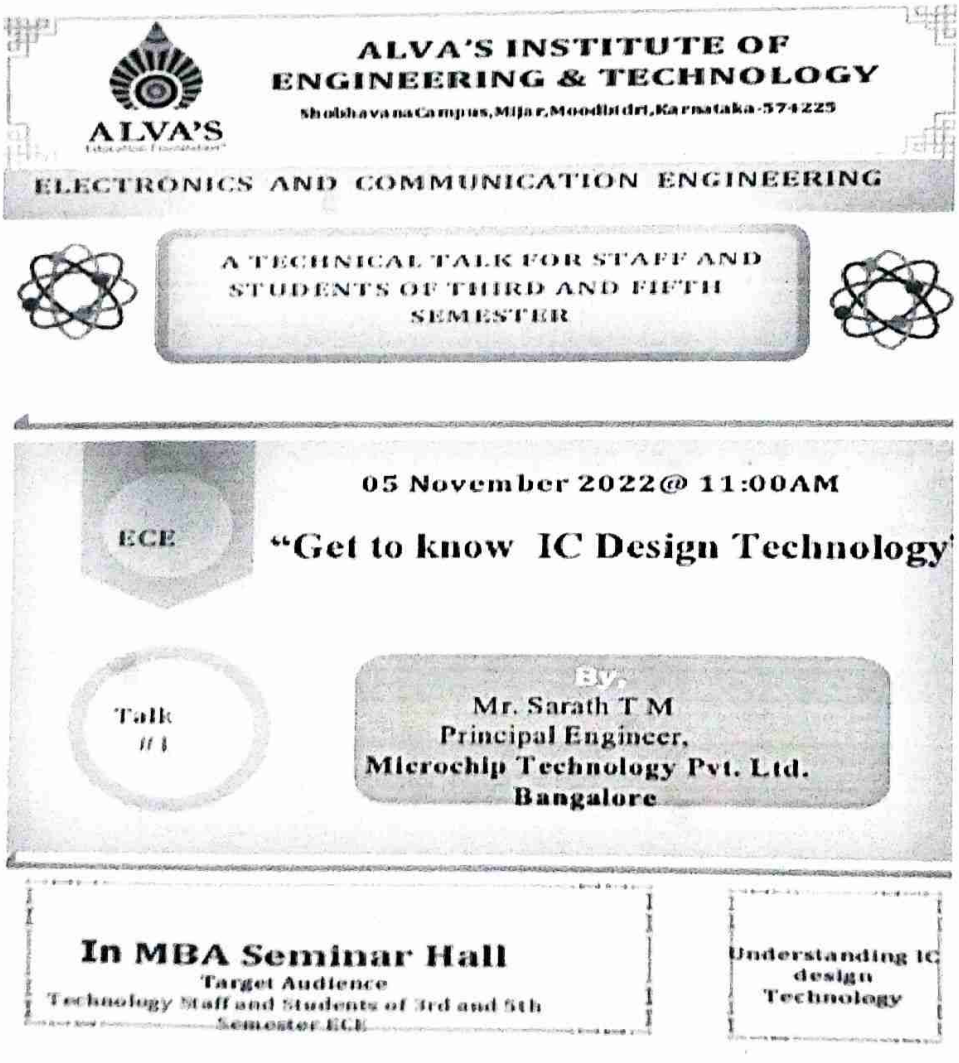
Technical Talk-I
on
"Get to know IC Design Technology"

Resource Person: Mr. Sarath T M

Principal Engineer,

Microchip Technology Pvt. Ltd. Bangalore

Date: 05-11-2022 | Time: 11:00AM to 12:45 PM.



Department of ECE, conducted the first technical talk of the odd semester 2022-23 on **"Get to know IC Design Technology"** for the staff and students of 3rd and 5th semester - ECE on 5th November2022 by Mr. Sarath T M, Principal Engineer, Microchip Technology Pvt. Ltd. Bangalore

Mr. Sarath T M is working as Principal Engineer, Microchip Technology Pvt. Ltd. Bangalore. He is having great experience as a VLSI(FPGA & ASIC) design and front end implementation engineer with leadership skills.

He is involved in micro architectural design, RTL development section.
He holds Multiple master degree in IC design and Management. His skills are, Application-Specific Integrated Circuits (ASIC) · Field-Programmable Gate Arrays (FPGA) · Logic Synthesis · RTL Design · Static Timing Analysis **Skills:** Application-Specific Integrated Circuits (ASIC) · Field-Programmable Gate Arrays (FPGA) · Logic Synthesis · RTL Design · Static Timing Analysis

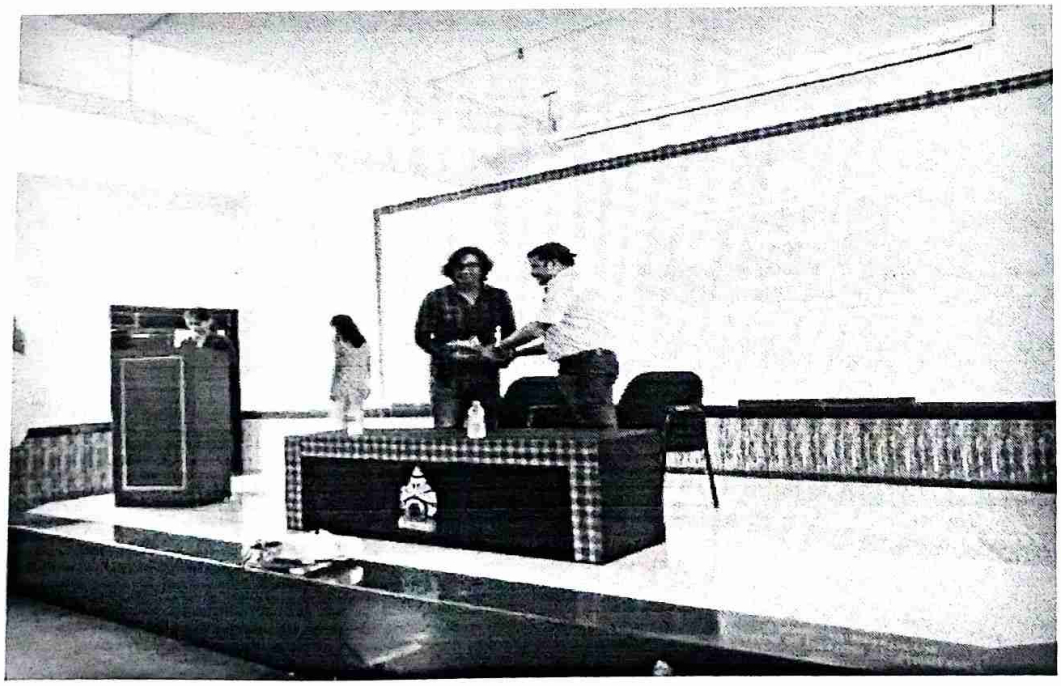


Fig: Welcoming of the guest

Fig. Technical talk by the guest

With millions or billions of components on one single chip, it's not possible to position and connect each component individually. Dies are too small to solder and connect to. Instead, designers use a special-purpose programming language to create small circuit elements and combine them to progressively increase the size and density of components to meet application requirements.

In the talk following points were discussed,

The fabrication of semiconductor devices is the process used to fabricate integrated circuits devices, typically metal oxide semiconductor MOS devices used in integrated circuits chips in any electrical and electronic devices. The starting material for integrated circuits fabrication is Single crystal silicon wafer. The fabrication operation is has many steps:

1. Layering, The layering step serves to add thin layers to the surface of the wafer. These layers may be of a different material, microstructure and composition of the same material such as polycristalline silicon and silicon oxide.

2. Patterning, the most important step in the wafer fabrication is patterning or lithography. The deposition, doping, etching and patterning refer to a series of steps to selectively mask or expose portions of the surface. It sets device's critical dimensions on the wafers.

3. Doping, it is refers to the process of incorporating specific amounts of electrically active impurities through openings on the surface of the wafers. The doped materials are typically impurities of the type p or n and are necessary to form devices such as diodes , transistors, conductors and IC devices.

Finally Prof. Sudhakara HM Associate Professor, department of ECE expressed gratitude to the resource person for giving such an informative talk to the students.