Verilog HDL

Course Code	: 18EC56	CIE Marks	:40
Lecture Hours/Week	: 03	SEE Marks	:60
Total Number of Lecture Hours	: 40 (08 Hrs/Module)	Exam Hours	:03
	CREDITS–03		

Course Learning Objectives: This course will enable students to:

- Learn different Verilog HDL constructs.
- Familiarize the different levels of abstraction in Verilog.
- Understand Verilog Tasks, Functions and Directives.
- Understand timing and delay Simulation.
- Understand the concept of logic synthesis and its impact in verification

Module 1

Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL-flow, why Verilog HDL?, trends in HDLs.
Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block. **L1,L2,L3**

Module 2

Basic Concepts: Lexical conventions, data types, system tasks, compiler directives.
Modules and Ports: Module definition, port declaration, connecting ports, hierarchical name referencing **L1,L2,L3**

Module 3

Gate-Level Modeling: Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays.
Dataflow Modeling: Continuous assignments, delay specification, expressions, operators, operands, operator types. **L1,L2,L3**

Module 4

Behavioral Modeling: Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks.
Tasks and Functions: Differences between tasks and functions, declaration, invocation, automatic tasks and functions. **L1,L2,L3**

Module 5

Useful Modeling Techniques: Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks.
Logic Synthesis with Verilog: Logic Synthesis, Impact of logic synthesis, Verilog HDL Synthesis, Synthesis design flow, Verification of Gate-Level Netlist. **(Chapter 14 till 14.5 of Text).** **L1,L2,L3**

Course Outcomes: At the end of this course, students will be able to

1. Write Verilog programs in gate, dataflow (RTL), behavioral and switch modeling levels of Abstraction.
2. Design and verify the functionality of digital circuit/system using test benches.
3. Identify the suitable Abstraction level for a particular digital design.
4. Write the programs more effectively using Verilog tasks, functions and directives.
5. Perform timing and delay Simulation and Interpret the various constructs in logic synthesis.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Samir Palnitkar, **"Verilog HDL: A Guide to Digital Design and Synthesis"**, Pearson Education, Second Edition.

Reference Books:

1. Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer Science+Business Media, LLC, Fifth edition.
2. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.
3. Padmanabhan, Tripura Sundari, "Design through Verilog HDL", Wiley, 2016 or earlier.

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