HDL LABORATORY

Course Code : **18ECL58**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:

- Familiarize with the CAD tool to write HDL programs.
- Understand simulation and synthesis of digital design.
- Program FPGAs/CPLDs to synthesize the digital designs.
- Interface hardware to programmable ICs through I/O ports.
- Choose either Verilog or VHDL for a given Abstraction level.

Note: Programming can be done using any compiler. Download the programs on a FPGA/CPLD board and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

PART A

1. Write Verilog program for the following combinational design along with test bench to verify the design:
   a. 2 to 4 decoder realization using NAND gates only (structural model)
   b. 8 to 3 encoder with priority and without priority (behavioural model)
   c. 8 to 1 multiplexer using case statement and if statements
   d. 4-bit binary to gray converter using 1-bit gray to binary converter 1-bit adder and subtractor
2. Model in Verilog for a full adder and add functionality to perform logical operations of XOR, XNOR, AND and OR gates. Write test bench with appropriate input patterns to verify the modeled behaviour.
3. Verilog 32-bit ALU shown in figure below and verify the functionality of ALU by selecting appropriate test patterns. The functionality of the ALU is presented in Table 1.
   a. Write test bench to verify the functionality of the ALU considering all possible input patterns
   b. The enable signal will set the output to required functions if enabled, if disabled all the outputs are set to tri-state
   c. The acknowledge signal is set high after every operation is complete

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