B. E.(Common to all branches)

Choice Based Credit System (CBCS) and Outcome-Based Education (OBE)

SEMESTER - III

TRANSFORM CALCULUS, FOURIER SERIES AND NUMERICAL TECHNIQUES			
Course Code	**21MAT 31**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:2:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course objectives: The goal of the course Transform Calculus, Fourier series and Numerical techniques 21MAT 31 is

- To have an insight into solving ordinary differential equations by using Laplace transform techniques
- Learn to use the Fourier series to represent periodical physical phenomena in engineering analysis.
- To enable the students to study Fourier Transforms and concepts of infinite Fourier Sine and Cosine transforms and to learn the method of solving difference equations by the z-transform method.
- To develop proficiency in solving ordinary and partial differential equations arising in engineering applications, using numerical methods

Module-1: Laplace Transform

Definition and Laplace transforms of elementary functions (statements only). Problems on Laplace'sTransform of $e^{at}f(t)$, $t^n f(t)$, $\frac{f(t)}{t}$. Laplace transforms of Periodic functions (statement only) and unit-step function – problems.

Inverse Laplace transforms definition and problems, Convolution theorem to find the inverse Laplace transforms (without Proof) problems.Laplace transforms of derivatives, solution ofdifferential equations.**(8 Hours)**

Self-study: Solution of simultaneous first-order differential equations.

(RBT Levels: L1, L2 and L3)

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-2: Fourier Series

Introduction toinfinite series, convergence and divergence. Periodic functions, Dirichlet's condition. Fourier series of periodic functions with period 2π and arbitrary period. Half range Fourier series. Practical harmonic analysis.**(8 Hours)**

Self-study: Convergence of series by D'Alembert's Ratio test and, Cauchy'sroot test.

(RBT Levels: L1, L2 and L3)

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-3: Infinite Fourier Transforms and Z-Transforms

Infinite Fourier transforms definition, Fourier sine and cosine transforms. Inverse Fourier transforms, Inverse Fourier cosine and sine transforms. Problems.

Difference equations, z-transform-definition, Standard z-transforms, Damping and shifting rules, Problems. Inverse z-transform and applications to solve difference equations.**(8 Hours)**

Self Study: Initial value and final value theorems, problems.

(RBT Levels: L1, L2 and L3)

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-4: Numerical Solution of Partial Differential Equations	
Classifications of second-order partial differential equations, finite difference approximations to derivatives, Solution of Laplace's equationusing standard five-point formula. Solution of heat equation by Schmidt explicit formula and Crank- Nicholson method, Solution of the Wave equation. Problems. **(8 Hours)** **Self Study**: Solution of Poisson equations using standard five-point formula. **(RBT Levels: L1, L2 and L3)**	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation
Module-5: Numerical Solution of Second-Order ODEs and Calculus of Variations	
Second-order differential equations - Runge-Kutta method and Milne's predictor and corrector method. (No derivations of formulae). Calculus of Variations:Functionals, Euler's equation, Problems on extremals of functional. Geodesics on a plane,Variationalproblems.**(8 Hours)** **Self Study:** Hanging chain problem **(RBT Levels: L1, L2 and L3)**	
Course outcomes: After successfully completing the course, the students will beable : ➢ To solve ordinary differential equations using Laplace transform. ➢ Demonstrate the Fourier series to study the behaviour of periodic functions and their applications in system communications, digital signal processing and field theory. ➢ To use Fourier transforms to analyze problems involving continuous-time signals and to apply Z-Transform techniques to solve difference equations ➢ To solve mathematical models represented by initial or boundary value problems involving partial differential equations ➢ Determine the extremals of functionals using calculus of variations and solve problems arising in dynamics of rigid bodies and vibrational analysis.	

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks (duration 01 hour)**
2. First test at the end of 5th week of the semester
3. Second test at the end of the 10th week of the semester
4. Third test at the end of the 15th week of the semester

Two assignments each of 10 Marks

5. First assignment at the end of 4th week of the semester
6. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

7. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

- The question paper will be set for 100 marks and marks scored will be proportionally scaled down to 50 marks
- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books:

1. **B.S.Grewal**:"HigherEngineeringMathematics",Khannapublishers,44th Ed.2018
2. **E.Kreyszig**:"AdvancedEngineeringMathematics",JohnWiley&Sons,10th Ed.(Reprint),2016.

Reference Books

1. **V.Ramana:**"HigherEngineeringMathematics"McGraw-HillEducation,11th Ed.
2. **SrimantaPal&SubodhC.Bhunia:**"EngineeringMathematics"OxfordUniversityPress,3rd Reprint, 2016.
3. **N.P Bali and Manish Goyal**: "A textbook of Engineering Mathematics" Laxmi Publications, Latest edition.
4. **C. Ray Wylie, Louis C. Barrett:** "Advanced Engineering Mathematics" McGraw – Hill Book Co.Newyork, Latested.
5. **Gupta C.B, Sing S.R and Mukesh Kumar:** "Engineering Mathematic for Semester I and II", Mc-Graw Hill Education(India) Pvt. Ltd2015.
6. **H.K.DassandEr.RajnishVerma:**"HigherEngineeringMathematics"S.ChandPublication(2014).
7. **JamesStewart:**"Calculus"Cengagepublications,7th edition,4th Reprint2019.

Web links and Video Lectures (e-Resources):

- http://.ac.in/courses.php?disciplineID=111
- http://www.class-central.com/subject/math(MOOCs)
- http://academicearth.org/
- http://www.bookstreet.in.
- VTU e-ShikshanaProgram
- VTU EDUSATProgram

Activity-Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quizzes
- Assignments
- Seminars

Siddesh

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III Semester

Digital System Design Using Verilog			
Course Code	21EC32	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 13 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

1. To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques.
2. To impart the concepts of designing and analyzing combinational logic circuits.
3. To impart design methods and analysis of sequential logic circuits.
4. To impart the concepts of Verilog HDL-data flow and behavioral models for the design of digital systems.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class .
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
- Give Programming Assignments.

Module-1

Principles of Combinational Logic: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps- up to 4 variables, Quine-McCluskey Minimization Technique. Quine-McCluskey using Don't Care Terms. (Section 3.1 to 3.5 of Text 1).

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-2

Logic Design with MSI Components and Programmable Logic Devices: Binary Adders and Subtractors, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices (PLDs) (Section 5.1 to 5.7 of Text 2)

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-3	
Flip-Flops and its Applications: The Master-Slave Flip-flops (Pulse-Triggered flip-flops): SR flip-flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, JK, D and SR flip-flops. (Section 6.4, 6.6 to 6.9 (Excluding 6.9.3) of Text 2)	
Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3
Module-4	
Introduction to Verilog: Structure of Verilog module, Operators, Data Types, Styles of Description. (Section 1.1 to 1.6.2, 1.6.4 (only Verilog), 2 of Text 3) **Verilog Data flow description:** Highlights of Data flow description, Structure of Data flow description. (Section 2.1 to 2.2 (only Verilog) of Text 3)	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3
Module-5	
Verilog Behavioral description: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers (2:1, 4:1, 8:1). (Section 3.1 to 3.4 (only Verilog) of Text 3) **Verilog Structural description:** Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder. (Section 4.1 to 4.2 of Text 3)	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Using suitable simulation software, demonstrate the operation of the following circuits:

Sl.No	Experiments
1	To simplify the given Boolean expressions and realize using Verilog program.
2	To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description.
3	To realize 4-bit ALU using Verilog program.
4	To realize the following Code converters using Verilog Behavioral description a) Gray to binary and vice versa b) Binary to excess3 and vice versa
5	To realize using Verilog Behavioral description: 8:1 mux, 8:3 encoder, Priority encoder
6	To realize using Verilog Behavioral description: 1:8 Demux, 3:8 decoder, 2-bit Comparator
7	To realize using Verilog Behavioral description: Flip-flops: a) JK type b) SR type c) T type and d) D type
8	To realize Counters - up/down (BCD and binary) using Verilog Behavioral description.
	Demonstration Experiments (For CIE only – not to be included for SEE)
	Use FPGA/CPLD kits for downloading Verilog codes and check the output for interfacing experiments.
9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
10	Verilog programs to interface a Relay or ADC to the FPGA/CPLD and demonstrate its working.
11	Verilog programs to interface DAC to the FPGA/CPLD for Waveform generation.
12	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

Course Outcomes

At the end of the course the student will be able to:

1. Simplify Boolean functions using K-map and Quine-McCluskey minimization technique.
2. Analyze and design for combinational logic circuits.
3. Analyze the concepts of Flip Flops (SR, D, T and JK) and to design the synchronous sequential circuits using Flip Flops.
4. Model Combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Second assignment at the end of 9th week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured out of 100 will be scaled down to 50 marks.

Suggested Learning Resources:

Text Books

1. Digital Logic Applications and Design by John M Yarbrough, Thomson Learning, 2001.
2. Digital Principles and Design by Donald D Givone, McGraw Hill, 2002.
3. HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dreamtech press.

Reference Books:

1. Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning
2. Logic Design, by Sudhakar Samuel, Pearson/ Sanguine, 2007
3. Fundamentals of HDL, by Cyril P R, Pearson/Sanguine 2010

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills.

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III Semester

Basic Signal Processing			
Course Code	21EC33	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 13 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

Preparation: To prepare students with fundamental knowledge/ overview in the field of Signal Processing with Familiarization with the concept of Vector spaces and orthogonality with a qualitative insight into applications in communications.

Core Competence: To equip students with a basic foundation of Signal Processing by delivering the basics of quantitative parameters for Matrices & Linear Transformations, the mathematical description of discrete time signals and systems, analyzing the signals in time domain using convolution sum, classifying signals into different categories based on their properties, analyzing Linear Time Invariant (LTI) systems in time and transform domains

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
- Give Programming Assignments.

Module-1

Vector Spaces: Vector spaces and Null subspaces, Rank and Row reduced form, Independence, Basis and dimension, Dimensions of the four subspaces, Rank-Nullity Theorem, Linear Transformations Orthogonality: Orthogonal Vectors and Subspaces, Projections and Least squares, Orthogonal Bases and Gram-Schmidt Orthogonalization procedure

(Refer Chapters 2 and 3 of Text 1)

Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Module-2	
Eigen values and Eigen vectors: Review of Eigen values and Diagonalization of a Matrix, Special Matrices (Positive Definite, Symmetric) and their properties, Singular Value Decomposition. **(Refer Chapter 5, Text 1)**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Module-3	
Introduction and Classification of signals: Definition of signal and systems with examples, Elementary signals/Functions: Exponential, sinusoidal, step, impulse and ramp functions **Basic Operations on signals:** Amplitude scaling, addition, multiplication, time scaling, time shift and time reversal. Expression of triangular, rectangular and other waveforms in terms of elementary signals **System Classification and properties:** Linear-nonlinear, Time variant -invariant, causal-noncausal, static-dynamic, stable-unstable, invertible. **(Text 2) [Only for Discrete Signals & Systems]**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Module-4	
Time domain representation of LTI System: Impulse response, convolution sum. Computation of convolution sum using graphical method for unit step and unit step, unit step and exponential, exponential and exponential, unit step and rectangular, and rectangular and rectangular. **LTI system Properties in terms of impulse response:** System interconnection, Memory less, Causal, Stable, Invertible and Deconvolution and step response **(Text 2) [Only for Discrete Signals & Systems]**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Module-5	
The Z-Transforms: Z transform, properties of the region of convergence, properties of the Z-transform, Inverse Z-transform by partial fraction, Causality and stability, Transform analysis of LTI systems. **(Text 2)**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC	
Sl.No	**Experiments**
1	a. Program to create and modify a vector (array). b. Program to create and modify a matrix.
2	Programs on basic operations on matrix.
3	Program to solve system of linear equations.
4	Program for Gram-Schmidt orthogonalization.
5	Program to find Eigen value and Eigen vector.
6	Program to find Singular value decomposition.

7	Program to generate discrete waveforms.
8	Program to perform basic operation on signals.
9	Program to perform convolution of two given sequences.
10	a. Program to perform verification of commutative property of convolution. b. Program to perform verification of distributive property of convolution. c. Program to perform verification of associative property of convolution.
11	Program to compute step response from the given impulse response.
12	Programs to find Z-transform and inverse Z-transform of a sequence.

Course outcomes (Course Skill Set)

At the end of the course the student will be able to :

1. Understand the basics of Linear Algebra
2. Analyse different types of signals and systems
3. Analyse the properties of discrete-time signals & systems
4. Analyse discrete time signals & systems using Z transforms

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Programming assignment at the end of 9th week of the semester, which can be implemented using programming languages like C++/Python/Java/Scilab

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured out of 100 will be scaled down to 50 marks.

Suggested Learning Resources:

Text Books

1. Gilbert Strang, "Linear Algebra and its Applications", Cengage Learning, 4th Edition, 2006, ISBN 97809802327
2. Simon Haykin and Barry Van Veen, "Signals and Systems", 2nd Edition, 2008, Wiley India. ISBN9971-51-239-4.

Reference Books:

1. **Michael Roberts,** "Fundamentals of Signals & Systems",2nd edition, Tata McGraw-Hill, 2010, ISBN978-0-07-070221-9.
2. **Alan V Oppenheim, Alan S Willsky and S Hamid Nawab,** "Signals and Systems" Pearson Education Asia / PHI, 2"" edition, 1997. Indian Reprint 2002.
3. **H P Hsu, R Ranjan,** "Signals and Systems", Schaum's outlines, TMH, 2006.
4. **B P Lathi,** "Linear Systems and Signals", Oxford University Press, 2005.
5. **Ganesh Rao and Satish Tunga,** "Signals and Systems", Pearson/Sanguine.
6. **Seymour Lipschutz, Marc Lipson,** "Schaums Easy Outline of Linear Algebra", 2020.

Web links and Video Lectures (e-Resources):

Video lectures on Signals and Systems by Alan V Oppenheim

Lecture 1, Introduction | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube

Lecture 2, Signals and Systems: Part 1 | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube

NPTEL video lectures signals and system:

https://www.youtube.com/watch?v=7Z3LE5uM-6Y&list=PLbMVogVj5nJQQZbah2uRZIRZ_9kfoqZyx

Video lectures on Linear Algebra by Gilbert Strang

https://www.youtube.com/watch?v=ZK3O402wf1c&list=PL49CF3715CB9EF31D&index=1

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

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III Semester

Analog Electronic Circuits			
Course Code	21EC34	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives: This course will enable students to

- Explain various BJT parameters, connections and configurations.
- Design and demonstrate the diode circuits and transistor amplifiers.
- Explain various types of FET biasing and demonstrate the use of FET amplifiers.
- Analyze Power amplifier circuits in different modes of operation.
- Construct Feedback and Oscillator circuits using FET.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

BJT Biasing: Biasing in BJT amplifier circuits: The Classical Discrete circuit bias (Voltage-divider bias), Biasing using a collector to base feedback resistor.

Small signal operation and Models: Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain, Separating the signal and the DC quantities, The hybrid Π model, The T model.

MOSFETs: Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor.

Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model.

[Text 1: 3.5(3.5.1, 3.5.3), 3.6(3.6.1 to 3.6.7), 4.5(4.5.1, 4.5.2, 4.5.3), 4.6(4.6.1 to 4.6.7)]

Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Basic BJT Amplifier Configurations- Design of Common Emitter and Common collector amplifier circuits. **RBT Level:** L1, L2, L3

Module-2

MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance RS, Source follower.

MOSFET internal capacitances and High frequency model: The gate capacitive effect, Junction capacitances, High frequency model.

Frequency response of the CS amplifier: The three frequency bands, high frequency response, Low frequency response.

Oscillators: FET based Phase shift oscillator, LC and Crystal Oscillators (no derivation) [Text 1: 4.7(4.7.1 to 4.7.4, 4.7.6) 4.8(4.8.1, 4.8.2, 4.8.3), 4.9, 12.2.2, 12.3.1, 12,3,2]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Discrete Circuit MOS Amplifier – The common source amplifier and the source follower. **RBT Level:** L1, L2, L3

Module-3

Feedback Amplifier: General feedback structure, Properties of negative feedback, The Four Basic Feedback Topologies, The series-shunt, series-series, shunt-shunt and shunt-series amplifiers (Qualitative Analysis). **Output Stages and Power Amplifiers:** Introduction, Classification of output stages, Class A output stage, Class B output stage: Transfer Characteristics, Power Dissipation, Power Conversion efficiency, Class AB output stage, Class C tuned Amplifier. [Text 1: 7.1, 7.2, 7.3, 7.4.1, 7.5.1, 7.6 (7.6.1 to 7.6.3), 13.1, 13.2, 13.3(13.3.1, 13.3.2, 13.3.3, 13.4, 13.7)]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Class D power amplifier. **RBT Level:** L1, L2, L3

Module-4

Op-Amp Circuits: Op-amp DC and AC Amplifiers, DAC - Weighted resistor and R-2R ladder, ADC-Successive approximation type, Small Signal half wave rectifier, Absolute value output circuit, Active Filters, First and second order low-pass and high-pass Butterworth filters, Band-pass filters, Band reject filters. **555 Timer and its applications:** Monostable and Astable Multivibrators. [Text 2: 6.2, 8.11(8.11.1a, 8.11.1b), 8.11.2a, 8.12.2,8.13 7.2, 7.3, 7.4, 7.5, 7.6, 7.8, 7.9, 9.4.1, 9.4.1(a), 9.4.3, 9.4.3(a)]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Clippers and Clampers, Peak detector, Sample and hold circuit. **RBT Level:** L1, L2, L3

Module-5

Overview of Power Electronic Systems: Power Electronic Systems, Power Electronic Converters and Applications. **Thyristors:** Static Anode-Cathode characteristics and Gate characteristics of SCR, Turn-ON methods, Turn-off Mechanism, Turn-OFF Methods: Natural and Forced Commutation – Class A without design consideration. **Gate Trigger Circuit:** Resistance Firing Circuit, Resistance capacitance firing circuit, Unijunction Transistor: Basic operation and UJT Firing Circuit. [Text 3: 1.3, 1.5,1.6, 2.2,2.3,2.4,2.6, 2.7,2.9, 2.10,3.2,3.5.1, 3.5.2, 3.6.1, 3.6.3,3.6.4]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Basic Construction, working and applications of DIAC, TRIAC, IGBT, GTO. **RBT Level:** L1, L2, L3

Course Outcomes (Course Skill Set)

At the end of the course the student will be able to :

1. Understand the characteristics of BJTs and FETs for switching and amplifier circuits.
2. Design and analyze FET amplifiers and oscillatorswith different circuit configurations and biasing conditions.
3. Understand the feedback topologies and approximations in the design of amplifiers and oscillators.
4. Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.
5. Understand the power electronic device components and its functions for basic power electronic circuits.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.

The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored out of 100 shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6thEdition, Oxford, 2015.ISBN:978-0-19-808913-1
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4thEdition, Pearson Education, 2018. ISBN: 978-93-325-4991-3
3. **MD Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897'**

Web links and Video Lectures (e-Resources):

- Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015.
- Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.

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02.10.2022

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

III Semester

Analog and Digital Electronics Lab			
Course Code	21ECL35	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Understand the electronic circuit schematic and its working
- Realize and test amplifier and oscillator circuits for the given specifications
- Realize the opamp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers.
- Study the static characteristics of SCR and test the RC triggering circuit.
- Design and test the combinational and sequential logic circuits for their functionalities.
- Use the suitable ICs based on the specifications and functions.

Sl.No.	Experiments
1	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.
2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator and iii) RC Phase shift oscillator
3	Design and set up the circuits using opamp: i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator
4	Obtain the static characteristics of SCR and test SCR Controlled HWR and FWR using RC triggering circuit.
5	Design and implement (a) Half Adder & Full Adder using basic gates and NAND gates, (b) Half subtractor & Full subtractor using NAND gates, (c) 4-variable function using IC74151(8:1MUX).
6	Realize (i) Binary to Gray code conversion & vice-versa (IC74139), (ii) BCD to Excess-3 code conversion and vice versa
7	a) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop b) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.
8	Realize a) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop b) Mod-N Counter using IC7490 / 7476 c) Synchronous counter using IC74192

9	Design 4-bit R – 2R Op-Amp Digital to Analog Converter (i) for a 4-bit binary input using toggle switches (ii) by generating digital inputs using mod-16
10	Pseudorandom sequence generator using IC7495
11	Test the precision rectifiers using opamp: i) Half wave rectifier ii) Full wave rectifier
12	Design and test Monostable and Astable Multivibrator using 555 Timer

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Design and analyze the BJT/FET amplifier and oscillator circuits.
2. Design and test Opamp circuits to realize the mathematical computations, DAC and precision rectifiers.
3. Design and test the combinational logic circuits for the given specifications.
4. Test the sequential logic circuits for the given functionality.
5. Demonstrate the basic electronic circuit experiments using SCR and 555 timer.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks.**

The split-up of CIE marks for record/ journal and test are in the ratio **60:40.**

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Fundamentals of Electronic Devices and Circuits Lab Manual, David A Bell, 5th Edition, 2009, Oxford University Press.
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018. ISBN: 978-93-325-4991-3.
3. Fundamentals of Logic Design, Charles H Roth Jr., Larry L Kinney, Cengage Learning, 7th Edition.

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IV Semester

Digital Signal Processing			
Course Code	21EC42	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives:

1. **Preparation:** To prepare students with fundamental knowledge/ overview in the field of Digital Signal Processing
2. **Core Competence:** To equip students with a basic foundation of Signal Processing by delivering the basics of Discrete Fourier Transforms & their properties, design of filters and overview of digital signal processors

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes
10. Give Programming Assignments

Module-1

Discrete Fourier Transforms (DFT): Frequency domain sampling and Reconstruction of Discrete Time Signals, The Discrete Fourier Transform, DFT as a linear transformation, Properties of the DFT: Periodicity, Linearity and Symmetry properties, Multiplication of two DFTs and Circular Convolution **[Text 1]**

Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

Module-2

Additional DFT Properties, Linear filtering methods based on the DFT: Use of DFT in Linear Filtering, Filtering of Long data Sequences. Fast-Fourier-Transform (FFT) algorithms: Efficient Computation of the DFT: Radix-2 FFT algorithms for the computation of DFT and IDFT decimation in-time **[Text 1]**

Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

Module-3

Design of FIR Filters: Characteristics of practical frequency-selective filters, Symmetric and Anti-symmetric FIR filters, Design of Linear-phase FIR (low pass and High pass) filters using windows - Rectangular, Hamming, Hanning, Bartlett windows. Structure for FIR Systems: Direct form, Cascade form and Lattice structures **[Text1]**

Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

Module-4

IIR Filter Design: Infinite Impulse response Filter Format, Bilinear Transformation Design Method, Analog Filters using Low pass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth (Lowpass and Highpass) Filter Design using BLT. Realization of IIR Filters in Direct form I and II **[Text 2]**

Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

Module-5

Digital Signal Processors: DSP Architecture, DSP Hardware Units, Fixed point format, Floating point Format, IEEE Floating point formats, Fixed point digital signal processors, FIR and IIR filter implementations in Fixed point systems. **[Text 2]**

Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC

List of Programs to be implemented & executed using any programming languages like C++/Python/Java/Scilab / MATLAB/CC Studio (but not limited to)

1. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum.
2. Computation of circular convolution of two given sequences and verification of commutative, distributive and associative property of convolution.
3. Computation of linear convolution of two sequences using DFT and IDFT.
4. Computation of circular convolution of two given sequences using DFT and IDFT
5. Verification of Linearity property, circular time shift property & circular frequency shift property of DFT.
6. Verification of Parseval's theorem
7. Design and implementation of IIR (Butterworth) low pass filter to meet given specifications.
8. Design and implementation of IIR (Butterworth) high pass filter to meet given specifications.
9. Design and implementation of low pass FIR filter to meet given specifications.
10. Design and implementation of high pass FIR filter to meet given specifications.
11. To compute N- Point DFT of a given sequence using DSK 6713 simulator
12. To compute linear convolution of two given sequences using DSK 6713 simulator
13. To compute circular convolution of two given sequences using DSK 6713 simulator

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Determine response of LTI systems using time domain and DFT techniques
2. Compute DFT of real and complex discrete time signals
3. Compute DFT using FFT algorithms
4. Design FIR and IIR Digital Filters
5. Design of Digital Filters using DSP processor

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Programming assignment at the end of 9th week of the semester, which can be implemented using programming languages like C++/Python/Java/Scilab

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50.

Suggested Learning Resources:

Text Books:

1. Proakis & Manolakis, "Digital Signal Processing - Principles Algorithms & Applications", 4th Edition, Pearson education, New Delhi, 2007. ISBN: 81-317-1000-9.
2. Li Tan, Jean Jiang, "Digital Signal processing - Fundamentals and Applications", Academic Press, 2013, ISBN: 978-0-12-415893.

Reference Books:

1. Sanjit K Mitra, "Digital Signal Processing, A Computer Based Approach", 4th Edition, McGraw Hill Education, 2013,
2. Oppenheim & Schaffer, "Discrete Time Signal Processing", PHI, 2003.
3. D Ganesh Rao and Vineeth P Gejji, "Digital Signal Processing" Cengage India Private Limited, 2017, ISBN: 9386858231

Web links and Video Lectures (e-Resources):

By Prof. S. C. Dutta Roy, IIT Delhi

https://nptel.ac.in/courses/117102060

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

Siddesh

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IV Semester

Circuits & Controls			
Course Code	21EC43	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

1. Apply mesh and nodal techniques to solve an electrical network.
2. Solve different problems related to Electrical circuits using Network Theorems and Two port network.
3. Familiarize with the use of Laplace transforms to solve network problems.
4. Understand basics of control systems and design mathematical models using block diagram reduction, SFG, etc.
5. Understand Time domain and Frequency domain analysis.
6. Familiarize with the State Space Model of the system.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class .
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
- Give Programming Assignments.

Module-1

Basic concepts and network theorems

Types of Sources, Loop analysis, Nodal analysis with independent DC and AC Excitations.
(Textbook 1: 2.3, 4.1, 4.2, 4.3, 4.4, 10.6)
Super position theorem, Thevenin's theorem, Norton's Theorem, Maximum Power transfer Theorem.
(Textbook 2: 9.2, 9.4, 9.5, 9.7)

Teaching-Learning Process	Chalk and Talk, YouTube videos, Demonstrate the concepts using circuits **RBT Level:** L1, L2, L3

Module-2	
Two port networks: Short- circuit Admittance parameters, Open- circuit Impedance parameters, Transmission parameters, Hybrid parameters (Textbook 3: 11.1, 11.2, 11.3, 11.4, 11.5) **Laplace transform and its Applications**: Step Ramp, Impulse, Solution of networks using Laplace transform, Initial value and final value theorem (Textbook 3: 7.1, 7.2, 7.4, 7.7, 8.4)	
Teaching-Learning Process	Chalk and Talk **RBT Level:** L1, L2, L3
Module-3	
Basic Concepts and representation: Types of control systems, effect of feedback systems, differential equation of physical systems (only electrical systems), Introduction to block diagrams, transfer functions, Signal Flow Graphs (Textbook 4: Chapter 1.1, 2.2, 2.4, 2.5, 2.6)	
Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3
Module-4	
Time Response analysis: Time response of first order systems. Time response of second order systems, time response specifications of second order systems (Textbook 4: Chapter 5.3, 5.4) **Stability Analysis:** Concepts of stability necessary condition for stability, Routh stability criterion, relative stability Analysis (Textbook 4: Chapter 5.3, 5.4, 6.1, 6.2, 6.4, 6.5)	
Teaching-Learning Process	Chalk and Talk, Any software tool to show time response **RBT Level:** L1, L2, L3
Module-5	
Root locus: Introduction the root locus concepts, construction of root loci (Textbook 4: 7.1, 7.2, 7.3) **Frequency Domain analysis and stability**: Correlation between time and frequency response and Bode plots (Textbook 4: 8.1, 8.2, 8.4) **State Variable Analysis:** Introduction to state variable analysis: Concepts of state, state variable and state models. State model for Linear continuous –Time systems, solution of state equations. (Textbook 4: 12.2, 12.3, 12.6)	
Teaching-Learning Process	Chalk and Talk, Any software tool to plot Root locus, Bode plot **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC Using suitable hardware and simulation software, demonstrate the operation of the following circuits:	
Sl.No	**Experiments**
1	Verification of Superposition theorem
2	Verification of Thevenin's theorem
3	Speed torque characteristics of i)AC Servomotor ii) DC Servomotors
4	Determination of time response specification of a second order Under damped System, for different damping factors.
5	Determination of frequency response of a second order System
6	Determination of frequency response of a lead lag compensator
7	Using Suitable simulation package study of speed control of DC motor using i) Armature control ii) Field control

8	Using suitable simulation package, draw Root locus & Bode plot of the given transfer function.
Demonstration Experiments (For CIE only, not for SEE)	
9	Using suitable simulation package, obtain the time response from state model of a system.
10	Implementation of PI, PD Controllers.
11	Implement a PID Controller and hence realize an Error Detector.
12	Demonstrate the effect of PI, PD and PID controller on the system response.

Course Outcomes

At the end of the course the student will be able to:

1. Analyse and solve Electric circuit, by applying, loop analysis, Nodal analysis and by applying network Theorems.
2. Evaluate two port parameters of a network and Apply Laplace transforms to solve electric networks.
3. Deduce transfer function of a given physical system, from differential equation representation or Block Diagram representation and SFG representation.
4. Calculate time response specifications and analyse the stability of the system.
5. Draw and analyse the effect of gain on system behaviour using root loci.
6. Perform frequency response Analysis and find the stability of the system.
7. Represent State model of the system and find the time response of the system.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Second assignment at the end of 9th week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks.**

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and

scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured out of 100 shall be reduced proportionally to 50.

Suggested Learning Resources:

Text Books

1. Engineering circuit analysis, William H Hayt, Jr, Jack E Kemmerly, Steven M Durbin, Mc Graw Hill Education, Indian Edition 8e.
2. Networks and Systems, D Roy Choudhury, New age international Publishers, second edition.
3. Network Analysis, M E Van Valkenburg, Pearson, 3e.
4. Control Systems Engineering, I J Nagrath, M. Gopal, New age international Publishers, Fifth edition.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/courses/108106098
- https://nptel.ac.in/courses/108102042

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

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VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

IV Semester

Communication Theory			
Course Code	21EC44	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives: This course will enable students to

- Understand and analyse concepts of Analog Modulation schemes viz; AM, FM., Low pass sampling and Quantization as a random process.
- Understand and analyse concepts digitization of signals viz; sampling, quantizing and encoding.
- Evolve the concept of SNR in the presence of channel induced noise and study Demodulation of analog modulated signals.
- Evolve the concept of quantization noise for sampled and encoded signals and study the concepts of reconstruction from these samples at a receiver.

Teaching-Learning Process (General Instructions)
These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

AMPLITUDE MODULATION: Introduction, Amplitude Modulation: Time & Frequency Domain description, Switching modulator, Envelop detector.
DOUBLE SIDE BAND-SUPPRESSED CARRIER MODULATION: Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing.
SINGLE SIDE-BAND AND VESTIGIAL SIDEBAND METHODS OF MODULATION: SSB Modulation, VSB Modulation, Frequency Translation, Frequency Division Multiplexing, Theme Example: VSB Transmission of Analog and Digital Television.

[Text1: 3.1 to 3.8]

Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Properties of the Fourier Transform, Dirac Delta Function. **RBT Level:** L1, L2, L3

Module-2

ANGLE MODULATION: Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM, Transmission bandwidth of FM Signals, Generation of FM Signals, Demodulation of FM Signals, FM Stereo Multiplexing, Phase-Locked Loop: Nonlinear model of PLL, Linear model of PLL, Nonlinear Effects in FM

Systems. The Superheterodyne Receiver [Text1: 4.1 to 4.6]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, YouTube videos. **Self-study topics:** FM Broadcasting System [Ref1] **RBT Level:** L1, L2, L3
Module-3	
NOISE: Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth. **NOISE IN ANALOG MODULATION**: Introduction, Receiver Model, Noise in DSB-SC receivers. Noise in AM receivers, Threshold effect, Noise in FM receivers, Capture effect, FM threshold effect, FM threshold reduction, Preemphasis and De-emphasis in FM (Text1: 5.10, 6.1 to 6.6)	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, YouTube videos. **Self-study topics:** Mean, Correlation and Covariance functions of Random Processes **RBT Level:** L1, L2, L3
Module-4	
SAMPLING AND QUANTIZATION: Introduction, Why Digitize Analog Sources? The Low pass Sampling process Pulse Amplitude Modulation. Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves. (Text1: 7.1 to 7.7)	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, YouTube videos. **Self-study topics:** T1 carrier systems [Ref1] **RBT Level:** L1, L2, L3
Module-5	
SAMPLING AND QUANTIZATION (Contd): The Quantization Random Process, Quantization Noise, Pulse–Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding, Filtering, Multiplexing; Delta Modulation (Text1: 7.8 to 7.10), Application examples - (a) Video + MPEG (Text1:7.11) and (b) Vocoders (refer Section 6.8 of Reference Book 1)	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, YouTube videos. **Self-study topics:** Digital Multiplexing. [Ref1] **RBT Level:** L1, L2, L3

Course Outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Understand the amplitude and frequency modulation techniques and perform time and frequency domain transformations.
2. Identify the schemes for amplitude and frequency modulation and demodulation of analog signals and compare the performance.
3. Characterize the influence of channel noise on analog modulated signals.
4. Understand the characteristics of pulse amplitude modulation, pulse position modulation and pulse code modulation systems.
5. Illustration of digital formatting representations used for Multiplexers, Vocoders and Video transmission.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. Simon Haykins & Moher, Communication Systems, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.

Reference Books

1. B P Lathi and Zhi Ding, Modern Digital and Analog Communication Systems, Oxford University Press., 4th edition, 2010, ISBN: 97801980738002.
2. Simon Haykins, An Introduction to Analog and Digital Communication, John Wiley India Pvt. Ltd., 2008, ISBN 978–81–265–3653–5.
3. H Taub & D L Schilling, Principles of Communication Systems, TMH, 2011.

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IV Semester

Communication Laboratory I			
Course Code	21ECL46	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Model an analog communication system signal transmission and reception.
- Realize the electronic circuits to perform analog and pulse modulations and demodulations.
- Verify the sampling theorem and relate the signal and its spectrum before and after sampling.
- Understand the process of PCM and delta modulations.
- Understand the PLL operation.

Sl.No.	Experiments
1	Design of active second order Butterworth low pass and high pass filters.
2	Amplitude Modulation and Demodulation of (a) Standard AM and (b) DSBSC (LM741 and LF398 ICs can be used)
3	Frequency modulation and demodulation
4	Design and test Time Division Multiplexing and Demultiplexing of two bandlimited signals.
5	Design and test i) Pulse sampling, flat top sampling and reconstruction. ii) Pulse amplitude modulation and demodulation.
6	Design and test BJT/FET Mixer
7	Pulse Code Modulation and demodulation
8	Phase locked loop Synthesis
9	Illustration of (a) AM modulation and demodulation and display the signal and its spectrum. (b) DSB-SC modulation and demodulation and display the signal and its spectrum. (Use MATLAB/SCILAB)
10	Illustration of FM modulation and demodulation and display the signal and its spectrum. (Use MATLAB/SCILAB)
11	Illustrate the process of sampling and reconstruction of low pass signals. Display the signals and its spectrums of both analog and sampled signals. (Use MATLAB/SCILAB).
12	Illustration of Delta Modulation and the effects of step size selection in the design of DM encoder. (Use MATLAB/SCILAB)

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Demonstrate the AM and FM modulation and demodulation by representing the signals in time and frequency domain.
2. Design and test the sampling, Multiplexing and PAM with relevant circuits.
3. Demonstrate the basic circuitry and operations used in AM and FM receivers.
4. Illustrate the operation of PCM and delta modulations for different input conditions.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by

[illegible]

[illegible]

Suggested Learning Resources

1. [illegible] Principles of Electronic Communication Systems, McGraw Hill Education (India) Private Limited, 2014.
2. B. P. Lathi, Zhi Ding, Modern Digital and Analog Communication Systems, Oxford University Press, 2010.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering

NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 – 22)

IV Semester

C++ Basics			
Course Code	21EC482	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- Understand object-oriented programming concepts, and apply them in solving problems.
- To create, debug and run simple C++ programs.
- Introduce the concepts of functions, friend functions, inheritance, polymorphism and function overloading.
- Introduce the concepts of exception handling and multithreading.

Sl.No	Experiments
1	Write a C++ program to find largest, smallest & second largest of three numbers using inline functions MAX & Min.
2	Write a C++ program to calculate the volume of different geometric shapes like cube, cylinder and sphere using function overloading concept.
3	Define a STUDENT class with USN, Name & Marks in 3 tests of a subject. Declare an array of 10 STUDENT objects. Using appropriate functions, find the average of the two better marks for each student. Print the USN, Name & the average marks of all the students.
4	Write a C++ program to create class called MATRIX using two-dimensional array of integers, by overloading the operator == which checks the compatibility of two matrices to be added and subtracted. Perform the addition and subtraction by overloading + and – operators respectively. Display the results by overloading the operator <<. If (m1 == m2) then m3 = m1 + m2 and m4 = m1 – m2 else display error
5	Demonstrate simple inheritance concept by creating a base class FATHER with data members: *First Name, Surname, DOB & bank Balance* and creating a derived class SON, which inherits: Surname & Bank Balance feature from base class but provides its own feature: First Name & DOB. Create & initialize F1 & S1 objects with appropriate constructors & display the FATHER & SON details.
6	Write a C++ program to define class name FATHER & SON that holds the income respectively. Calculate & display total income of a family using Friend function.
7	Write a C++ program to accept the student detail such as name & 3 different marks by get_data() method & display the name & average of marks using display() method. Define a friend function for calculating the average marks using the method mark_avg().
8	Write a C++ program to explain virtual function (Polymorphism) by creating a base class polygon which has virtual function areas two classes rectangle & triangle derived from polygon & they have area to calculate & return the area of rectangle & triangle respectively.
9	Design, develop and execute a program in C++ based on the following requirements: An EMPLOYEE class containing data members & members functions: i) Data members: employee number (an integer), Employee_ Name (a string of characters), Basic_ Salary (in integer), All_ Allowances (an integer), Net_Salary (an integer). (ii) Member functions: To read the data of an employee, to calculate Net_Salary & to print the values of all the data members. (All_Allowances = 123% of Basic, Income Tax (IT) =30% of gross salary (=basic_ Salary_All_Allowances_IT).
10	Write a C++ program with different class related through multiple inheritance & demonstrate the use of different access specified by means of members variables & members functions.
11	Write a C++ program to create three objects for a class named count object with data members

	such as roll_no & Name. Create a members function set_data ( ) for setting the data values & display ( ) member function to display which object has invoked it using „this" pointer.
12	Write a C++ program to implement exception handling with minimum 5 exceptions classes including two built in exceptions.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Write C++ program to solve simple and complex problems
2. Apply and implement major object-oriented concepts like message passing, function overloading, operator overloading and inheritance to solve real-world problems.
3. Use major C++ features such as Templates for data type independent designs and File I/O to deal with large data set.
4. Analyze, design and develop solutions to real-world problems applying OOP concepts of C++

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and

result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.
The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Object oriented programming in TURBO C++, Robert Lafore, Galgotia Publications, 2002
2. The Complete Reference C++, Herbert Schildt, 4th Edition, Tata McGraw Hill, 2003.
3. Object Oriented Programming with C++, E Balaguruswamy, 4th Edition, Tata McGraw Hill, 2006.

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DIGITAL SIGNAL PROCESSING

Course Code : **18EC52**	CIE Marks : 40
Lecture Hours/Week : 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)	Exam Hours : 03
CREDITS : 04	

Course Learning Objectives: This course will enable students to

- Understand the frequency domain sampling and reconstruction of discrete time signals.
- Study the properties and the development of efficient algorithms for the computation of DFT.
- Realization of FIR and IIR filters in different structural forms.
- Learn the procedures to design of IIR filters from the analog filters using impulse invariance and bilinear transformation.
- Study the different windows used in the design of FIR filters and design appropriate filters based on the specifications.
- Understand the architecture and working of DSP processor

Module-1

Discrete Fourier Transforms (DFT): Frequency domain sampling and Reconstruction of Discrete Time Signals, The Discrete Fourier Transform, DFT as a linear transformation, Properties of the DFT: Periodicity, Linearity and Symmetry properties, Multiplication of two DFTs and Circular Convolution, Additional DFT properties.

[Text 1], **L1,L2,L3**

Module-2

Linear filtering methods based on the DFT: Use of DFT in Linear Filtering, Filtering of Long data Sequences.

Fast-Fourier-Transform (FFT) algorithms: Efficient Computation of the DFT: Radix-2 FFT algorithms for the computation of DFT and IDFT–decimation-in-time and decimation-in-frequency algorithms.

[Text 1], **L1,L2, L3**

Module-3

Design of FIR Filters: Characteristics of practical frequency–selective filters, Symmetric and Antisymmetric FIR filters, Design of Linear-phase FIR filters using windows - Rectangular, Hamming, Hanning, Bartlett windows. Design of FIR filters using frequency sampling method. Structure for FIR Systems: Direct form, Cascade form and Lattice structures.

[Text1], **L1, L2, L3**

Module-4

IIR Filter Design: Infinite Impulse response Filter Format, Bilinear Transformation Design Method, Analog Filters using Lowpass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth Filter Design using BLT. Realization of IIR Filters in Direct form I and II.

[Text 2], L1,L2,L3

Module-5

Digital Signal Processors: DSP Architecture, DSP Hardware Units, Fixed point format, Floating point Format, IEEE Floating point formats, Fixed point digital signal processors, Floating point processors, FIR and IIR filter implementations in Fixed point systems.

[Text 2], L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

1. Determine response of LTI systems using time domain and DFT techniques.
2. Compute DFT of real and complex discrete time signals.
3. Compute DFT using FFT algorithms and linear filtering approach.
4. Design and realize FIR and IIR digital filters.
5. Understand the DSP processor architecture.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60

Text Book:

1. Proakis & Manolakis, "Digital Signal Processing – Principles Algorithms & Applications", 4th Edition, Pearson education, New Delhi, 2007. ISBN: 81-317-1000-9.
2. Li Tan, Jean Jiang, "Digital Signal processing – Fundamentals and Applications", Academic Press, 2013, ISBN: 978-0-12-415893.

Reference Books:

1. Sanjit K Mitra, "Digital Signal Processing, A Computer Based Approach", 4th Edition, McGraw Hill Education, 2013,
2. Oppenheim & Schaffer, "Discrete Time Signal Processing" , PHI, 2003.
3. D.Ganesh Rao and Vineeth P Gejji, "Digital Signal Processing" Cengage India Private Limited, 2017, ISBN: 9386858231

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PRINCIPLES OF COMMUNICATION SYSTEMS

Course Code : **18EC53**	CIE Marks : 40
Lecture Hours/Week : 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)	Exam Hours : 03
CREDITS : 04	

Course Learning Objectives: This course will enable students to

- Understand and analyse concepts of Analog Modulation schemes viz; AM, FM, Low pass sampling and Quantization as a random process.
- Understand and analyse concepts digitization of signals viz; sampling, quantizing and encoding.
- Evolve the concept of SNR in the presence of channel induced noise and study Demodulation of analog modulated signals.
- Evolve the concept of quantization noise for sampled and encoded signals and study the concepts of reconstruction from these samples at a receiver.

Module-1

AMPLITUDE MODULATION: Introduction, Amplitude Modulation: Time & Frequency Domain description, Switching modulator, Envelop detector. **(3.1 – 3.2 in Text)**

DOUBLE SIDE BAND-SUPPRESSED CARRIER MODULATION: Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing. **(3.3 – 3.4 in Text)**

SINGLE SIDE–BAND AND VESTIGIAL SIDEBAND METHODS OF MODULATION: SSB Modulation, VSB Modulation, Frequency Translation, Frequency- Division Multiplexing,Theme Example: VSB Transmission of Analog and Digital Television. **(3.5 – 3.8 in Text)**

L1, L2, L3

Module-2

ANGLE MODULATION: Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM, Transmission bandwidth of FM Signals, Generation of FM Signals, Demodulation of FM Signals, FM Stereo Multiplexing, Phase–Locked Loop: Nonlinear model of PLL, Linear model of PLL, Nonlinear Effects in FM Systems. The Superheterodyne Receiver **(4.1 – 4.6 of Text)**

L1, L2, L3

Module-3

[Review of Mean, Correlation and Covariance functions of Random Processes. ***(No questions to be set on these topics)]***

NOISE - Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth **(5.10 in Text)**

NOISE IN ANALOG MODULATION: Introduction, Receiver Model, Noise in DSB-SC receivers. Noise in AM receivers, Threshold effect, Noise in FM receivers, Capture effect, FM threshold effect, FM threshold reduction, Pre-emphasis and De-emphasis in FM **(6.1 – 6.6 in Text)**

L1,L2,L3

Module-4

SAMPLING AND QUANTIZATION: Introduction, Why Digitize Analog Sources?, The Low pass Sampling process Pulse Amplitude Modulation. Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves.**(7.1 – 7.7 in Text)**

L1,L2,L3

Module-5

SAMPLING AND QUANTIZATION (Contd): The Quantization Random Process, Quantization Noise, Pulse–Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding, Filtering, Multiplexing; Delta Modulation **(7.8 – 7.10 in Text)**,

Application examples - (a) Video + MPEG **(7.11 in Text)** and (b) Vocoders **(refer Section 6.8 of Reference Book 1)**.

L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Analyze and compute performance of AM and FM modulation in the presence of noise at the receiver.
2. Analyze and compute performance of digital formatting processes with quantization noise.
3. Multiplex digitally formatted signals at Transmitter.
4. Demultiplex the signals and reconstruct digitally formatted signals at the receiver.
5. Design /Demonstrate the use of digital formatting in Multiplexers, Vocoders and Video transmission.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.

- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. "Communication Systems", Simon Haykin & Moher, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.

Reference Books:

1. Modern Digital and Analog Communication Systems, B. P. Lathi, Oxford University Press, 4th edition.
2. An Introduction to Analog and Digital Communication, Simon Haykin, John Wiley India Pvt. Ltd., 2008, ISBN 978–81–265–3653–5.
3. Principles of Communication Systems, H.Taub & D.L.Schilling, TMH, 2011.
4. Communication Systems, Harold P.E, Samy A. Mahmoud, Lee Elliott Stern, Pearson Edition, 2004.

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INFORMATION THEORY and CODING

Course Code	: **18EC54**	CIE Marks	:40
Lecture Hours/Week	: 3	SEE Marks	:60
Total Number of Lecture Hours : 40 (8 Hrs / Module)		Exam Hours	:03
CREDITS – 03			

Course Learning Objectives: This course will enable students to

- Understand the concept of Entropy, Rate of information and order of the source with reference to dependent and independent source.
- Study various source encoding algorithms.
- Model discrete & continuous communication channels.
- Study various error control coding algorithms.

Module-1

Information Theory: Introduction, Measure of information, Information content of message, Average Information content of symbols in Long Independent sequences, Average Information content of symbols in Long dependent seqùences, Markov Statistical Model for Information Sources, Entropy and Information rate of Markoff Sources

(Section 4.1, 4.2 of Text 1) **L1, L2,L3**

Module-2

Source Coding: Encoding of the Source Output, Shannon's Encoding Algorithm**(Sections 4.3, 4.3.1 of Text 1),** Shannon Fano Encoding Algorithm **(Section 2.15 of Reference Book 4)**

Source coding theorem, Prefix Codes, Kraft McMillan Inequality property – KMI, Huffman codes **(Section 2.2 of Text 2)**

L1, L2, L3

Module-3

Information Channels: Communication Channels, Discrete Communication channels Channel Matrix, Joint probabilty Matrix, Binary Symmetric Channel, System Entropies. **(Section 4.4, 4.5, 4.51,4.5.2 of Text 1)**

Mutual Information, Channel Capacity, Channel Capacity of Binary Symmetric Channel, **(Section 2.5, 2.6 of Text 2)**

Binary Erasure Channel, Muroga's Theorem **(Section 2.27, 2.28 of Reference Book 4)**

L1, L2, L3

Module-4

Error Control Coding:
Introduction, Examples of Error control coding, methods of Controlling Errors, Types of Errors, types of Codes, Linear Block Codes: matrix description of Linear Block Codes, Error detection & Correction capabilities of Linear Block Codes, Single error correction Hamming code, Table lookup Decoding using Standard Array.

Binary Cyclic Codes: Algebraic Structure of Cyclic Codes, Encoding using an (n-k) Bit Shift register, Syndrome Calculation, Error Detection and Correction **(Sections 9.1, 9.2,9.3,9.3.1,9.3.2,9.3.3 of Text 1)** ,

L1, L2, L3

Module-5

Convolution Codes: Convolution Encoder, Time domain approach, Transform domain approach, Code Tree, Trellis and State Diagram, The Viterbi Algorithm) **(Section 8.5 – Articles 1, 2 and 3, 8.6- Article 1 of Text 2),**

L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

1. Explain concept of Dependent & Independent Source, measure of information, Entropy, Rate of Information and Order of a source
2. Represent the information using Shannon Encoding, Shannon Fano, Prefix and Huffman Encoding Algorithms
3. Model the continuous and discrete communication channels using input, output and joint probabilities
4. Determine a codeword comprising of the check bits computed using Linear Block codes, cyclic codes & convolutional codes
5. Design the encoding and decoding circuits for Linear Block codes, cyclic codes, convolutional codes, BCH and Golay codes.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Digital and Analog Communication Systems, K. Sam Shanmugam, John Wiley India Pvt. Ltd, 1996.
2. Digital Communication, Simon Haykin, John Wiley India Pvt. Ltd, 2008.

Reference Books:

1. ITC and Cryptography, Ranjan Bose, TMH, II edition, 2007
2. Principles of Digital Communication, J. Das, S. K. Mullick, P. K. Chatterjee, Wiley, 1986 - Technology & Engineering
3. Digital Communications – Fundamentals and Applications, Bernard Sklar, Second Edition, Pearson Education, 2016, ISBN: 9780134724058.
4. Information Theory and Coding, HariBhat, Ganesh Rao, Cengage, 2017.
5. Error Correction Coding, Todd K Moon, Wiley Std. Edition, 2006

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ELECTROMAGNETIC WAVES

Course Code	: 18EC55	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (8 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Study the different coordinate systems, Physical significance of Divergence, Curl and Gradient.
- Understand the applications of Coulomb's law and Gauss law to different charge distributions and the applications of Laplace's and Poisson's Equations to solve real time problems on capacitance of different charge distributions.
- Understand the physical significance of Biot-Savart's, Ampere's Law and Stokes' theorem for different current distributions.
- Infer the effects of magnetic forces, materials and inductance.
- Know the physical interpretation of Maxwell's equations and applications for Plane waves for their behavior in different media.
- Acquire knowledge of Poynting theorem and its application of power flow.

Module-1

Revision of Vector Calculus – **(Text 1: Chapter 1)**

Coulomb's Law, Electric Field Intensity and Flux density: Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge distribution, Field of a line charge, Field due to Sheet of charge, Electric flux density, Numerical Problems. **(Text: Chapter 2.1 to 2.5, 3.1)**

L1, L2, L3

Module-2

Gauss's law and Divergence: Gauss law, Application of Gauss law to point charge, line charge, Surface charge and volume charge, Point (differential) form of Gauss law, Divergence. Maxwell's First equation (Electrostatics), Vector Operator ∇ and divergence theorem, Numerical Problems **(Text: Chapter 3.2 to 3.7).**

Energy, Potential and Conductors: Energy expended or work done in moving a point charge in an electric field, The line integral, Definition of potential difference and potential, The potential field of point charge, Potential gradient, Numerical Problems **(Text: Chapter 4.1 to 4.4 and 4.6).** Current and Current density, Continuity of current. **(Text: Chapter 5.1, 5.2)**

L1, L2, L3

Module-3

Poisson's and Laplace's Equations: Derivation of Poisson's and Laplace's Equations, Uniqueness theorem, Examples of the solution of Laplace's equation, Numerical problems on Laplace equation **(Text: Chapter 7.1 to 7.3)**

Steady Magnetic Field: Biot-Savart Law, Ampere's circuital law, Curl, Stokes' theorem, Magnetic flux and magnetic flux density, Basic concepts Scalar and Vector Magnetic Potentials, Numerical problems. **(Text: Chapter 8.1 to 8.6)**

L1, L2, L3

Module-4

Magnetic Forces: Force on a moving charge, differential current elements, Force between differential current elements, Numerical problems **(Text: Chapter 9.1 to 9.3).**

Magnetic Materials: Magnetization and permeability, Magnetic boundary conditions, The magnetic circuit, Potential energy and forces on magnetic materials, Inductance and mutual reactance, Numerical problems **(Text: Chapter 9.6 to 9.7).**

Faraday' law of Electromagnetic Induction –Integral form and Point form, Numerical problems **(Text: Chapter 10.1)**

L1, L2, L3

Module-5

Maxwell's equations Continuity equation, Inconsistency of Ampere's law with continuity equation, displacement current, Conduction current, Derivation of Maxwell's equations in point form, and integral form, Maxwell's equations for different media, Numerical problems **(Text: Chapter 10.2 to 10.4)**

Uniform Plane Wave: Plane wave, Uniform plane wave, Derivation of plane wave equations from Maxwell's equations, Solution of wave equation for perfect dielectric, Relation between E and H, Wave propagation in free space, Solution of wave equation for sinusoidal excitation, wave propagation in any conducting media (γ, α, β, η) and good conductors, Skin effect or Depth of penetration, Poynting's theorem and wave power, Numerical problems. **(Text: Chapter 12.1 to 12.4)**

L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

1. Evaluate problems on electrostatic force, electric field due to point, linear, volume charges by applying conventional methods and charge in a volume.
2. Apply Gauss law to evaluate Electric fields due to different charge distributions and Volume Charge distribution by using Divergence Theorem.

3. Determine potential and energy with respect to point charge and capacitance using Laplace equation and Apply Biot-Savart's and Ampere's laws for evaluating Magnetic field for different current configurations
4. Calculate magnetic force, potential energy and Magnetization with respect to magnetic materials and voltage induced in electric circuits.
5. Apply Maxwell's equations for time varying fields, EM waves in free space and conductors and Evaluate power associated with EM waves using Poynting theorem

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. W.H. Hayt and J.A. Buck, —Engineering Electromagnetics, 8th Edition, Tata McGraw-Hill, 2014, ISBN-978-93-392-0327-6.

Reference Books:

1. Elements of Electromagnetics – Matthew N.O., Sadiku, Oxford university press, 4th Edn.
2. Electromagnetic Waves and Radiating systems – E. C. Jordan and K.G. Balmain, PHI, 2nd Edn.
3. Electromagnetics- Joseph Edminister, Schaum Outline Series, McGraw Hill.
4. Fundamentals of Electromagnetics for Engineering - N. Narayana Rao, Pearson.

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Verilog HDL

Course Code	: 18EC56	CIE Marks	:40
Lecture Hours/Week	: 03	SEE Marks	:60
Total Number of Lecture Hours	: 40 (08 Hrs/Module)	Exam Hours	:03
	CREDITS–03		

Course Learning Objectives: This course will enable students to:

- Learn different Verilog HDL constructs.
- Familiarize the different levels of abstraction in Verilog.
- Understand Verilog Tasks, Functions and Directives.
- Understand timing and delay Simulation.
- Understand the concept of logic synthesis and its impact in verification

Module 1

Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL-flow, why Verilog HDL?, trends in HDLs.
Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block. **L1,L2,L3**

Module 2

Basic Concepts: Lexical conventions, data types, system tasks, compiler directives.
Modules and Ports: Module definition, port declaration, connecting ports, hierarchical name referencing **L1,L2,L3**

Module 3

Gate-Level Modeling: Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays.
Dataflow Modeling: Continuous assignments, delay specification, expressions, operators, operands, operator types. **L1,L2,L3**

Module 4

Behavioral Modeling: Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks.
Tasks and Functions: Differences between tasks and functions, declaration, invocation, automatic tasks and functions. **L1,L2,L3**

Module 5

Useful Modeling Techniques: Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks.
Logic Synthesis with Verilog: Logic Synthesis, Impact of logic synthesis, Verilog HDL Synthesis, Synthesis design flow, Verification of Gate-Level Netlist. **(Chapter 14 till 14.5 of Text).** **L1,L2,L3**

Course Outcomes: At the end of this course, students will be able to

1. Write Verilog programs in gate, dataflow (RTL), behavioral and switch modeling levels of Abstraction.
2. Design and verify the functionality of digital circuit/system using test benches.
3. Identify the suitable Abstraction level for a particular digital design.
4. Write the programs more effectively using Verilog tasks, functions and directives.
5. Perform timing and delay Simulation and Interpret the various constructs in logic synthesis.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Samir Palnitkar, **"Verilog HDL: A Guide to Digital Design and Synthesis"**, Pearson Education, Second Edition.

Reference Books:

1. Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer Science+Business Media, LLC, Fifth edition.
2. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.
3. Padmanabhan, Tripura Sundari, "Design through Verilog HDL", Wiley, 2016 or earlier.

D. V.

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DIGITAL SIGNAL PROCESSING LABORATORY

Course Code : **18ECL57**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to

- Simulate discrete time signals and verification of sampling theorem.
- Compute the DFT for a discrete signal and verification of its properties using MATLAB.
- Find solution to the difference equations and computation of convolution and correlation along with the verification of properties.
- Compute and display the filtering operations and compare with the theoretical values.
- Implement the DSP computations on DSP hardware and verify the result.

Laboratory Experiments

Following Experiments to be done using MATLAB / SCILAB / OCTAVE or equivalent:

1. Verification of sampling theorem (use interpolation function).
2. Linear and circular convolution of two given sequences, Commutative, distributive and associative property of convolution.
3. Auto and cross correlation of two sequences and verification of their properties
4. Solving a given difference equation.
5. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum (using DFT equation and verify it by built-in routine).
6. (i) Verification of DFT properties (like Linearity and Parseval's theorem, etc.)
   (ii) DFT computation of square pulse and Sinc function etc.

7. Design and implementation of Low pass and High pass FIR filter to meet the desired specifications (using different window techniques) and test the filter with an audio file. Plot the spectrum of audio signal before and after filtering.

8. Design and implementation of a digital IIR filter (Low pass and High pass) to meet given specifications and test with an audio file. Plot the spectrum of audio signal before and after filtering.

Following Experiments to be done using DSP kit

9. Obtain the Linear convolution of two sequences.
10. Compute Circular convolution of two sequences.
11. Compute the N-point DFT of a given sequence.
12. Determine the Impulse response of first order and second order system.
13. Generation of sine wave and standard test signals

Course Outcomes:

On the completion of this laboratory course, the students will be able to:

1. Understand the concepts of analog to digital conversion of signals and frequency domain sampling of signals.
2. Model the discrete time signals and systems and verify its properties and results.
3. Implement discrete computations using DSP processor and verify the results.
4. Realize the digital filters using a simulation tool and analyze the response of the filter for an audio signal.
5. Write programs using Matlab / Scilab/Octave to illustrate DSP concepts.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
3. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Reference Books:

1. Vinay K Ingle, John G Proakis, Digital Signal Processing using MATLAB, Fourth Edition, Cengage India Private Limited, 2017.

D. V. 9

HDL LABORATORY

Course Code : **18ECL58**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:

- Familiarize with the CAD tool to write HDL programs.
- Understand simulation and synthesis of digital design.
- Program FPGAs/CPLDs to synthesize the digital designs.
- Interface hardware to programmable ICs through I/O ports.
- Choose either Verilog or VHDL for a given Abstraction level.

Note: Programming can be done using any compiler. Download the programs on a FPGA/CPLD board and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

PART A

1. Write Verilog program for the following combinational design along with test bench to verify the design:
   a. 2 to 4 decoder realization using NAND gates only (structural model)
   b. 8 to 3 encoder with priority and without priority (behavioural model)
   c. 8 to 1 multiplexer using case statement and if statements
   d. 4-bit binary to gray converter using 1-bit gray to binary converter 1-bit adder and subtractor
2. Model in Verilog for a full adder and add functionality to perform logical operations of XOR, XNOR, AND and OR gates. Write test bench with appropriate input patterns to verify the modeled behaviour.
3. Verilog 32-bit ALU shown in figure below and verify the functionality of ALU by selecting appropriate test patterns. The functionality of the ALU is presented in Table 1.
   a. Write test bench to verify the functionality of the ALU considering all possible input patterns
   b. The enable signal will set the output to required functions if enabled, if disabled all the outputs are set to tri-state
   c. The acknowledge signal is set high after every operation is complete

D. V. T

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B. E. 2018 Scheme Sixth Semester Syllabus (EC)

Choice Based Credit System (CBCS) and Outcome Based Education (OBE)

SEMESTER – VI

DIGITAL COMMUNICATION

Course Code	: 18EC61	CIE Marks : 40
Lecture Hours/Week	: 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)		Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to:

- Understand the mathematical representation of signal, symbol, and noise.
- Understand the concept of signal processing of digital data and signal conversion to symbols at the transmitter and receiver.
- Compute performance metrics and parameters for symbol processing and recovery in ideal and corrupted channel conditions.
- Compute performance parameters and mitigate channel induced impediments in corrupted channel conditions.

Module-1

Bandpass Signal to Equivalent Low pass: Hilbert Transform, Pre-envelopes, Complex envelopes, Canonical representation of bandpass signals, Complex low pass representation of bandpass systems, Complex representation of band pass signals and systems **(Text 1: 2.8, 2.9, 2.10, 2.11, 2.12, 2.13).**

Line codes: Unipolar, Polar, Bipolar (AMI) and Manchester code and their power spectral densities **(Text 1: Ch 6.10).**
Overview of HDB3, B3ZS, B6ZS **(Ref. 1: 7.2)**

L1,L2,L3

Module-2

Signaling over AWGN Channels- Introduction, Geometric representation of signals, Gram-Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel, Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver **(Text 1: 7.1, 7.2, 7.3, 7.4).**

L1,L2,L3

Module – 3

Digital Modulation Techniques: Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M–ary PSK, M–ary QAM **(Relevant topics in Text 1 of 7.6, 7.7).**

Frequency shift keying techniques using Coherent detection: BFSK generation, detection and error probability **(Relevant topics in Text 1 of 7.8).**
Non coherent orthogonal modulation techniques: BFSK, DPSK Symbol representation, Block diagrams treatment of Transmitter and Receiver, Probability of error (without derivation of probability of error equation) **(Text 1: 7.11, 7.12. 7.13).**

L1,L2,L3

Module-4

Communication through Band Limited Channels: Digital Transmission through Band limited channels: Digital PAM Transmission through Band limited Channels, Signal design for Band limited Channels: Design of band limited signals for zero ISI–The Nyquist Criterion (statement only), Design of band limited signals with controlled ISI-Partial Response signals, Probability of error for detection of Digital PAM: Probability of error for detection of Digital PAM with Zero ISI, Symbol–by–Symbol detection of data with controlled ISI **(Text 2: 9.1, 9.2, 9.3.1, 9.3.2).**
Channel Equalization: Linear Equalizers (ZFE, MMSE), **(Text 2: 9.4.2).**

L1,L2,L3

Module-5

Principles of Spread Spectrum: Spread Spectrum Communication Systems: Model of a Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Systems, Effect of De-spreading on a narrowband Interference, Probability of error (statement only), Some applications of DS Spread Spectrum Signals, Generation of PN Sequences, Frequency Hopped Spread Spectrum, CDMA based on IS-95 **(Text 2: 11.3.1, 11.3.2, 11.3.3, 11.3.4, 11.3.5, 11.4.2).**

L1,L2,L3

Course Outcomes: At the end of the course, the students will be able to:

1. Associate and apply the concepts of Bandpass sampling to well specified signals and channels.
2. Analyze and compute performance parameters and transfer rates for low pass and bandpass symbol under ideal and corrupted non band limited channels.
3. Test and validate symbol processing and performance parameters at the receiver under ideal and corrupted bandlimited channels.

4. Demonstrate that bandpass signals subjected to corruption and distortion in a bandlimited channel can be processed at the receiver to meet specified performance criteria.
5. Understand the principles of spread spectrum communications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN 978-0-471-64735-5.
2. John G Proakis and Masoud Salehi, "Fundamentals of Communication Systems", 2014 Edition, Pearson Education, ISBN 978-8-131-70573-5.

Reference Books:

1. B.P.Lathi and Zhi Ding, "Modern Digital and Analog communication Systems", Oxford University Press, 4th Edition, 2010, ISBN: 978-0-198-07380-2.
2. Ian A Glover and Peter M Grant, "Digital Communications", Pearson Education, Third Edition, 2010, ISBN 978-0-273-71830-7.
3. Bernard Sklar and Ray, "Digital Communications - Fundamentals and Applications", Pearson Education, Third Edition, 2014, ISBN: 978-81-317-2092-9.

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EMBEDDED SYSTEMS

Course Code	: 18EC62	CIE Marks : 40
Lecture Hours/Week	: 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)		Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to:

- Explain the architectural features and instructions of 32 bit microcontroller -ARM Cortex M3.
- Develop Programs using the various instructions of ARM Cortex M3 and C language for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Develop the hardware software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

Module 1

ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence **(Text 1: Ch-1, 2, 3)**

L1,L2

Module 2

ARM Cortex M3 Instruction Sets and Programming: Assembly basics, Instruction list and description, Thumb and ARM instructions, Special instructions, Useful instructions, CMSIS, Assembly and C language Programming **(Text 1: Ch-4, Ch-10.1 to 10.6)**

L1,L2,L3

Module 3

Embedded System Components: Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Elements of an Embedded System (Block diagram and explanation), Differences between RISC and CISC, Harvard and Princeton, Big and Little Endian formats, Memory (ROM and RAM types), Sensors, Actuators, Optocoupler, Communication Interfaces (I2C, SPI, IrDA, Bluetooth, Wi-Fi, Zigbee only)

(Text 2: All the Topics from Ch-1 and Ch-2 (Fig and explanation before 2.1) 2.1.1.6 to 2.1.1.8, 2.2 to 2.2.2.3, 2.3 to 2.3.2, 2.3.3.3, selected topics of 2.4.1 and 2.4.2 only).

L1, L2

Module 4

Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modeling (excluding UML), Embedded firmware design and development (excluding C language). **Text 2: Ch-3, Ch-4 (4.1, 4.2.1 and 4.2.2 only), Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)**

L1,L2,L3

Module 5

RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques **(Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch-12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)**

L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.
2. Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
3. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
4. Develop the hardware software co-design and firmware design approaches.
5. Explain the need of real time operating system for embedded system applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", 2nd Edition, Newnes, (Elsevier), 2010.
2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2nd Edition.

Reference Books:

1. James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008, ISBN: 978-0-471-72180-2.
2. Yifeng Zhu, "Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C", 2nd Ed. Man Press LLC ©2015 ISBN: 0982692633 9780982692639.
3. K.V. K. K Prasad, Embedded Real Time Systems, Dreamtech publications, 2003.
4. Rajkamal, Embedded Systems, 2nd Edition, McGraw hill Publications, 2010.

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Mijar, MOODBIDRI - 574 225

MICROWAVE and ANTENNAS

Course Code	: 18EC63	CIE Marks : 40
Lecture Hours/Week	: 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)		Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to:

- Describe the microwave properties and its transmission media
- Describe microwave devices for several applications
- Understand the basics of antenna theory
- Select antennas for specific applications

Module 1

Microwave Tubes: Introduction, Reflex Klystron Oscillator, Mechanism of Oscillations, Modes of Oscillations, Mode Curve (Qualitative Analysis only). **(Text 1: 9.1, 9.2.1)**

Microwave Transmission Lines: Microwave Frequencies, Microwave devices, Microwave Systems, Transmission Line equations and solutions, Reflection Coefficient and Transmission Coefficient, Standing Wave and Standing Wave Ratio, Smith Chart, Single Stub matching.
(Text 2: 0.1, 0.2, 0.3, 3.1, 3.2, 3.3, 3.5, 3.6 Except Double stub matching)
L1,L2

Module 2

Microwave Network theory: Introduction, Symmetrical Z and Y-Parameters for reciprocal Networks, S matrix representation of Multi-Port Networks. **(Text1: 6.1, 6.2, 6.3)**

Microwave Passive Devices: Coaxial Connectors and Adapters, Attenuators, Phase Shifters, Waveguide Tees, Magic tees.
(Text 1: 6.4.2,6.4.14, 6.4.15, 6.4.16) **L1,L2**

Module 3

Strip Lines: Introduction, Micro Strip lines, Parallel Strip lines, Coplanar Strip lines, Shielded Strip Lines. **(Text 2: 11.1, 11.2, 11.3, 11.4)**

Antenna Basics: Introduction, Basic Antenna Parameters, Patterns, Beam Area, Radiation Intensity, Beam Efficiency, Directivity and Gain, Antenna Apertures, Effective Height, Radio Communication Link, Antenna Field Zones. **(Text 3: 2.1 - 2.7, 2.9 – 2.11, 2.13)** **L1,L2,L3**

Module 4

Point Sources and Arrays: Introduction, Point Sources, Power Patterns, Power Theorem, Radiation Intensity, Arrays of two isotropic point sources, Linear Arrays of n Isotropic Point Sources of equal Amplitude and Spacing.
(Text 3: 5.1 – 5.6, 5.9, 5.13)

Electric Dipoles: Introduction, Short Electric Dipole, Fields of a Short Dipole, Radiation Resistance of a Short Electric Dipole, Thin Linear Antenna (Field Analyses)
(Text 3: 6.1 - 6.5)

L1,L2,L3,L4

Module 5

Loop and Horn Antenna: Introduction, Small loop, The Loop Antenna General Case, The Loop Antenna as a special case, Radiation resistance of loops, Directivity of Circular Loop Antennas with uniform current, Horn antennas Rectangular Horn Antennas.
(Text 3: 7.1, 7.2, 7.4, 7.6, 7.7, 7.8, 7.19, 7.20)

Antenna Types: The Helix geometry, Helix modes, Practical Design considerations for the mono-filar axial mode Helical Antenna, Yagi-Uda array, Parabolic reflector
(Text 3: 8.3, 8.4, 8.5, 8.8, 9.5)

L1,L2,L3

Course outcomes: At the end of the course students will be able to:

1. Describe the use and advantages of microwave transmission
2. Analyze various parameters related to microwave transmission lines and waveguides
3. Identify microwave devices for several applications
4. Analyze various antenna parameters necessary for building a RF system
5. Recommend various antenna configurations according to the applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. **Microwave Engineering** – Annapurna Das, Sisir K Das, TMH, Publication, 2nd, 2010.
2. **Microwave Devices and circuits**- Samuel Y Liao, Pearson Education
3. **Antennas and Wave Propagation**- John D. Krauss, Ronald J Marhefka, Ahmad S Khan, 4th Edition, McGraw Hill Education, 2013

Reference Books:

1. **Microwave Engineering** - David M Pozar, John Wiley India Pvt. Ltd., 3rd Edn, 2008.
2. **Microwave Engineering** – Sushrut Das, Oxford Higher Education, 2nd Edn, 2015
3. **Antennas and Wave Propagation** – Harish and Sachidananda: Oxford University Press, 2007

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Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

EMBEDDED SYSTEMS LABORATORY

Course Code : **18ECL66**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS– 02		

Course Learning Objectives: This course will enable students to:

- Understand the instruction set of ARM Cortex M3, a 32 bit microcontroller and the software tool required for programming in Assembly and C language.
- Program ARM Cortex M3 using the various instructions in assembly level language for different applications.
- Interface external devices and I/O with ARM Cortex M3.
- Develop C language programs and library functions for embedded system applications.

Laboratory Experiments

Conduct the following experiments on an ARM CORTEX M3 evaluation board to learn ALP and using evaluation version of Embedded 'C' & Keil uVision-4 tool/compiler.

PART A:

1. ALP to multiply two 16 bit binary numbers.
2. ALP to find the sum of first 10 integer numbers.
3. ALP to find the number of 0's and 1's in a 32 bit data
4. ALP to find determine whether the given 16 bit is even or odd
5. ALP to write data to RAM

PART B:

6. Display "Hello world" message using internal UART
7. Interface and Control the speed of a DC Motor.
8. Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.
9. Interface a DAC and generate Triangular and Square waveforms.
10. Interface a 4x4 keyboard and display the key code on an LCD.
11. Demonstrate the use of an external interrupt to toggle an LED On/Off.
12. Display the Hex digits 0 to F on a 7-segment LED interface, with an appropriate delay.
13. Measure Ambient temperature using a sensor and SPI ADC IC.

Course outcomes: After studying this course, students will be able to:

1. Understand the instruction set of 32 bit microcontroller ARM Cortex M3, and the software tool required for programming in Assembly and C language.
2. Develop assembly language programs using ARM Cortex M3 for different applications.
3. Interface external devices and I/O with ARM Cortex M3.
4. Develop C language programs and library functions for embedded system applications.
5. Analyze the functions of various peripherals, peripheral registers and power saving modes of ARM Cortex M3

Conduction of Practical Examination:

- One Question from PART A and one Question from PART B to be asked in the examination.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

H. O. D.
Dept. Of Electronics & Communication
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

COMMUNICATION LABORATORY

Course Code : **18ECL67**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:

- Design and test the communication circuits for different analog modulation schemes.
- Design and demonstrate the digital modulation techniques
- Demonstrate and measure the wave propagation in microstrip antennas
- Characteristics of microstrip devices and measurement of its parameters.
- Understand the probability of error computations of coherent digital modulation schemes.

Laboratory Experiments

PART-A: Expt. 1 to Expt. 5 have to be performed using discrete components.

1. Amplitude Modulation and Demodulation: i) Standard AM, ii)DSBSC (LM741 and LF398 ICs can be used)
2. Frequency modulation and demodulation (IC 8038/2206 can be used)
3. Pulse sampling, flat top sampling and reconstruction
4. Time Division Multiplexing and Demultiplexing of two bandlimited signals.
5. FSK and PSK generation and detection
6. Measurement of frequency, guide wavelength, power, VSWR and attenuation in microwave test bench.
7. Obtain the Radiation Pattern and Measurement of directivity and gain of microstrip dipole and Yagi antennas.
8. Determination of
   a. Coupling and isolation characteristics of microstrip directional coupler.
   b. Resonance characteristics of microstrip ring resonator and computation of dielectric constant of the substrate.
   c. Power division and isolation of microstrip power divider.

PART-B: Simulation Experiments using SCILAB/MATLAB/Simulink or LabVIEW

1. To Simulate NRZ, RZ, half-sinusoid & raised cosine pulses and generate eye diagram for binary polar signaling.
2. Pulse code modulation and demodulation system.

3. Computations of the Probability of bit error for coherent binary ASK, FSK and PSK for an AWGN Channel and compare them with their performance curves.
4. Digital Modulation Schemes i) DPSK Transmitter and Receiver, ii) QPSK Transmitter and Receiver.

Course Outcomes: On the completion of this laboratory course, the students will be able to:

1. Design and test circuits for analog modulation and demodulation schemes viz., AM, FM, etc.
2. Determine the characteristics and response of microwave waveguide.
3. Determine characteristics of microstrip antennas and devices & compute the parameters associated with it.
4. Design and test the digital and analog modulation circuits and display the waveforms.
5. Simulate the digital modulation systems and compare the error performance of basic digital modulation schemes.

Conduct of Practical Examination:

- All laboratory experiments are to be considered for practical examination.
- For examination one question from **PART-A** and one question from **PART-B or** only one question from **PART-B** experiments based on the complexity, to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

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VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination 2018 – 19
Outcome Based Education(OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2018 – 19)

VI SEMESTER

Sl. No	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P					
1	PCC	18EC61	Digital Communication		3	2	--	03	40	60	100	4
2	PCC	18EC62	Embedded Systems		3	2	--	03	40	60	100	4
3	PCC	18EC63	Microwave & Antennas		3	2	--	03	40	60	100	4
4	PEC	18XX64X	Professional Elective -1		3	--	--	03	40	60	100	3
5	OEC	18XX65X	Open Elective –A		3	--	--	03	40	60	100	3
6	PCC	18ECL66	Embedded Systems Laboratory		--	2	2	03	40	60	100	2
7	PCC	18ECL67	Communication Laboratory		--	2	2	03	40	60	100	2
8	MP	18ECMP68	Mini-project		--	--	2	03	40	60	100	2
9	Internship	--	Internship	To be carried out during the vacation/s of VI and VII semesters and /or VII and VIII semesters.								
				TOTAL	15	10	6	24	320	480	800	24

Note: PCC: Professional core, PEC: Professional Elective, OE: Open Elective, MP: Mini-project.

Professional Elective -1

Course code under 18XX64X	Course Title
18EC641	Operating System
18EC642	Artificial Neural Networks
18EC643	Object Oriented Programming using C++
18EC644	Digital System Design using Verilog
18EC645	Nanoelectronics

Open Elective –A

(i) 18EC651 Signal Processing (ii)18EC652 Sensors &Signal Conditioning

Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please refer to the list of open electives under 18XX65X).

Selection of an open elective shall not be allowed if,

- The candidate has studied the same course during the previous semesters of the programme.
- The syllabus content of open elective is similar to that of the Departmental core courses or professional electives.
- A similar course, under any category, is prescribed in the higher semesters of the programme.

Registration to electives shall be documented under the guidance of Programme Coordinator/ Advisor/Mentor.

Mini-project work:

Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini- project can be assigned to an individual student or to a group having not more than 4 students.

CIE procedure for Mini-project:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the Mini-project work, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all the guides of the college.

The CIE marks awarded for the Mini-project, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

SEE for Mini-project:

(i) Single discipline: Contribution to the Mini-project and the performance of each group member shall be assessed individually in the semester end examination (SEE) conducted at the department.

(ii) Interdisciplinary: Contribution to the Mini-project and the performance of each group member shall be assessed individually in semester end examination (SEE) conducted separately at the departments to which the student/s belong to.

Internship: All the students admitted to III year of BE/B.Tech shall have to undergo mandatory internship of 4 weeks during the vacation of VI and VII semesters and /or VII and VIII semesters. A University examination shall be conducted during VIII semester and the prescribed credit shall be included in VIII semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

H. O. D.
Dept. Of Electronics & Communication
Ativa' Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

SEMESTER – VII
COMPUTER NETWORKS

Course Code	: 18EC71	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs/module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand the layering architecture of OSI reference model and TCP/IP protocol suite.
- Understand the protocols associated with each layer.
- Learn the different networking architectures and their representations.
- Learn the functions and services associated with each layer.

Module-1

Introduction: Data communication: Components, Data representation, Data flow, Networks: Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet.

(1.1,1.2, 1.3(1.3.1to 1.3.4 of Text)

Network Models: Protocol Layering: Scenarios, Principles, Logical Connections, TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP.

(2.1, 2.2, 2.3 of Text) **L1, L2**

Module-2

Data-Link Layer: Introduction: Nodes and Links, Services, Two Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services: Framing, Flow and Error Control, Data Link Layer Protocols: Simple Protocol, Stop and Wait protocol, Piggybacking.

(9.1, 9.2(9.2.1, 9.2.2), 11.1, 11.2of Text)

Media Access Control: Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA.**(12.1 of Text)**

Wired and Wireless LANs: Ethernet Protocol, Standard Ethernet. Introduction to wireless LAN: Architectural Comparison, Characteristics, Access Control.

(13.1, 13.2(13.2.1 to 13.2.5), 15.1 of Text) **L1,L2, L3**

Module-3

Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution, Forwarding of IP Packets: Based on destination Address and Label.

(18.1, 18.2, 18.4, 18.5.1, 18.5.2 of Text)

Network Layer Protocols: Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams. **(19.1of Text).**

Unicast Routing: Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing.

(20.1, 20.2of Text) L1,L2, L3

Module-4

Transport Layer: Introduction: Transport Layer Services, Connectionless and Connection oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-Back-N Protocol, Selective repeat protocol. **(23.1, 23.2.1, 23.2.2, 23.2.3, 23.2.4 of Text)**

Transport-Layer Protocols in the Internet:

User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Flow control, Error control, TCP congestion control.

(24.2, 24.3.1, 24.3.2, 24.3.3, 24.3.4, 24.3.5, 24.3.6, 24.3.7, 24.3.8, 24.3.9 of Text) L1,L2, L3

Module-5

Application Layer: Introduction: providing services, Application- layer paradigms, Standard Client –Server Protocols: World wide web, Hyper Text Transfer Protocol, FTP: Two connections, Control Connection, Data Connection, Electronic Mail: Architecture, Wed Based Mail, Telnet: Local versus remote logging.Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS, security of DNS.

(25.1, 26.1, 26.2, 26.3, 26.4, 26.6 of Text) L1, L2

Course Outcomes: At the end of the course, the students will be able to:

1. Understand the concepts of networking.
2. Describe the various networking architectures.
3. Identify the protocols and services of different layers.
4. Distinguish the basic network configurations and standards associated with each network.
5. Analyze a simple network and measure its parameters.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOK:

- Behrouz A Forouzan, "Data Communications and Networking", 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.

REFERENCE BOOKS:

1. James J Kurose, Keith W Ross, "Computer Networks", Pearson Education.
2. Wayne Tomasi, "Introduction to Data Communication and Networking", Pearson Education.
3. Andrew S Tanenbaum, "Computer Networks", Prentice Hall.
4. William Stallings, "Data and Computer Communications", Prentice Hall.

VLSI DESIGN

Course Code	: 18EC72	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40(08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: The objectives of the course is to enable students to:

- Impart knowledge of MOS transistor theory and CMOS technologies
- Learn the operation principles and analysis of inverter circuits.
- Design Combinational, sequential and dynamic logic circuits as per the requirements
- Infer the operation of Semiconductors Memory circuits.
- Demonstrate the concepts of CMOS testing

Module-1

Introduction: A Brief History, MOS Transistors, CMOS Logic **(1.1 to 1.4 of TEXT2)**

MOS Transistor Theory: Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics **(2.1, 2.2, 2.4 and 2.5 of TEXT2).**, **L1, L2**

Module-2

Fabrication: CMOS Fabrication and Layout, VLSI Design Flow, Introduction, CMOS Technologies, Layout Design Rules, **(1.5 and 3.1 to 3.3 of TEXT2).**

MOSFET Scaling and Small-Geometry Effects, MOSFET Capacitances **(3.5 to 3.6 of TEXT1),** **L1, L2,**

Module-3

Delay: Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths **(4.1 to 4.5 of TEXT2, except sub-sections 4.3.7, 4.4.5, 4.4.6, 4.5.5 and 4.5.6).**

Combinational Circuit Design: Introduction, Circuit families **(9.1 to 9.2 of TEXT2, except subsection 9.2.4).**, **L1, L2, L3**

Module-4

Sequential Circuit Design: Introduction, Circuit Design for Latches and Flip-Flops **(10.1 and 10.3.1 to 10.3.4 of TEXT2)**

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques **(9.1, 9.2, 9.4 to 9.5 of TEXT1)**, **L1, L2, L3**

Module-5

Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM),
(10.1 to 10.3 of TEXT1)
Testing and Verification: Introduction, Logic Verification Principles, Manufacturing Test Principles, Design for testability
(15.1, 15.3, 15.5 15.6.1 to 15.6.3 of TEXT 2). L1, L2

Course outcomes: At the end of the course, the students will be able to:

1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
2. Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
3. Demonstrate ability to design Combinational, sequential and dynamic logic circuits as per the requirements
4. Interpret Memory elements along with timing considerations
5. Interpret testing and testability issues in VLSI Design

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOKS:

1. "CMOS Digital Integrated Circuits: Analysis and Design" - **Sung Mo Kang & Yosuf Leblebici,** Third Edition, Tata McGraw-Hill.
2. **"CMOS VLSI Design- A Circuits and Systems Perspective"-** Neil H. E. Weste and David Money Harris, 4th Edition, Pearson Education.

REFERENCE BOOKS:

1. Adel Sedra and K. C. Smith, "Microelectronics Circuits Theory and Applications", 6th or 7th Edition, Oxford University Press, International Version, 2009.
2. Douglas A Pucknell & Kamran Eshragian, "Basic VLSI Design", PHI 3rd Edition, (original Edition – 1994).
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.

COMPUTER NETWORKS LAB

Course Code : **18ECL76**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:

- Choose suitable tools to model a network and understand the protocols at various OSI reference levels.
- Design a suitable network and simulate using a Network simulator tool.
- Simulate the networking concepts and protocols using C/C++ programming.
- Model the networks for different configurations and analyze the results.

Laboratory Experiments

PART-A: Simulation experiments using NS2/ NS3/ OPNET/ NCTUNS/ NetSim/QualNet or any other equivalent tool

1. Implement a point to point network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.
2. Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent by TCP/UDP.
3. Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.
4. Implement Ethernet LAN using n nodes and assign multiple traffic to the nodes and obtain congestion window for different sources/ destinations.
5. Implement ESS with transmission nodes in Wireless LAN and obtain the performance parameters.
6. Implementation of Link state routing algorithm.

PART-B: Implement the following in C/C++

1. Write a program for a HLDC frame to perform the following.
   i) Bit stuffing
   ii) Character stuffing.
2. Write a program for distance vector algorithm to find suitable path for transmission.
3. Implement Dijkstra's algorithm to compute the shortest routing path.

4. For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify the program for the cases
   a. Without error
   b. With error
5. Implementation of Stop and Wait Protocol and Sliding Window Protocol
6. Write a program for congestion control using leaky bucket algorithm.

Course outcomes: On the completion of this laboratory course, the students will be able to:

1. Choose suitable tools to model a network.
2. Use the network simulator for learning and practice of networking algorithms.
3. Illustrate the operations of network protocols and algorithms using C programming.
4. Simulate the network with different configurations to measure the performance parameters.
5. Implement the data link and routing protocols using C programming.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination one question from software and one question from hardware or only one hardware experiments based on the complexity to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

VLSI LABORATORY

Course Code : **18ECL77**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:

- Design, model, simulate and verify CMOS digital circuits
- Design layouts and perform physical verification of CMOS digital circuits
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist
- Perform RTL-GDSII flow and understand the stages in ASIC design

Experiments can be conducted using any of the following or equivalent design tools: Cadence/Synopsis/Mentor Graphics/Microwind

Laboratory Experiments

Part – A

Analog Design

Use any VLSI design tools to carry out the experiments, use library files and technology files below 180 nm.

1.a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following:

i. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time period of 20ns and plot the input voltage and output voltage of designed inverter?

ii. From the simulation results compute tpHL, tpLH and td for all three geometrical settings of width?

iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter?

1. b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

2. a) Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 1. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.

2. b) Draw layout of NAND with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

3. a) Capture schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measures the Unity Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB.

3. b) Draw layout of common source amplifier, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

4.a) Capture schematic of two-stage operational amplifier and measure the following:

i. UGB
ii. dB bandwidth
iii. Gain margin and phase margin with and without coupling capacitance
iv. Use the op-amp in the inverting and non-inverting configuration and verify its functionality
v. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations.

4.b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in 4.a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

Part - B

Digital Design

Carry out the experiments using semicustom design flow or ASIC design flow, use technology library 180/90/45nm and below

Note: The experiments can also be carried out using FPGA design flow, it is required to set appropriate constraints in FPGA advanced synthesis options

1. Write verilog code for 4-bit up/down asynchronous reset counter and carry out the following:
   a. Verify the functionality using test bench
   b. Synthesize the design by setting area and timing constraint. Obtain

the gate level netlist, find the critical path and maximum frequency of operation. Record the area requirement in terms of number of cells required and properties of each cell in terms of driving strength, power and area requirement.

c. Perform the above for 32-bit up/down counter and identify the critical path, delay of critical path, and maximum frequency of operation, total number of cells required and total area.

2. Write verilog code for 4-bit adder and verify its functionality using test bench. Synthesize the design by setting proper constraints and obtain the net list. From the report generated identify critical path, maximum delay, total number of cells, power requirement and total area required. Change the constraints and obtain optimum synthesis results.
3. Write verilog code for UART and carry out the following:
   a. Perform functional verification using test bench
   b. Synthesize the design targeting suitable library and by setting area and timing constraints
   c. For various constrains set, tabulate the area, power and delay for the synthesized netlist
   d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints
4. Write verilog code for 32-bit ALU supporting four logical and four arithmetic operations, use case statement and if statement for ALU behavioral modeling.
   a. Perform functional verification using test bench
   b. Synthesize the design targeting suitable library by setting area and timing constraints
   c. For various constrains set, tabulate the area, power and delay for the synthesized netlist
   d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints

   Compare the synthesis results of ALU modeled using IF and CASE statements.
5. Write verilog code for Latch and Flip-flop, Synthesize the design and compare the synthesis report (D, SR, JK).
6. For the synthesized netlist carry out the following for any two above experiments:
   a. Floor planning (automatic), identify the placement of pads
   b. Placement and Routing, record the parameters such as no. of layers used for routing, flip method for placement of standard cells, placement of standard cells, routes of power and ground, and routing of standard cells
   c. Physical verification and record the LVS and DRC reports

d. Perform Back annotation and verify the functionality of the design
e. Generate GDSII and record the number of masks and its color composition

Course Outcomes: On the completion of this laboratory course, the students will be able to:

1. Design and simulate combinational and sequential digital circuits using Verilog HDL
2. Understand the Synthesis process of digital circuits using EDA tool.
3. Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list
4. Design and simulate basic CMOS circuits like inverter, common source amplifier and differential amplifiers.
5. Perform RTL-GDSII flow and understand the stages in ASIC design.

DSP ALGORITHMS and ARCHITECTURE

Course Code	: 18EC734	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Figure out the knowledge and concepts of digital signal processing techniques.
- Understand the computational building blocks of DSP processors and its speed issues.
- Understand the various addressing modes, peripherals, interrupts and pipelining structure of TMS320C54xx processor.
- Learn how to interface the external devices to TMS320C54xx processor in various modes.
- Understand basic DSP algorithms with their implementation.

Module -1

Introduction to Digital Signal Processing:

Introduction, A Digital Signal – Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation.

Computational Accuracy in DSP Implementations:

Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementation.

L1,L2

Module -2

Architectures for Programmable Digital Signal – Processing Devices:

Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.

L1,L2

Module -3

Programmable Digital Signal Processors:

Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54XX, Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and

Programming, On – Chip Peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor.

L1,L2

Module -4

Implementation of Basic DSP Algorithms:

Introduction, The Q – notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case).

Implementation of FFT Algorithms:

Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit – Reversed Index. Generation & Implementation on the TMS32OC54xx.

L1,L2

Module -5

Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices:

Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA).

Interfacing and Applications of DSP Processors:

Introduction, Synchronous Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System.

L1,L2

Course Outcomes: At the end of this course, students would be able to:

1. Comprehend the knowledge and concepts of digital signal processing techniques.
2. Apply the knowledge of DSP computational building blocks to achieve speed in DSP architecture or processor.
3. Apply knowledge of various types of addressing modes, interrupts, peripherals and pipelining structure of TMS320C54xx processor.
4. Develop basic DSP algorithms using DSP processors.
5. Discuss about synchronous serial interface and multichannel buffered serial port (McBSP) of DSP device and demonstrate the programming of CODEC interfacing.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.

- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- "Digital Signal Processing", Avatar Singh and S. Srinivasan, Thomson Learning, 2004.

Reference Books:

1. "Digital Signal Processing: A practical approach", Ifeachor E. C., Jervis B. W Pearson-Education, PHI, 2002.
2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2nd, 2010
3. "Architectures for Digital Signal Processing", Peter Pirsch John Wiley, 2008

IoT & WIRELESS SENSOR NETWORKS

Course Code	: 18EC741	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Describe the OSI Model for IoT/M2M Systems.
- Understand the architecture and design principles for device supporting IoT.
- Develop competence in programming for IoT Applications.
- Identify the uplink and downlink communication protocols which best suits the specific application of IoT / WSNs.

Module-1

Overview of Internet of Things: IoT Conceptual Framework, IoT Architectural View, Technology Behind IoT, Sources of IoT,M2M communication, Examples of IoT. Modified OSI Model for the IoT/M2M Systems, data enrichment, data consolidation and device management at IoT/M2M Gateway, web communication protocols used by connected IoT/M2M devices, Message communication protocols (CoAP-SMS, CoAP-MQ, MQTT,XMPP) for IoT/M2M devices. – Refer Chapter 1, 2 and 3 of Text 1.

L1, L2

Module-2

Architecture and Design Principles for IoT: Internet connectivity, Internet-based communication,IPv4, IPv6,6LoWPAN protocol, IP Addressing in the IoT, Application layer protocols: HTTP, HTTPS,FTP,TELNET and ports.

Data Collection, Storage and Computing using a Cloud Platform: Introduction, Cloud computing paradigm for data collection, storage and computing, Cloud service models, IoT Cloud- based data collection, storage and computing services using Nimbits. - Refer Chapter 4 and 6 of Text 1.

L1, L2

Module-3

Prototyping and Designing Software for IoT Applications: Introduction, Prototyping Embedded device software, Programming Embedded Device Arduino Platform using IDE, Reading data from sensors and devices, Devices, Gateways, Internet and Web/Cloud services software development.

Programming MQTT clients and MQTT server. Introduction to IoT privacy

and security. Vulnerabilities, security requirements and threat analysis, IoT Security Tomography and layered attacker model. - Refer Chapter 9 and 10 of Text 1. **L1, L2, L3**

Module-4

Overview of Wireless Sensor Networks:

Challenges for Wireless Sensor Networks, Enabling Technologies for Wireless Sensor Networks.

Architectures: Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes, Operating Systems and Execution Environments, Network Architecture-Sensor Network Scenarios, Optimization Goals and Figures of Merit, Design principles for WSNs, Service interfaces of WSNs Gateway Concepts. - Refer Chapter 1, 2, 3 of Text 2.

L1, L2, L3

Module-5

Communication Protocols:

Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Contention based protocols(CSMA,PAMAS), Schedule based protocols (LEACH, SMACS, TRAMA) Address and Name Management in WSNs, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing, Hierarchical networks by clustering. - Refer Chapter 4, 5, 7 and 11 of Text 2.

L1, L2, L3

Course Outcomes: At the end of the course, students will be able to:

1. Understand choice and application of IoT & M2M communication protocols.
2. Describe Cloud computing and design principles of IoT.
3. Relate to MQTT clients, MQTT server and its programming.
4. Describe the architectures and its communication protocols of WSNs.
5. Identify the uplink and downlink communication protocols associated with specific application of IOT / WSNs

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4sub questions.
- There will be 2 full questions from each module covering all the topics of the module.

- Students will have to answer 5full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Raj Kamal, "Internet of Things-Architecture and design principles", McGraw Hill Education.
2. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless Sensor Networks", John Wiley, 2005.

Reference Books:

1. Feng Zhao & Leonidas J. Guibas, "Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
2. Kazem Sohraby, Daniel Minoli, & Taieb Znati, "Wireless Sensor Networks- Technology, Protocols and Applications", John Wiley, 2007.
3. Anna Hac, "Wireless Sensor Network Designs", John Wiley, 2003.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination 2018 – 19
Outcome Based Education(OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2018 – 19)

VII SEMESTER

Sl. No	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P					
1	PCC	18EC71	Computer Networks		3	--	--	03	40	60	100	3
2	PCC	18EC72	VLSI Design		3	--	--	03	40	60	100	3
3	PEC	18XX73X	Professional Elective - 2		3	--	--	03	40	60	100	3
4	PEC	18XX74X	Professional Elective - 3		3	--	--	03	40	60	100	3
5	OEC	18XX75X	Open Elective -B		3	--	--	03	40	60	100	3
6	PCC	18ECL76	Computer Networks Lab		--	2	2	03	40	60	100	2
7	PCC	18ECL77	VLSI Laboratory		--	2	2	03	40	60	100	2
8	Project	18ECP78	Project Work Phase - 1		--	--	2	--	100	--	100	1
9	Internship	--	Internship	(If not completed during the vacation of VI and VII semesters, it shall be carried out during the vacation of VII and VIII semesters)								
				TOTAL	15	4	6	21	380	420	800	20

Note: PCC: Professional core, PEC: Professional Elective.

Professional Elective - 2

Course code under 18XX73X	Course Title
18EC731	Real Time System
18EC732	Satellite Communication
18EC733	Digital Image Processing
18EC734	Data Structures using C++
18EC735	DSP Algorithms & Architecture

Professional Electives - 3

Course code under 18XX74X	Course Title
18EC741	IOT & Wireless Sensor Networks
18EC742	Automotive Electronics
18EC743	Multimedia Communication
18EC744	Cryptography
18EC745	Machine Learning

Open Elective –B

(i) 18EC751 Communication Theory (ii) 18EC752 Neural Networks

Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please refer to the list of open electives under 18XX75X).

Selection of an open elective shall not be allowed if,

- The candidate has studied the same course during the previous semesters of the programme.
- The syllabus content of open elective is similar to that of the Departmental core courses or professional electives.
- A similar course, under any category, is prescribed in the higher semesters of the programme.

Registration to electives shall be documented under the guidance of Programme Coordinator/ Advisor/Mentor.

Project work:

Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary project can be assigned to an individual student or to a group having not more than 4 students. In extraordinary cases, like the funded projects requiring students from different disciplines, the project student strength can be 5 or 6.

CIE procedure for Project Work Phase - 1:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work phase -1, shall be based on the evaluation of the project work phase -1 Report (covering Literature Survey, Problem identification, Objectives and Methodology), project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the Project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable.

The CIE marks awarded for the project work phase -1, shall be based on the evaluation of project work phase -1 Report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

Internship: All the students admitted to III year of BE/B.Tech shall have to undergo mandatory internship of 4 weeks during the vacation of VI and VII semesters and /or VII and VIII semesters. A University examination shall be conducted during VIII semester and the prescribed credit shall be included in VIII semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

H.O.D.
Dept. Of Electronics & Communication
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

SEMESTER – VIII

WIRELESS and CELLULAR COMMUNICATION

Course Code	: 18EC81	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs / Module)	Exam Hours	: 03
	CREDITS – 03		

Course Learning Objectives: This course will enable students to:

- Understand the concepts of propagation over wireless channels from a physics standpoint
- Application of Communication theory both Physical and networking to understand GSM systems that handle mobile telephony
- Application of Communication theory both Physical and networking to understand CDMA systems that handle mobile telephony.
- Application of Communication theory both Physical and networking to understand LTE-4G systems.

Module-1

Mobile Radio Propagation –
Large Scale Path Loss - Free Space Propagation Model, Relating Power to Electric Field, Three Basic Propagation Mechanisms – Reflection (Ground Reflection) , Diffraction, Scattering, Practical Link Budget,
(Text 1 - 2.2 and Ref1 - Chapter 4)
Fading and Multipath – Broadband wireless channel, Delay Spread and Coherence Bandwidth, Doppler Spread and Coherence Time, Angular spread and Coherence Distance **(Text 1 – 2.4)**
Statistical Channel Model of a Broadband Fading Channel
(Text 1 – 2.5.1)
The Cellular Concept – Cellular Concept , Analysis of Cellular Systems, Sectoring
(Text 1- 2.3) **L1, L2**

Module-2

GSM and TDMA Technology
GSM System overview – Introduction, GSM Network and System Architecture, GSM Channel Concept.

GSM System Operations – GSM Identities, System Operations –Traffic cases, GSM Infrastructure Communications (Um Interface)
(Text 2, Part1 and Part 2 of Chapter 5) **L1,L2,L3**

Module-3

CDMA Technology
CDMA System Overview – Introduction, CDMA Network and System Architecture
CDMA Basics – CDMA Channel Concepts, CDMA System (Layer 3) operations, 3G CDMA
(Text 2-Part 1, Part2 and Part 3 of Chapter 6) **L1,L2,L3**

Module-4

LTE – 4G
Key Enablers for LTE 4G – OFDM, SC-FDE, SC-FDMA, Channel Dependant Multiuser Resource Scheduling, Multi-Antenna Techniques, Flat IP Architecture, LTE Network Architecture. **(Text 1, Sec 1.4)**
Multi-Carrier Modulation – Multicarrier concepts, OFDM Basics, OFDM in LTE, Timing and Frequency Synchronization, Peak to Average Ration, SC-Frequency Domain Equalization, Computational Complexity Advantage of OFDM and SC-FDE.
(Text 1, Sec 3.1 – 3.7) **L1,L2,L3**

Module-5

LTE - 4G
OFDMA and SC-FDMA – Multiple Access for OFDM Systems, OFDMA, SCFDMA, Multiuser Diversity and Opportunistic Scheduling, OFDMA and SC-FDMA in LTE, OFDMA system Design Considerations.
(Text 1, Sec 4.1 – 4.6)
The LTE Standard – Introduction to LTE and Hierarchical Channel Structure of LTE, Downlink OFDMA Radio Resources, Uplink SC-FDMA Radio Resources.
(Text 1, Sec 6.1 – 6.4) **L1, L2,L3**

Course Outcomes: After studying this course, students will be able to:

1. Understand the Communication theory both Physical and networking associated with GSM, CDMA & LTE 4G systems.
2. Explain concepts of propagation mechanisms like Reflection, Diffraction, Scattering in wireless channels.
3. Develop a scheme for idle mode, call set up, call progress handling and call tear down in a GSM cellular network.

4. Develop a scheme for idle mode, call set up, call progress handling and call tear down in a CDMA cellular network.
5. Understand the Basic operations of Air interface in a LTE 4G system.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "Fundamentals of LTE" Arunabha Ghosh, Jan Zhang, Jefferey Andrews, Riaz Mohammed, Pearson education (Formerly Prentice Hall, Communications Engg and Emerging Technologies), ISBN-13: 978-0-13-703311-9.
2. "Introduction to Wireless Telecommunications Systems and Networks", Gary Mullet, First Edition, Cengage Learning India Pvt Ltd., 2006, ISBN - 13: 978-81-315-0559-5.

Reference Books:

1. "Wireless Communications: Principles and Practice" Theodore Rappaport, 2nd Edition, Prentice Hall Communications Engineering and Emerging Technologies Series, 2002, ISBN 0-13-042232-0.
2. LTE for UMTS Evolution to LTE-Advanced' Harri Holma and Antti Toskala, Second Edition - 2011, John Wiley & Sons, Ltd. Print ISBN: 9780470660003. 2

NETWORK SECURITY

Course Code	: 18EC821	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Describe network security services and mechanisms.
- Understand Transport Level Security and Secure Socket Layer
- Know about Security concerns in Internet Protocol security
- Discuss about Intruders, Intrusion detection and Malicious Software
- Discuss about Firewalls, Firewall characteristics, Biasing and Configuration

Module-1

Attacks on Computers and Computer Security: Need for Security, Security Approaches, Principles of Security Types of Attacks.
(Chapter1-Text2) **L1, L2**

Module-2

Transport Level Security: Web Security Considerations, Secure Sockets Layer, Transport Layer Security, HTTPS, Secure Shell (SSH)
(Chapter15- Text1) **L1,L2**

Module-3

IP Security: Overview of IP Security (IPSec),IP Security Architecture, Modes of Operation, Security Associations (SA), Authentication Header (AH), Encapsulating Security Payload (ESP), Internet Key Exchange.
(Chapter19-Text1) **L1,L2**

Module-4

Intruders, Intrusion Detection.**(Chapter20-Text1)**
MALICIOUS SOFTWARE: Viruses and Related Threats, Virus Counter measures,
(Chapter21-Text1) **L1,L2**

Module-5

Firewalls: The Need for firewalls, Firewall Characteristics, Types of Firewalls, Firewall Biasing, Firewall location and configuration
(Chapter22-Text 1) **L1, L2**

Course Outcomes: After studying this course, students will be able to:

1. Explain network security services and mechanisms and explain security concepts
2. Understand the concept of Transport Level Security and Secure Socket Layer.
3. Explain Security concerns in Internet Protocol security
4. Explain Intruders, Intrusion detection and Malicious Software
5. Describe Firewalls, Firewall Characteristics, Biasing and Configuration

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOKS:

1. Cryptography and Network Security Principles and Practice , Pearson Education Inc., William Stallings, 5th Edition, 2014, ISBN: 978-81-317- 6166-3.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

REFERENCE BOOKS:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination 2018 – 19
Outcome Based Education(OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2018 – 19)

VIII SEMESTER

Sl. No	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P					
1	PCC	18EC81	Wireless and Cellular Communication		3	--	--	03	40	60	100	3
2	PEC	18XX82X	Professional Elective - 4		3	--	--	03	40	60	100	3
3	Project	18ECP83	Project Work Phase - 2		--	--	2	03	40	60	100	8
4	Seminar	18ECS84	Technical Seminar		--	--	2	03	100	--	100	1
5	Internship	18ECI85	Internship	Completed during the vacation/s of VI and VII semesters and /or VII and VIII semesters.)				03	40	60	100	3
				TOTAL	06	--	4	15	260	240	500	18

Note: PCC: Professional Core, PEC: Professional Elective

Professional Electives - 4

Course code under 18XX82X	Course Title
18EC821	Network Security
18EC822	Micro Electro Mechanical Systems
18EC823	Radar Engineering
18EC824	Optical Communication Networks
18EC825	Biomedical Signal Processing

Project Work

CIE procedure for Project Work Phase - 2:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work phase -2, shall be based on the evaluation of project work phase -2 Report, project presentation skill and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable.

The CIE marks awarded for the project work phase -2, shall be based on the evaluation of project work phase -2 Report, project presentation skill and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

SEE for Project Work Phase - 2:

(i) Single discipline: Contribution to the project and the performance of each group member shall be assessed individually in semester end examination (SEE) conducted at the department.

(ii) Interdisciplinary: Contribution to the project and the performance of each group member shall be assessed individually in semester end examination (SEE) conducted separately at the departments to which the student/s belong to.

Internship: Those, who have not pursued /completed the internship shall be declared as fail and have to complete during subsequent University examination after satisfying the internship requirements.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card. Activity points of the students who have earned the prescribed AICTE activity Points shall be sent the University along with the CIE marks of 8th semester. In case of students who have not satisfied the AICTE activity Points at the end of eighth semester, the column under activity Points shall be marked NSAP (Not Satisfied Activity Points).

H. O. D.
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