ADVANCED COMPUTER ARCHITECTURES (Effective from the academic year 2018 -2019) SEMESTER – VIII			
Course Code	**18CS733**	**CIE Marks**	40
Number of Contact Hours/Week	3:0:0	**SEE Marks**	60
Total Number of Contact Hours	40	**Exam Hours**	03
CREDITS –3			

Course Learning Objectives: This course (18CS733) will enable students to:

- Describe computer architecture.
- Measure the performance of architectures in terms of right parameters.
- Summarize parallel architecture and the software used for them

Module 1	**Contact Hours**
Theory of Parallelism: Parallel Computer Models, The State of Computing, Multiprocessors and Multicomputer, Multivector and SIMD Computers, PRAM and VLSI Models, Program and Network Properties, Conditions of Parallelism, Program Partitioning and Scheduling, Program Flow Mechanisms, System Interconnect Architectures, Principles of Scalable Performance, Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws. For all Algorithm or mechanism any one example is sufficient. **Chapter 1 (1.1to 1.4), Chapter 2(2.1 to 2.4) Chapter 3 (3.1 to 3.3)** **RBT: L1, L2**	08
Module 2	
Hardware Technologies 1: Processors and Memory Hierarchy, Advanced Processor Technology, Superscalar and Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology. For all Algorithms or mechanisms any one example is sufficient. **Chapter 4 (4.1 to 4.4)** **RBT: L1, L2, L3**	08
Module 3	
Hardware Technologies 2: Bus Systems, Cache Memory Organizations, Shared Memory Organizations, Sequential and Weak Consistency Models, Pipelining and Superscalar Techniques, Linear Pipeline Processors, Nonlinear Pipeline Processors. For all Algorithms or mechanisms any one example is sufficient. **Chapter 5 (5.1 to 5.4) Chapter 6 (6.1 to 6.2)** **RBT: L1, L2, L3**	08
Module 4	
Parallel and Scalable Architectures: Multiprocessors and Multicomputers, Multiprocessor System Interconnects, Cache Coherence and Synchronization Mechanisms, Message-Passing Mechanisms, Multivector and SIMD Computers, Vector Processing Principles, Multivector Multiprocessors, Compound Vector Processing, Scalable, Multithreaded, and Dataflow Architectures, Latency-Hiding Techniques, Principles of Multithreading, Fine-Grain Multicomputers. For all Algorithms or mechanisms any one example is sufficient. **Chapter 7 (7.1,7.2 and 7.4) Chapter 8(8.1 to 8.3) Chapter 9(9.1 to 9.3)** **RBT: L1, L2, L3**	08
Module 5	
Software for parallel programming: Parallel Models, Languages, and Compilers ,Parallel Programming Models, Parallel Languages and Compilers, Dependence Analysis of Data Arrays. Instruction and System Level Parallelism, Instruction Level Parallelism, Computer Architecture, Contents, Basic Design Issues, Problem Definition, Model of a Typical	08

Processor, Compiler-detected Instruction Level Parallelism ,Operand Forwarding ,Reorder Buffer, Register Renaming ,Tomasulo's Algorithm. For all Algorithms or mechanisms any one example is sufficient. **Chapter 10(10.1 to 10.3) Chapter 12(12.1 to 12.9)** **RBT: L1, L2, L3**	
Course Outcomes: The student will be able to : • Explain the concepts of parallel computing and hardware technologies • Compare and contrast the parallel architectures • Illustrate parallel programming concepts	
Question Paper Pattern: • The question paper will have ten questions. • Each full Question consisting of 20 marks • There will be 2 full questions (with a maximum of four sub questions) from each module. • Each full question will have sub questions covering all the topics under a module. • The students will have to answer 5 full questions, selecting one full question from each module.	
Textbooks: 1. Kai Hwang and Naresh Jotwani, Advanced Computer Architecture (SIE): Parallelism, Scalability, Programmability, McGraw Hill Education 3/e. 2015	
Reference Books: 1. John L. Hennessy and David A. Patterson, Computer Architecture: A quantitative approach, 5th edition, Morgan Kaufmann Elseveir, 2013	

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