



AIET

DEPT. OF ELECTRONICS
AND COMMUNICATION
ENGINEERING

COURSE OBJECTIVE

This course aims to providing detailed knowledge in VLSI design process starting from digital design , hardware descriptive languages, RTL synthesis and simulation verification FPGA programming implementation. In this process the student will understand the entire logic design process the student will understand the entire logic design process and will be able to take on the challenges posed by the even demanding chip design industry

CADENCE TOOL

Real time Hands on training Simulation.. incisie synthesis... Genus Digital System Implementation...Innovus and its library Projects on digital MOSFET dimensions hands on training on VIRTUOSO tool basic schematic for different designs creation of symbols for different designs test bench

ANALOG DESIGN

Different types of VLSI tools- Micro wind,Electric tool Synopsys, Icarus tool Mentor Graphics, Magic tool DSCH for schematic

OUTCOMES

After the end of the course the student will be able to complete significant VLSI design project having a set of objective criteria and design constraints. Expected Job Roles :VLSI

Training program on Analog and Digital VLSI

29 JUNE 2023 TO 2 JULY 2023

RESOURCE PERSON

Dr. Srinivasar Rao Udara
(B.Tech, M.Tech, MISTE ,P.H.D)
Distinguished Scientist
Awardee Managing Director
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