VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E. in Electronics and Communication Engineering (ECE)

Scheme of Teaching and Examinations 2021

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 - 22)

III SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21MAT31	Mathematics Course (Common to all)	TD- Maths PSB-Maths					03	50	50	100	3
2	IPCC 21EC32	Digital System Design using Verilog	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4
3	IPCC 21EC33	Basic Signal Processing	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4
4	PCC 21EC34	Analog Electronic Circuits	TD: ECE PSB: ECE	3	0	0	1	03	50	50	100	3
5	PCC 21ECL35	Analog and Digital Electronics Lab	TD: ECE PSB: ECE	0	0	2		03	50	50	100	1
6	UHV 21UH36	Social Connect and Responsibility	Any Department	0	0	1		01	50	50	100	1
7	HSMC 21KSK37/47	Samskrutika Kannada	TD and PSB HSMC	1	0	0		01	50	50	100	1
	HSMC 21KBK37/47	Balake Kannada										
		OR										
	HSMC 21CIP37/47	Constitution of India and Professional Ethics										
8	AEC 21EC38X	Ability Enhancement Course - III	TD: Concerned department PSB: Concerned Board	If offered as Theory Course: 1	0	0		01	50	50	100	1
				If offered as lab. course: 0	0	2		02				
								Total	**400**	**400**	**800**	**18**
9	Scheduled activities for III to VIII semesters	NMDC 21NS83	National Service Scheme (NSS)	NSS	All students have to register for any one of the course namely National Service Scheme, Physical Education (PE)(Sports and Athletics) and Yoga with the concerned coordinator of the course during the first week of III semester. The activities shall be carried out between III semester to VIII semester (for 5 semesters). SEE in the above courses shall be conducted during VIII semester examinations and the accumulated CIE marks shall be added to the SEE marks. Successful completion of the registered course is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE and Yoga activities.								
		NMDC 21PE83	Physical Education (PE)(Sports and Athletics)	PE								
		NMDC 21YO83	Yoga	Yoga								

Course prescribed to lateral entry Diploma holders admitted to III semester B.E./B.Tech programs

1	NCMC 21MATDIP31	Additional Mathematics - I	Maths	02	02	--	--	---	100	----	100	0

Note: BSC: Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course.
L –Lecture, **T** – Tutorial, P- Practical/ Drawing, **S** – Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination.**TD**-Teaching Department, **PSB**: Paper Setting department

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and **21KBK37/47** Balake Kannada is for non-Kannada speaking, reading, and writing students.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2021-22 may be referred.

21INT49Inter/Intra Institutional Internship: All the students admitted to engineering programs under the lateral entry category shall have to undergo a mandatory 21INT49 Inter/Intra Institutional Internship of 03 weeks during the intervening period of III and IV semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the IV semester grade card. The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequently after satisfying the internship requirements. The faculty coordinator or mentor shall monitor the students' internship progress and interact with them for the successful completion of the internship.

Non–credit mandatory courses (NCMC):

(A) Additional Mathematics I and II:

(1) These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/ to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

(B) National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses sh be mandatory for the award of degree.

Ability Enhancement Course - III			
21EC381	LD (Logic Design) Lab using Pspice / MultiSIM	21EC383	LIC (Linear Integrated Circuits) Lab using Pspice / MultiSIM
21EC382	AEC (Analog Electronic Circuits) Lab	21EC384	LabVIEW Programming Basics

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Scheme of Teaching and Examinations 2021

Outcome-Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 - 22)

IV SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21EC41	Maths for Communication Engineers	TD, PSB-Maths					03	50	50	100	3
2	IPCC 21EC42	Digital Signal Processing	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4
3	IPCC 21EC43	Circuits & Controls	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4
4	PCC 21EC44	Communication Theory	TD: ECE PSB: ECE	3	0	0	1	03	50	50	100	3
5	AEC 21BE45	Biology For Engineers	BT, CHE, PHY	2	0	0		02	50	50	100	2
6	PCC 21ECL46	Communication Laboratory I	TD: ECE PSB: ECE	0	0	2		03	50	50	100	1
7	HSMC 21KSK37/47	Samskrutika Kannada	HSMC	1	0	0		01	50	50	100	1
	HSMC 21KBK37/47	Balake Kannada										
		OR										
	HSMC 21CIP37/47	Constitution of India & Professional Ethics										
8	AEC 21EC48X	Ability Enhancement Course- IV	TD and PSB: Concerned department	If offered as theory Course: 1 0 0				01	50	50	100	1
				If offered as lab. course: 0 0 2				02				
9	UHV 21UH49	Universal Human Values	Any Department	1	0	0		01	50	50	100	
10	INT 21INT49	Inter/Intra Institutional Internship	Evaluation By the appropriate authorities	Completed during the intervening period ofII and III semesters by students admitted to first year of BE./B.Tech and during the intervening period of III and IV semesters by Lateral entry students admitted to III semester.				3	100	--	100	2
								Total	**550**	**450**	**1000**	**22**

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

1	NCMC 21MATDIP41	Additional Mathematics - II	Maths	02	02	--	--	--	100	--	100	0

Note: BSC: Basic Science Course, IPCC: Integrated Professional Core Course, PCC: Professional Core Course, AEC –Ability Enhancement Courses, HSMC: Humanity and Social Science and Management Courses, UHV- Universal Human Value Courses.

L –Lecture, T – Tutorial, P- Practical/ Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

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Non – credit mandatory course (NCMC):

Additional Mathematics - II:

(1) Lateral entry Diploma holders admitted to III semester of B.E./B.Tech., shall attend the classes during the IV semester to complete all the

formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfil the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the course Additional Mathematics II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics II shall be indicated as Unsatisfactory.

Ability Enhancement Course - IV

21EC481	Embedded C Basics	21EC483	Octave / Scilab for Signals
21EC482	C++ Basics	21EC484	DAQ using LabVIEW

Internship of 04 weeks during the intervening period of IV and V semesters; 21INT68Innovation/ Entrepreneurship/ Societal based Internship.

(1) All the students shall have to undergo a mandatory internship of 04 weeks during the intervening period of IV and V semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the VI semester grade card.The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be considered under F (fail) grade and shall have to complete during subsequently after satisfying the internship requirements.

(2) Innovation/ Entrepreneurship Internship shall be carried out at industry, State and Central Government /Non-government organizations (NGOs micro, small and medium enterprise (MSME), Innovation centres or Incubation centres. Innovation need not be a single major breakthrough; it can also be a series of small or incremental changes. Innovation of any kind can also happen outside of the business world.

Entrepreneurship internships offers a chance to gain hands on experience in the world of entrepreneurship and helps to learn what it takes to run a small entrepreneurial business by performing intern duties with an established company. This experience can then be applied to future business endeavours. Start-ups and small companies are a preferred place to learn the business tack ticks for future entrepreneurs as learning how a small business operates will serve the intern well when he/she manages his/her own company. Entrepreneurship acts as a catalyst to open the minds to creativity and innovation. Entrepreneurship internship can be from several sectors, including technology, small and medium-sized, and the service sector.

(3) Societal or social internship.

Urbanization is increasing on a global scale; and yet, half the world's population still resides in rural areas and is devoid of many things that urban population enjoy. Rural internship is a work-based activity in which students will have a chance to solve/reduce the problems of the rural place for better living.

As proposed under the AICTE rural internship programme, activities under Societal or social internship, particularly in rural areas, shall be considered for 40 points under AICTE activity point programme.

B. E.(Common to all branches)

Choice Based Credit System (CBCS) and Outcome-Based Education (OBE)

SEMESTER - III

TRANSFORM CALCULUS, FOURIER SERIES AND NUMERICAL TECHNIQUES			
Course Code	**21MAT 31**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:2:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course objectives: The goal of the course Transform Calculus, Fourier series and Numerical techniques 21MAT 31 is

- To have an insight into solving ordinary differential equations by using Laplace transform techniques
- Learn to use the Fourier series to represent periodical physical phenomena in engineering analysis.
- To enable the students to study Fourier Transforms and concepts of infinite Fourier Sine and Cosine transforms and to learn the method of solving difference equations by the z-transform method.
- To develop proficiency in solving ordinary and partial differential equations arising in engineering applications, using numerical methods

Module-1: Laplace Transform

Definition and Laplace transforms of elementary functions (statements only). Problems on Laplace'sTransform of $e^{at}f(t)$, $t^n f(t)$, $\frac{f(t)}{t}$. Laplace transforms of Periodic functions (statement only) and unit-step function – problems.

Inverse Laplace transforms definition and problems, Convolution theorem to find the inverse Laplace transforms (without Proof) problems.Laplace transforms of derivatives, solution ofdifferential equations.**(8 Hours)**

Self-study: Solution of simultaneous first-order differential equations.

(RBT Levels: L1, L2 and L3)

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-2: Fourier Series

Introduction toinfinite series, convergence and divergence. Periodic functions, Dirichlet's condition. Fourier series of periodic functions with period 2π and arbitrary period. Half range Fourier series. Practical harmonic analysis.**(8 Hours)**

Self-study: Convergence of series by D'Alembert's Ratio test and, Cauchy'sroot test.

(RBT Levels: L1, L2 and L3)

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-3: Infinite Fourier Transforms and Z-Transforms

Infinite Fourier transforms definition, Fourier sine and cosine transforms. Inverse Fourier transforms, Inverse Fourier cosine and sine transforms. Problems.

Difference equations, z-transform-definition, Standard z-transforms, Damping and shifting rules, Problems. Inverse z-transform and applications to solve difference equations.**(8 Hours)**

Self Study: Initial value and final value theorems, problems.

(RBT Levels: L1, L2 and L3)

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-4: Numerical Solution of Partial Differential Equations	
Classifications of second-order partial differential equations, finite difference approximations to derivatives, Solution of Laplace's equationusing standard five-point formula. Solution of heat equation by Schmidt explicit formula and Crank- Nicholson method, Solution of the Wave equation. Problems. **(8 Hours)** **Self Study**: Solution of Poisson equations using standard five-point formula. **(RBT Levels: L1, L2 and L3)**	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation
Module-5: Numerical Solution of Second-Order ODEs and Calculus of Variations	
Second-order differential equations - Runge-Kutta method and Milne's predictor and corrector method. (No derivations of formulae). Calculus of Variations:Functionals, Euler's equation, Problems on extremals of functional. Geodesics on a plane,Variationalproblems.**(8 Hours)** **Self Study:** Hanging chain problem **(RBT Levels: L1, L2 and L3)**	
Course outcomes: After successfully completing the course, the students will beable : ➢ To solve ordinary differential equations using Laplace transform. ➢ Demonstrate the Fourier series to study the behaviour of periodic functions and their applications in system communications, digital signal processing and field theory. ➢ To use Fourier transforms to analyze problems involving continuous-time signals and to apply Z-Transform techniques to solve difference equations ➢ To solve mathematical models represented by initial or boundary value problems involving partial differential equations ➢ Determine the extremals of functionals using calculus of variations and solve problems arising in dynamics of rigid bodies and vibrational analysis.	

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks (duration 01 hour)**
2. First test at the end of 5th week of the semester
3. Second test at the end of the 10th week of the semester
4. Third test at the end of the 15th week of the semester

Two assignments each of 10 Marks

5. First assignment at the end of 4th week of the semester
6. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

7. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

- The question paper will be set for 100 marks and marks scored will be proportionally scaled down to 50 marks
- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books:

1. **B.S.Grewal**:"HigherEngineeringMathematics",Khannapublishers,44th Ed.2018
2. **E.Kreyszig**:"AdvancedEngineeringMathematics",JohnWiley&Sons,10th Ed.(Reprint),2016.

Reference Books

1. **V.Ramana:**"HigherEngineeringMathematics"McGraw-HillEducation,11th Ed.
2. **SrimantaPal&SubodhC.Bhunia:**"EngineeringMathematics"OxfordUniversityPress,3rd Reprint, 2016.
3. **N.P Bali and Manish Goyal**: "A textbook of Engineering Mathematics" Laxmi Publications, Latest edition.
4. **C. Ray Wylie, Louis C. Barrett:** "Advanced Engineering Mathematics" McGraw – Hill Book Co.Newyork, Latested.
5. **Gupta C.B, Sing S.R and Mukesh Kumar:** "Engineering Mathematic for Semester I and II", Mc-Graw Hill Education(India) Pvt. Ltd2015.
6. **H.K.DassandEr.RajnishVerma:**"HigherEngineeringMathematics"S.ChandPublication(2014).
7. **JamesStewart:**"Calculus"Cengagepublications,7th edition,4th Reprint2019.

Web links and Video Lectures (e-Resources):

- http://.ac.in/courses.php?disciplineID=111
- http://www.class-central.com/subject/math(MOOCs)
- http://academicearth.org/
- http://www.bookstreet.in.
- VTU e-ShikshanaProgram
- VTU EDUSATProgram

Activity-Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quizzes
- Assignments
- Seminars

Siddesh

H. O. D.
Dept. Of Electronics & Communication
Alva's Institute of Technology
Mijar, MOODBIDRI - 574 225

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NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

III Semester

Digital System Design Using Verilog			
Course Code	21EC32	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 13 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

1. To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques.
2. To impart the concepts of designing and analyzing combinational logic circuits.
3. To impart design methods and analysis of sequential logic circuits.
4. To impart the concepts of Verilog HDL-data flow and behavioral models for the design of digital systems.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class .
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
- Give Programming Assignments.

Module-1

Principles of Combinational Logic: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps- up to 4 variables, Quine-McCluskey Minimization Technique. Quine-McCluskey using Don't Care Terms. (Section 3.1 to 3.5 of Text 1).

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-2

Logic Design with MSI Components and Programmable Logic Devices: Binary Adders and Subtractors, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices (PLDs) (Section 5.1 to 5.7 of Text 2)

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-3	
Flip-Flops and its Applications: The Master-Slave Flip-flops (Pulse-Triggered flip-flops): SR flip-flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, JK, D and SR flip-flops. (Section 6.4, 6.6 to 6.9 (Excluding 6.9.3) of Text 2)	
Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3
Module-4	
Introduction to Verilog: Structure of Verilog module, Operators, Data Types, Styles of Description. (Section 1.1 to 1.6.2, 1.6.4 (only Verilog), 2 of Text 3) **Verilog Data flow description:** Highlights of Data flow description, Structure of Data flow description. (Section 2.1 to 2.2 (only Verilog) of Text 3)	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3
Module-5	
Verilog Behavioral description: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers (2:1, 4:1, 8:1). (Section 3.1 to 3.4 (only Verilog) of Text 3) **Verilog Structural description:** Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder. (Section 4.1 to 4.2 of Text 3)	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Using suitable simulation software, demonstrate the operation of the following circuits:

Sl.No	Experiments
1	To simplify the given Boolean expressions and realize using Verilog program.
2	To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description.
3	To realize 4-bit ALU using Verilog program.
4	To realize the following Code converters using Verilog Behavioral description a) Gray to binary and vice versa b) Binary to excess3 and vice versa
5	To realize using Verilog Behavioral description: 8:1 mux, 8:3 encoder, Priority encoder
6	To realize using Verilog Behavioral description: 1:8 Demux, 3:8 decoder, 2-bit Comparator
7	To realize using Verilog Behavioral description: Flip-flops: a) JK type b) SR type c) T type and d) D type
8	To realize Counters - up/down (BCD and binary) using Verilog Behavioral description.
	Demonstration Experiments (For CIE only – not to be included for SEE)
	Use FPGA/CPLD kits for downloading Verilog codes and check the output for interfacing experiments.
9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
10	Verilog programs to interface a Relay or ADC to the FPGA/CPLD and demonstrate its working.
11	Verilog programs to interface DAC to the FPGA/CPLD for Waveform generation.
12	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

Course Outcomes

At the end of the course the student will be able to:

1. Simplify Boolean functions using K-map and Quine-McCluskey minimization technique.
2. Analyze and design for combinational logic circuits.
3. Analyze the concepts of Flip Flops (SR, D, T and JK) and to design the synchronous sequential circuits using Flip Flops.
4. Model Combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Second assignment at the end of 9th week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured out of 100 will be scaled down to 50 marks.

Suggested Learning Resources:

Text Books

1. Digital Logic Applications and Design by John M Yarbrough, Thomson Learning, 2001.
2. Digital Principles and Design by Donald D Givone, McGraw Hill, 2002.
3. HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dreamtech press.

Reference Books:

1. Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning
2. Logic Design, by Sudhakar Samuel, Pearson/ Sanguine, 2007
3. Fundamentals of HDL, by Cyril P R, Pearson/Sanguine 2010

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills.

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VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

III Semester

Basic Signal Processing			
Course Code	21EC33	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 13 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

Preparation: To prepare students with fundamental knowledge/ overview in the field of Signal Processing with Familiarization with the concept of Vector spaces and orthogonality with a qualitative insight into applications in communications.

Core Competence: To equip students with a basic foundation of Signal Processing by delivering the basics of quantitative parameters for Matrices & Linear Transformations, the mathematical description of discrete time signals and systems, analyzing the signals in time domain using convolution sum, classifying signals into different categories based on their properties, analyzing Linear Time Invariant (LTI) systems in time and transform domains

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
- Give Programming Assignments.

Module-1

Vector Spaces: Vector spaces and Null subspaces, Rank and Row reduced form, Independence, Basis and dimension, Dimensions of the four subspaces, Rank-Nullity Theorem, Linear Transformations Orthogonality: Orthogonal Vectors and Subspaces, Projections and Least squares, Orthogonal Bases and Gram-Schmidt Orthogonalization procedure

(Refer Chapters 2 and 3 of Text 1)

Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Module-2	
Eigen values and Eigen vectors: Review of Eigen values and Diagonalization of a Matrix, Special Matrices (Positive Definite, Symmetric) and their properties, Singular Value Decomposition. **(Refer Chapter 5, Text 1)**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Module-3	
Introduction and Classification of signals: Definition of signal and systems with examples, Elementary signals/Functions: Exponential, sinusoidal, step, impulse and ramp functions **Basic Operations on signals:** Amplitude scaling, addition, multiplication, time scaling, time shift and time reversal. Expression of triangular, rectangular and other waveforms in terms of elementary signals **System Classification and properties:** Linear-nonlinear, Time variant -invariant, causal-noncausal, static-dynamic, stable-unstable, invertible. **(Text 2) [Only for Discrete Signals & Systems]**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Module-4	
Time domain representation of LTI System: Impulse response, convolution sum. Computation of convolution sum using graphical method for unit step and unit step, unit step and exponential, exponential and exponential, unit step and rectangular, and rectangular and rectangular. **LTI system Properties in terms of impulse response:** System interconnection, Memory less, Causal, Stable, Invertible and Deconvolution and step response **(Text 2) [Only for Discrete Signals & Systems]**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Module-5	
The Z-Transforms: Z transform, properties of the region of convergence, properties of the Z-transform, Inverse Z-transform by partial fraction, Causality and stability, Transform analysis of LTI systems. **(Text 2)**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC	
Sl.No	**Experiments**
1	a. Program to create and modify a vector (array). b. Program to create and modify a matrix.
2	Programs on basic operations on matrix.
3	Program to solve system of linear equations.
4	Program for Gram-Schmidt orthogonalization.
5	Program to find Eigen value and Eigen vector.
6	Program to find Singular value decomposition.

7	Program to generate discrete waveforms.
8	Program to perform basic operation on signals.
9	Program to perform convolution of two given sequences.
10	a. Program to perform verification of commutative property of convolution. b. Program to perform verification of distributive property of convolution. c. Program to perform verification of associative property of convolution.
11	Program to compute step response from the given impulse response.
12	Programs to find Z-transform and inverse Z-transform of a sequence.

Course outcomes (Course Skill Set)

At the end of the course the student will be able to :

1. Understand the basics of Linear Algebra
2. Analyse different types of signals and systems
3. Analyse the properties of discrete-time signals & systems
4. Analyse discrete time signals & systems using Z transforms

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Programming assignment at the end of 9th week of the semester, which can be implemented using programming languages like C++/Python/Java/Scilab

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured out of 100 will be scaled down to 50 marks.

Suggested Learning Resources:

Text Books

1. Gilbert Strang, "Linear Algebra and its Applications", Cengage Learning, 4th Edition, 2006, ISBN 97809802327
2. Simon Haykin and Barry Van Veen, "Signals and Systems", 2nd Edition, 2008, Wiley India. ISBN9971-51-239-4.

Reference Books:

1. **Michael Roberts,** "Fundamentals of Signals & Systems",2nd edition, Tata McGraw-Hill, 2010, ISBN978-0-07-070221-9.
2. **Alan V Oppenheim, Alan S Willsky and S Hamid Nawab,** "Signals and Systems" Pearson Education Asia / PHI, 2"" edition, 1997. Indian Reprint 2002.
3. **H P Hsu, R Ranjan,** "Signals and Systems", Schaum's outlines, TMH, 2006.
4. **B P Lathi,** "Linear Systems and Signals", Oxford University Press, 2005.
5. **Ganesh Rao and Satish Tunga,** "Signals and Systems", Pearson/Sanguine.
6. **Seymour Lipschutz, Marc Lipson,** "Schaums Easy Outline of Linear Algebra", 2020.

Web links and Video Lectures (e-Resources):

Video lectures on Signals and Systems by Alan V Oppenheim

Lecture 1, Introduction | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube

Lecture 2, Signals and Systems: Part 1 | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube

NPTEL video lectures signals and system:

https://www.youtube.com/watch?v=7Z3LE5uM-6Y&list=PLbMVogVj5nJQQZbah2uRZIRZ_9kfoqZyx

Video lectures on Linear Algebra by Gilbert Strang

https://www.youtube.com/watch?v=ZK3O402wf1c&list=PL49CF3715CB9EF31D&index=1

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

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III Semester

Analog Electronic Circuits			
Course Code	21EC34	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives: This course will enable students to

- Explain various BJT parameters, connections and configurations.
- Design and demonstrate the diode circuits and transistor amplifiers.
- Explain various types of FET biasing and demonstrate the use of FET amplifiers.
- Analyze Power amplifier circuits in different modes of operation.
- Construct Feedback and Oscillator circuits using FET.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

BJT Biasing: Biasing in BJT amplifier circuits: The Classical Discrete circuit bias (Voltage-divider bias), Biasing using a collector to base feedback resistor.

Small signal operation and Models: Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain, Separating the signal and the DC quantities, The hybrid Π model, The T model.

MOSFETs: Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor.

Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model.

[Text 1: 3.5(3.5.1, 3.5.3), 3.6(3.6.1 to 3.6.7), 4.5(4.5.1, 4.5.2, 4.5.3), 4.6(4.6.1 to 4.6.7)]

Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Basic BJT Amplifier Configurations- Design of Common Emitter and Common collector amplifier circuits. **RBT Level:** L1, L2, L3

Module-2

MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance RS, Source follower.

MOSFET internal capacitances and High frequency model: The gate capacitive effect, Junction capacitances, High frequency model.

Frequency response of the CS amplifier: The three frequency bands, high frequency response, Low frequency response.

Oscillators: FET based Phase shift oscillator, LC and Crystal Oscillators (no derivation) [Text 1: 4.7(4.7.1 to 4.7.4, 4.7.6) 4.8(4.8.1, 4.8.2, 4.8.3), 4.9, 12.2.2, 12.3.1, 12,3,2]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Discrete Circuit MOS Amplifier – The common source amplifier and the source follower. **RBT Level:** L1, L2, L3

Module-3

Feedback Amplifier: General feedback structure, Properties of negative feedback, The Four Basic Feedback Topologies, The series-shunt, series-series, shunt-shunt and shunt-series amplifiers (Qualitative Analysis). **Output Stages and Power Amplifiers:** Introduction, Classification of output stages, Class A output stage, Class B output stage: Transfer Characteristics, Power Dissipation, Power Conversion efficiency, Class AB output stage, Class C tuned Amplifier. [Text 1: 7.1, 7.2, 7.3, 7.4.1, 7.5.1, 7.6 (7.6.1 to 7.6.3), 13.1, 13.2, 13.3(13.3.1, 13.3.2, 13.3.3, 13.4, 13.7)]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Class D power amplifier. **RBT Level:** L1, L2, L3

Module-4

Op-Amp Circuits: Op-amp DC and AC Amplifiers, DAC - Weighted resistor and R-2R ladder, ADC-Successive approximation type, Small Signal half wave rectifier, Absolute value output circuit, Active Filters, First and second order low-pass and high-pass Butterworth filters, Band-pass filters, Band reject filters. **555 Timer and its applications:** Monostable and Astable Multivibrators. [Text 2: 6.2, 8.11(8.11.1a, 8.11.1b), 8.11.2a, 8.12.2,8.13 7.2, 7.3, 7.4, 7.5, 7.6, 7.8, 7.9, 9.4.1, 9.4.1(a), 9.4.3, 9.4.3(a)]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Clippers and Clampers, Peak detector, Sample and hold circuit. **RBT Level:** L1, L2, L3

Module-5

Overview of Power Electronic Systems: Power Electronic Systems, Power Electronic Converters and Applications. **Thyristors:** Static Anode-Cathode characteristics and Gate characteristics of SCR, Turn-ON methods, Turn-off Mechanism, Turn-OFF Methods: Natural and Forced Commutation – Class A without design consideration. **Gate Trigger Circuit:** Resistance Firing Circuit, Resistance capacitance firing circuit, Unijunction Transistor: Basic operation and UJT Firing Circuit. [Text 3: 1.3, 1.5,1.6, 2.2,2.3,2.4,2.6, 2.7,2.9, 2.10,3.2,3.5.1, 3.5.2, 3.6.1, 3.6.3,3.6.4]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Basic Construction, working and applications of DIAC, TRIAC, IGBT, GTO. **RBT Level:** L1, L2, L3

Course Outcomes (Course Skill Set)

At the end of the course the student will be able to :

1. Understand the characteristics of BJTs and FETs for switching and amplifier circuits.
2. Design and analyze FET amplifiers and oscillatorswith different circuit configurations and biasing conditions.
3. Understand the feedback topologies and approximations in the design of amplifiers and oscillators.
4. Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.
5. Understand the power electronic device components and its functions for basic power electronic circuits.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.

The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored out of 100 shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6thEdition, Oxford, 2015.ISBN:978-0-19-808913-1
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4thEdition, Pearson Education, 2018. ISBN: 978-93-325-4991-3
3. **MD Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897'**

Web links and Video Lectures (e-Resources):

- Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015.
- Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.

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III Semester

Analog and Digital Electronics Lab			
Course Code	21ECL35	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Understand the electronic circuit schematic and its working
- Realize and test amplifier and oscillator circuits for the given specifications
- Realize the opamp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers.
- Study the static characteristics of SCR and test the RC triggering circuit.
- Design and test the combinational and sequential logic circuits for their functionalities.
- Use the suitable ICs based on the specifications and functions.

Sl.No.	Experiments
1	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.
2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator and iii) RC Phase shift oscillator
3	Design and set up the circuits using opamp: i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator
4	Obtain the static characteristics of SCR and test SCR Controlled HWR and FWR using RC triggering circuit.
5	Design and implement (a) Half Adder & Full Adder using basic gates and NAND gates, (b) Half subtractor & Full subtractor using NAND gates, (c) 4-variable function using IC74151(8:1MUX).
6	Realize (i) Binary to Gray code conversion & vice-versa (IC74139), (ii) BCD to Excess-3 code conversion and vice versa
7	a) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop b) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.
8	Realize a) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop b) Mod-N Counter using IC7490 / 7476 c) Synchronous counter using IC74192

9	Design 4-bit R – 2R Op-Amp Digital to Analog Converter (i) for a 4-bit binary input using toggle switches (ii) by generating digital inputs using mod-16
10	Pseudorandom sequence generator using IC7495
11	Test the precision rectifiers using opamp: i) Half wave rectifier ii) Full wave rectifier
12	Design and test Monostable and Astable Multivibrator using 555 Timer

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Design and analyze the BJT/FET amplifier and oscillator circuits.
2. Design and test Opamp circuits to realize the mathematical computations, DAC and precision rectifiers.
3. Design and test the combinational logic circuits for the given specifications.
4. Test the sequential logic circuits for the given functionality.
5. Demonstrate the basic electronic circuit experiments using SCR and 555 timer.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks.**

The split-up of CIE marks for record/ journal and test are in the ratio **60:40.**

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Fundamentals of Electronic Devices and Circuits Lab Manual, David A Bell, 5th Edition, 2009, Oxford University Press.
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018. ISBN: 978-93-325-4991-3.
3. Fundamentals of Logic Design, Charles H Roth Jr., Larry L Kinney, Cengage Learning, 7th Edition.

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III Semester

LD (Logic Design) Lab using Pspice / MultiSIM			
Course Code	**21EC381**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- Impart the concepts of De Morgan's Theorem, SOP, POS forms.
- Impart the concepts of designing and analyzing combinational logic circuits.
- Impart the concepts of analysis of sequential logic circuits.
- Analyze and design any given synchronous sequential circuits.

Sl.No	Experiments
1	Implementation of De Morgan's theorem and SOP/POS expressions using Pspice/Multisim.
2	Implementation of Half Adder, Full Adder, Half Subtractor and Full Subtractor using Pspice/ Multisim.
3	Design and implementation of 4-bit Parallel Adder/ Subtractor using IC 7483 and BCD to Excess-3 code conversion and vice-versa using Pspice/Multisim.
4	Design and implement of IC 7485 5-bit magnitude comparator using Pspice/Multisim.
5	To Realize Adder & Subtractor using IC 74153 (4:1 MUX) and 4-variable function using IC74151 (8:1MUX) using Pspice/Multisim.
6	To realize Adder and Subtractor using IC 74139/ 74155N (Demux/Decoder) and Binary to Gray code conversion & vice versa using 74139/ 74155N using Pspice/Multisim.
7	SR, Master-Slave JK, D & T flip-flops using NAND Gates using Pspice/Multisim.
8	Design and realize the Synchronous counters (up/down decade/binary) using Pspice/Multisim.
9	Realize the shift registers and their modes (SISO, PISO, PIPO, SIPO) using 7474/7495 using Pspice/Multisim.
10	Design Pseudo Random Sequence generator using 7495 using Pspice/Multisim.
11	Design Serial Adder with Accumulator and simulate using Pspice/Multisim.
12	Design using Pspice/Multisim Mod-N Counters.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Demonstrate the truth table of various expressions and combinational circuits using logic gates.
2. Design various combinational circuits such as adders, subtractors, comparators, multiplexers and code converters.
3. Construct flips-flops, counters and shift registers.
4. Design and implement synchronous counters.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall

be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

- Digital Logic Applications and Design by John M Yarbrough, Thomson Learning, 2001
- Digital Principles and Design by Donald D Givone, McGraw Hill, 2002.

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VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

III Semester

AEC (Analog Electronic Circuits) Lab			
Course Code	21EC382	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	2

Course objectives:

- To provide practical exposure to the students on designing, setting up, executing and debugging various electronic circuits using simulation software.
- To give the knowledge and practical exposure on simple applications of analog electronic circuits.

Sl.No	Experiments using Pspice/MultiSIM software
1	Experiments to realize diode clipping (single, double ended) circuits.
2	Experiments to realize diode clamping (positive, negative) circuits.
3	Experiments to realize Full wave rectifier without filter (and set-up to measure the ripple factor, Vp-p, Vrms, etc.).
4	Design and conduct an experiment on Series Voltage Regulator using Zener diode to determine line/load regulation characteristics.
5	Realize BJT Darlington Emitter follower without bootstrapping and determine the gain, input and output impedances (other configurations of emitter follower can also be considered).
6	Set-up and study the working of complementary symmetry class B push pull power amplifier (other power amplifiers can also be suitably considered) and calculate the efficiency.
7	Design and set-up the oscillator circuits (Hartley, Colpitts, etc. using BJT/FET) and determine the frequency of oscillation.
8	Design and set-up the crystal oscillator and determine the frequency of oscillation.
9	Experiment to realize Input and Output characteristics of BJT Common emitter configuration and evaluation of parameters.
10	Experiments to realize Transfer and drain characteristics of a MOSFET.
11	Experiments to realize UJT triggering circuit for Controlled Full wave Rectifier.
12	Design and simulation of Regulated power supply.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Understand the circuit schematic and its working.
2. Study the characteristics of different electronic devices.
3. Design and test simple electronic circuits as per the specifications using discrete electronic components.
4. Compute the parameters from the characteristics of active devices.
5. Familiarize with EDA software which can be used for electronic circuit simulation.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours.

Rubrics suggested in Annexure-II of Regulation book.

Suggested Learning Resources:

1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual, 5th Edition, 2009, Oxford University Press.
2. Muhammed H Rashid, "Introduction to PSpice using OrCAD for circuits and electronics", 3rd Edition, Prentice Hall, 2003.

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III Semester

LIC (Linear Integrated Circuits) Lab using Pspice / MultiSIM			
Course Code	**21EC383**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- To apply operational amplifiers in linear and nonlinear applications.
- To acquire the basic knowledge of special function ICs.
- To use Multisim/Pspice software for circuit design and simulation

Sl.No	**Experiments using Pspice / MultiSIM** Every experiment has to be designed, circuit to be drawn / constructed and executed in the specified software. Results are also to be noted and inferred.
	Note: Standard design procedure to be adopted.
1	To realize using op-amp an Inverting Amplifier and Non-Inverting Amplifier
2	To realize using op-amps i) Summing Amplifier ii)Difference amplifier
3	To realize using op-amps an Instrumentation Amplifier
4	To realize using op-amps i) Differentiator ii)Integrator
5	To realize using op-amps a Full wave Precision Rectifier
6	To realize using op-amps • Inverting and Non-Inverting Zero Crossing Detectors • Positive and Negative Voltage level detectors
7	To realize using op-amp an Inverting Schmitt Trigger
8	To realize using op-amp an Astable Multivibrator
9	To design and implement using op-amps • Butterworth I & II order Low Pass Filter • Butterworth I & II order High Pass Filter
10	To design and implement using op-amp a RC Phase Shift Oscillator
11	To design and implement Mono-stable Multivibrator using 555 timer
12	To design and implement 4 - bit R-2R Digital to Analog Converter

Course outcomes (Course Skill Set):

After studying this course, students will be able to;

1. Sketch/draw circuit schematics, construct circuits, analyze and troubleshoot circuits containing op-amps, resistors, diodes, capacitors and independent sources.
2. Relate to the manufacturer's data sheets of IC 555 timer and IC μa741 op-amp.
3. Realize and verify the operation of analog integrated circuits like Amplifiers, Precision Rectifiers, Comparators and Waveform generators.
4. Design and implement analog integrated circuits like Oscillators, Active filters, Timer circuits, Data converters and compare the experimental results with theoretical values.

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III Semester

LabVIEW Programming Basics			
Course Code	**21EC384**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- Aware of various front panel controls and indicators.
- Connect and manipulate nodes and wires in the block diagram.
- Locate various toolbars and pull-down menus for the purpose of implementing specific functions.
- Locate and utilize the context help window.
- Familiar with LabVIEW and different applications using it.
- Run a Virtual Instrument (VI).

Sl.No	**VI Programs (using LabVIEW software) to realize the following:**
1	Basic arithmetic operations: addition, subtraction, multiplication and division
2	Boolean operations: AND, OR, XOR, NOT and NAND
3	Sum of 'n' numbers using 'for' loop
4	Factorial of a given number using 'for' loop
5	Determine square of a given number
6	Factorial of a given number using 'while 'loop
7	Sorting even numbers using 'while' loop in an array
8	Finding the array maximum and array minimum
	Demonstration Experiments (For CIE)
9	Build a Virtual Instrument that simulates a heating and cooling system. The system must be able to be controlled manually or automatically.
10	Build a Virtual Instrument that simulates a Basic Calculator (using formula node).
11	Build a Virtual Instrument that simulates a Water Level Detector.
12	Demonstrate how to create a basic VI which calculates the area and perimeter of a circle.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Use Lab VIEW to create data acquisition, analysis and display operations
2. Create user interfaces with charts, graph and buttons
3. Use the programming structures and data types that exist in Lab VIEW
4. Use various editing and debugging techniques

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018.

The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
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- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Virtual Instrumentation using LABVIEW, Jovitha Jerome, PHI, 2011
2. Virtual Instrumentation using LABVIEW, Sanjay Gupta, Joseph John, TMH, McGraw Hill, Second Edition, 2011.

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VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E. in Electronics and Communication Engineering (ECE)

Scheme of Teaching and Examinations 2021

Outcome-Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 - 22)

MESTER

Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
			Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
			L	T	P	S					
BSC 21EC41	Maths for Communication Engineers	TD, PSB-Maths					03	50	50	100	3
IPCC 21EC42	Digital Signal Processing	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4
IPCC 21EC43	Circuits & Controls	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4
PCC 21EC44	Communication Theory	TD: ECE PSB: ECE	3	0	0	1	03	50	50	100	3
AEC 21BE45	Biology For Engineers	BT, CHE, PHY	2	0	0		02	50	50	100	2
PCC 21ECL46	Communication Laboratory I	TD: ECE PSB: ECE	0	0	2		03	50	50	100	1
HSMC 21KSK37/47	Samskrutika Kannada	HSMC	1	0	0		01	50	50	100	1
HSMC 21KBK37/47	Balake Kannada										
	OR										
HSMC 21CIP37/47	Constitution of India & Professional Ethics										
AEC 21EC48X	Ability Enhancement Course- IV	TD and PSB: Concerned department	If offered as theory Course: 1	0	0		01	50	50	100	1
			If offered as lab. course: 0	0	2		02				
UHV 21UH49	Universal Human Values	Any Department	1	0	0		01	50	50	100	1
INT 21INT49	Inter/Intra Institutional Internship	Evaluation By the appropriate authorities	Completed during the intervening period ofII and III semesters by students admitted to first year of BE./B.Tech and during the intervening period of III and IV semesters by Lateral entry students admitted to III semester.				3	100	--	100	2
							Total	550	450	1000	22

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

NCMC 21MATDIP41	Additional Mathematics - II	Maths	02	02	--	--	--	100	--	100	0

ote: BSC: Basic Science Course, IPCC: Integrated Professional Core Course, PCC: Professional Core Course, AEC –Ability Enhancement Courses, SMC: Humanity and Social Science and Management Courses, UHV- Universal Human Value Courses.

–Lecture, T – Tutorial, P- Practical/ Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

1KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and 21KBK37/47 Balake Kannada is for non-Kannada speaking, eading, and writing students.

ntegrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with Practicals of the same course. Credit for IPCC an be 04 and its Teaching – Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both y CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from practical part of IPCCshall be included in the SEE question paper.For more details the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech.) 2021-22 may be referred.

ion – credit mandatory course (NCMC):

Additional Mathematics - II:

1) Lateral entry Diploma holders admitted to III semester of B.E./B.Tech., shall attend the classes during the IV semester to complete all the

formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfil the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3)Successful completion of the course Additional Mathematics II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics II shall be indicated as Unsatisfactory.

Ability Enhancement Course - IV			
21EC481	Embedded C Basics	21EC483	Octave / Scilab for Signals
21EC482	C++ Basics	21EC484	DAQ using LabVIEW

Internship of 04 weeks during the intervening period of IV and V semesters; 21INT68Innovation/ Entrepreneurship/ Societal based Internship.

(1)All the students shall have to undergo a mandatory internship of 04 weeks during the intervening period of IV and V semesters. The internship hall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the VI semester grade card.The internship hall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / omplete the internship shall be considered under F (fail) grade and shall have to complete during subsequently after satisfying the internship equirements.

2)Innovation/ Entrepreneurship Internship shall be carried out at industry, State and Central Government /Non-government organizations (NGOs) nicro, small and medium enterprise (MSME), Innovation centres or Incubation centres. Innovation need not be a single major breakthrough; it can lso be a series of small or incremental changes. Innovation of any kind can also happen outside of the business world.

ntrepreneurship internships offers a chance to gain hands on experience in the world of entrepreneurship and helps to learn what it takes to run a mall entrepreneurial business by performing intern duties with an established company. This experience can then be applied to future business ndeavours. Start-ups and small companies are a preferred place to learn the business tack ticks for future entrepreneurs as learning how a small usiness operates will serve the intern well when he/she manages his/her own company. Entrepreneurship acts as a catalyst to open the minds to reativity and innovation. Entrepreneurship internship can be from several sectors, including technology, small and medium-sized, and the service ector.

3) Societal or social internship.

Irbanization is increasing on a global scale; and yet, half the world's population still resides in rural areas and is devoid of many things that urban opulation enjoy. Rural internship is a work-based activity in which students will have a chance to solve/reduce the problems of the rural place for etter living.

As proposed under the AICTE rural internship programme, activities under Societal or social internship, particularly in rural areas, shall be considered or 40 points under AICTE activity point programme.

IV Semester

Digital Signal Processing			
Course Code	21EC42	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives:

1. **Preparation:** To prepare students with fundamental knowledge/ overview in the field of Digital Signal Processing
2. **Core Competence:** To equip students with a basic foundation of Signal Processing by delivering the basics of Discrete Fourier Transforms & their properties, design of filters and overview of digital signal processors

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes
10. Give Programming Assignments

Module-1

Discrete Fourier Transforms (DFT): Frequency domain sampling and Reconstruction of Discrete Time Signals, The Discrete Fourier Transform, DFT as a linear transformation, Properties of the DFT: Periodicity, Linearity and Symmetry properties, Multiplication of two DFTs and Circular Convolution **[Text 1]**

Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

Module-2

Additional DFT Properties, Linear filtering methods based on the DFT: Use of DFT in Linear Filtering, Filtering of Long data Sequences. Fast-Fourier-Transform (FFT) algorithms: Efficient Computation of the DFT: Radix-2 FFT algorithms for the computation of DFT and IDFT decimation in-time **[Text 1]**

Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

Module-3

Design of FIR Filters: Characteristics of practical frequency-selective filters, Symmetric and Anti-symmetric FIR filters, Design of Linear-phase FIR (low pass and High pass) filters using windows - Rectangular, Hamming, Hanning, Bartlett windows. Structure for FIR Systems: Direct form, Cascade form and Lattice structures **[Text1]**

Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

Module-4

IIR Filter Design: Infinite Impulse response Filter Format, Bilinear Transformation Design Method, Analog Filters using Low pass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth (Lowpass and Highpass) Filter Design using BLT. Realization of IIR Filters in Direct form I and II **[Text 2]**

Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

Module-5

Digital Signal Processors: DSP Architecture, DSP Hardware Units, Fixed point format, Floating point Format, IEEE Floating point formats, Fixed point digital signal processors, FIR and IIR filter implementations in Fixed point systems. **[Text 2]**

Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC

List of Programs to be implemented & executed using any programming languages like C++/Python/Java/Scilab / MATLAB/CC Studio (but not limited to)

1. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum.
2. Computation of circular convolution of two given sequences and verification of commutative, distributive and associative property of convolution.
3. Computation of linear convolution of two sequences using DFT and IDFT.
4. Computation of circular convolution of two given sequences using DFT and IDFT
5. Verification of Linearity property, circular time shift property & circular frequency shift property of DFT.
6. Verification of Parseval's theorem
7. Design and implementation of IIR (Butterworth) low pass filter to meet given specifications.
8. Design and implementation of IIR (Butterworth) high pass filter to meet given specifications.
9. Design and implementation of low pass FIR filter to meet given specifications.
10. Design and implementation of high pass FIR filter to meet given specifications.
11. To compute N- Point DFT of a given sequence using DSK 6713 simulator
12. To compute linear convolution of two given sequences using DSK 6713 simulator
13. To compute circular convolution of two given sequences using DSK 6713 simulator

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Determine response of LTI systems using time domain and DFT techniques
2. Compute DFT of real and complex discrete time signals
3. Compute DFT using FFT algorithms
4. Design FIR and IIR Digital Filters
5. Design of Digital Filters using DSP processor

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Programming assignment at the end of 9th week of the semester, which can be implemented using programming languages like C++/Python/Java/Scilab

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50.

Suggested Learning Resources:

Text Books:

1. Proakis & Manolakis, "Digital Signal Processing - Principles Algorithms & Applications", 4th Edition, Pearson education, New Delhi, 2007. ISBN: 81-317-1000-9.
2. Li Tan, Jean Jiang, "Digital Signal processing - Fundamentals and Applications", Academic Press, 2013, ISBN: 978-0-12-415893.

Reference Books:

1. Sanjit K Mitra, "Digital Signal Processing, A Computer Based Approach", 4th Edition, McGraw Hill Education, 2013,
2. Oppenheim & Schaffer, "Discrete Time Signal Processing", PHI, 2003.
3. D Ganesh Rao and Vineeth P Gejji, "Digital Signal Processing" Cengage India Private Limited, 2017, ISBN: 9386858231

Web links and Video Lectures (e-Resources):

By Prof. S. C. Dutta Roy, IIT Delhi

https://nptel.ac.in/courses/117102060

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

Siddesh

H. O. D.

Dept. Of Electronics & Communication
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

IV Semester

Circuits & Controls			
Course Code	21EC43	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

1. Apply mesh and nodal techniques to solve an electrical network.
2. Solve different problems related to Electrical circuits using Network Theorems and Two port network.
3. Familiarize with the use of Laplace transforms to solve network problems.
4. Understand basics of control systems and design mathematical models using block diagram reduction, SFG, etc.
5. Understand Time domain and Frequency domain analysis.
6. Familiarize with the State Space Model of the system.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class .
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
- Give Programming Assignments.

Module-1

Basic concepts and network theorems

Types of Sources, Loop analysis, Nodal analysis with independent DC and AC Excitations.
(Textbook 1: 2.3, 4.1, 4.2, 4.3, 4.4, 10.6)
Super position theorem, Thevenin's theorem, Norton's Theorem, Maximum Power transfer Theorem.
(Textbook 2: 9.2, 9.4, 9.5, 9.7)

Teaching-Learning Process	Chalk and Talk, YouTube videos, Demonstrate the concepts using circuits **RBT Level:** L1, L2, L3

Module-2	
Two port networks: Short- circuit Admittance parameters, Open- circuit Impedance parameters, Transmission parameters, Hybrid parameters (Textbook 3: 11.1, 11.2, 11.3, 11.4, 11.5) **Laplace transform and its Applications**: Step Ramp, Impulse, Solution of networks using Laplace transform, Initial value and final value theorem (Textbook 3: 7.1, 7.2, 7.4, 7.7, 8.4)	
Teaching-Learning Process	Chalk and Talk **RBT Level:** L1, L2, L3
Module-3	
Basic Concepts and representation: Types of control systems, effect of feedback systems, differential equation of physical systems (only electrical systems), Introduction to block diagrams, transfer functions, Signal Flow Graphs (Textbook 4: Chapter 1.1, 2.2, 2.4, 2.5, 2.6)	
Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3
Module-4	
Time Response analysis: Time response of first order systems. Time response of second order systems, time response specifications of second order systems (Textbook 4: Chapter 5.3, 5.4) **Stability Analysis:** Concepts of stability necessary condition for stability, Routh stability criterion, relative stability Analysis (Textbook 4: Chapter 5.3, 5.4, 6.1, 6.2, 6.4, 6.5)	
Teaching-Learning Process	Chalk and Talk, Any software tool to show time response **RBT Level:** L1, L2, L3
Module-5	
Root locus: Introduction the root locus concepts, construction of root loci (Textbook 4: 7.1, 7.2, 7.3) **Frequency Domain analysis and stability**: Correlation between time and frequency response and Bode plots (Textbook 4: 8.1, 8.2, 8.4) **State Variable Analysis:** Introduction to state variable analysis: Concepts of state, state variable and state models. State model for Linear continuous –Time systems, solution of state equations. (Textbook 4: 12.2, 12.3, 12.6)	
Teaching-Learning Process	Chalk and Talk, Any software tool to plot Root locus, Bode plot **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC Using suitable hardware and simulation software, demonstrate the operation of the following circuits:	
Sl.No	**Experiments**
1	Verification of Superposition theorem
2	Verification of Thevenin's theorem
3	Speed torque characteristics of i)AC Servomotor ii) DC Servomotors
4	Determination of time response specification of a second order Under damped System, for different damping factors.
5	Determination of frequency response of a second order System
6	Determination of frequency response of a lead lag compensator
7	Using Suitable simulation package study of speed control of DC motor using i) Armature control ii) Field control

8	Using suitable simulation package, draw Root locus & Bode plot of the given transfer function.
Demonstration Experiments (For CIE only, not for SEE)	
9	Using suitable simulation package, obtain the time response from state model of a system.
10	Implementation of PI, PD Controllers.
11	Implement a PID Controller and hence realize an Error Detector.
12	Demonstrate the effect of PI, PD and PID controller on the system response.

Course Outcomes

At the end of the course the student will be able to:

1. Analyse and solve Electric circuit, by applying, loop analysis, Nodal analysis and by applying network Theorems.
2. Evaluate two port parameters of a network and Apply Laplace transforms to solve electric networks.
3. Deduce transfer function of a given physical system, from differential equation representation or Block Diagram representation and SFG representation.
4. Calculate time response specifications and analyse the stability of the system.
5. Draw and analyse the effect of gain on system behaviour using root loci.
6. Perform frequency response Analysis and find the stability of the system.
7. Represent State model of the system and find the time response of the system.

Assessment Details (both CIE and SEE)

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CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Second assignment at the end of 9th week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks.**

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and

scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

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SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured out of 100 shall be reduced proportionally to 50.

Suggested Learning Resources:

Text Books

1. Engineering circuit analysis, William H Hayt, Jr, Jack E Kemmerly, Steven M Durbin, Mc Graw Hill Education, Indian Edition 8e.
2. Networks and Systems, D Roy Choudhury, New age international Publishers, second edition.
3. Network Analysis, M E Van Valkenburg, Pearson, 3e.
4. Control Systems Engineering, I J Nagrath, M. Gopal, New age international Publishers, Fifth edition.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/courses/108106098
- https://nptel.ac.in/courses/108102042

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

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IV Semester

Communication Theory			
Course Code	21EC44	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives: This course will enable students to

- Understand and analyse concepts of Analog Modulation schemes viz; AM, FM., Low pass sampling and Quantization as a random process.
- Understand and analyse concepts digitization of signals viz; sampling, quantizing and encoding.
- Evolve the concept of SNR in the presence of channel induced noise and study Demodulation of analog modulated signals.
- Evolve the concept of quantization noise for sampled and encoded signals and study the concepts of reconstruction from these samples at a receiver.

Teaching-Learning Process (General Instructions)
These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

AMPLITUDE MODULATION: Introduction, Amplitude Modulation: Time & Frequency Domain description, Switching modulator, Envelop detector.
DOUBLE SIDE BAND-SUPPRESSED CARRIER MODULATION: Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing.
SINGLE SIDE-BAND AND VESTIGIAL SIDEBAND METHODS OF MODULATION: SSB Modulation, VSB Modulation, Frequency Translation, Frequency Division Multiplexing, Theme Example: VSB Transmission of Analog and Digital Television.

[Text1: 3.1 to 3.8]

Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Properties of the Fourier Transform, Dirac Delta Function. **RBT Level:** L1, L2, L3

Module-2

ANGLE MODULATION: Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM, Transmission bandwidth of FM Signals, Generation of FM Signals, Demodulation of FM Signals, FM Stereo Multiplexing, Phase-Locked Loop: Nonlinear model of PLL, Linear model of PLL, Nonlinear Effects in FM

Systems. The Superheterodyne Receiver [Text1: 4.1 to 4.6]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, YouTube videos. **Self-study topics:** FM Broadcasting System [Ref1] **RBT Level:** L1, L2, L3
Module-3	
NOISE: Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth. **NOISE IN ANALOG MODULATION**: Introduction, Receiver Model, Noise in DSB-SC receivers. Noise in AM receivers, Threshold effect, Noise in FM receivers, Capture effect, FM threshold effect, FM threshold reduction, Preemphasis and De-emphasis in FM (Text1: 5.10, 6.1 to 6.6)	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, YouTube videos. **Self-study topics:** Mean, Correlation and Covariance functions of Random Processes **RBT Level:** L1, L2, L3
Module-4	
SAMPLING AND QUANTIZATION: Introduction, Why Digitize Analog Sources? The Low pass Sampling process Pulse Amplitude Modulation. Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves. (Text1: 7.1 to 7.7)	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, YouTube videos. **Self-study topics:** T1 carrier systems [Ref1] **RBT Level:** L1, L2, L3
Module-5	
SAMPLING AND QUANTIZATION (Contd): The Quantization Random Process, Quantization Noise, Pulse–Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding, Filtering, Multiplexing; Delta Modulation (Text1: 7.8 to 7.10), Application examples - (a) Video + MPEG (Text1:7.11) and (b) Vocoders (refer Section 6.8 of Reference Book 1)	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, YouTube videos. **Self-study topics:** Digital Multiplexing. [Ref1] **RBT Level:** L1, L2, L3

Course Outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Understand the amplitude and frequency modulation techniques and perform time and frequency domain transformations.
2. Identify the schemes for amplitude and frequency modulation and demodulation of analog signals and compare the performance.
3. Characterize the influence of channel noise on analog modulated signals.
4. Understand the characteristics of pulse amplitude modulation, pulse position modulation and pulse code modulation systems.
5. Illustration of digital formatting representations used for Multiplexers, Vocoders and Video transmission.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. Simon Haykins & Moher, Communication Systems, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.

Reference Books

1. B P Lathi and Zhi Ding, Modern Digital and Analog Communication Systems, Oxford University Press., 4th edition, 2010, ISBN: 97801980738002.
2. Simon Haykins, An Introduction to Analog and Digital Communication, John Wiley India Pvt. Ltd., 2008, ISBN 978–81–265–3653–5.
3. H Taub & D L Schilling, Principles of Communication Systems, TMH, 2011.

Siddesh
H.O.D.
Dept. of Electronics & Communication
Sir M. Institute of Engg. & Technology
Nijar, [illegible] - 574 225

BIOLOGY FOR ENGINEERS

Course Code	21BE45	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	1:2:0:0 /2:0:0:0	SEE Marks	50
Total Hours of Pedagogy	25	Total Marks	100
Credits	02	Exam Hours	02

Course objectives:

- To familiarize the students with the basic biological concepts and their engineering applications.
- To enable the students with an understanding of biodesign principles to create novel devices and structures.
- To provide the students an appreciation of how biological systems can be re-designed as substitute products for natural systems.
- To motivate the students develop the interdisciplinary vision of biological engineering.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- ✓ Explanation via real life problem, situation modelling, and deliberation of solutions, hands-on sessions, reflective and questioning /inquiry-based teaching.
- ✓ Instructions with interactions in classroom lectures (physical/hybrid).
- ✓ Use of ICT tools, including YouTube videos, related MOOCs, AR/VR/MR tools.
- ✓ Flipped classroom sessions (~10% of the classes).
- ✓ Industrial visits, Guests talks and competitions for learning beyond the syllabus.
- ✓ Students' participation through audio-video based content creation for the syllabus (as assignments).
- ✓ Use of gamification tools (in both physical/hybrid classes) for creative learning outcomes.
- ✓ Students' seminars (in solo or group) /oral presentations.

Module-1 (5 Hours)

BIOMOLECULES AND THEIR APPLICATIONS (QUALITATIVE):

Carbohydrates (cellulose-based water filters, PHA and PLA as bioplastics), Nucleic acids (DNA Vaccine for Rabies and RNA vaccines for Covid19, Forensics – DNA fingerprinting), Proteins (Proteins as food – whey protein and meat analogs, Plant based proteins), lipids (biodiesel, cleaning agents/detergents), Enzymes (glucose-oxidase in biosensors, lignolytic enzyme in bio-bleaching).

Module-2 (5 Hours)

HUMAN ORGAN SYSTEMS AND BIO DESIGNS - 1 (QUALITATIVE):

Brain as a CPU system (architecture, CNS and Peripheral Nervous System, signal transmission, EEG, Robotic arms for prosthetics. Engineering solutions for Parkinson's disease).Eye as a Camera system (architecture of rod and cone cells, optical corrections, cataract, lens materials, bionic eye).Heart as a pump system (architecture, electrical signalling - ECG monitoring and heart related issues, reasons for blockages of blood vessels, design of stents, pace makers, defibrillators).

Module-3 (5 Hours)

HUMAN ORGAN SYSTEMS AND BIO-DESIGNS - 2 (QUALITATIVE):

Lungs as purification system (architecture, gas exchange mechanisms, spirometry, abnormal lung physiology - COPD, Ventilators, Heart-lung machine).Kidney as a filtration system (architecture, mechanism of filtration, CKD, dialysis systems). Muscular and Skeletal Systems as scaffolds (architecture, mechanisms, bioengineering solutions for muscular dystrophy and osteoporosis).

Module-4 (5 Hours)

NATURE-BIOINSPIRED MATERIALS AND MECHANISMS (QUALITATIVE):

Echolocation (ultrasonography, sonars), Photosynthesis (photovoltaic cells, bionic leaf). Bird flying (GPS and aircrafts), Lotus leaf effect (Super hydrophobic and self-cleaning surfaces), Plant burrs (Velcro), Shark skin (Friction reducing swim suits), Kingfisher beak (Bullet train). Human Blood substitutes - hemoglobin-based oxygen carriers (HBOCs) and perfluorocarbons (PFCs).

Module-5 (5 Hours)

TRENDS IN BIOENGINEERING (QUALITATIVE):

Bioprinting techniques and materials, 3D printing of ear, bone and skin. 3D printed foods. Electrical tongue and electrical nose in food science, DNA origami and Biocomputing, Bioimaging and Artificial Intelligence for disease diagnosis. Self-healing Bioconcrete (based on bacillus spores, calcium lactate nutrients and biomineralization processes) and Bioremediation and Biomining via microbial surface adsorption (removal of heavy metals like Lead, Cadmium, Mercury, Arsenic).

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

- Elucidate the basic biological concepts via relevant industrial applications and case studies.
- Evaluate the principles of design and development, for exploring novel bioengineering projects.
- Corroborate the concepts of biomimetics for specific requirements.
- Think critically towards exploring innovative biobased solutions for socially relevant problems.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation:

Three Unit Tests each of 20 Marks (duration 01 hour)

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester
- Third test at the end of the 15th week of the semester

Two assignments each of 10 Marks

- First assignment at the end of 4th week of the semester
- Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for20 Marks (duration 01 hours)

- At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be scaled down to 50 marks

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 2 sub-questions), should have a mix of topics under that module.

The students have to answer 5 full questions, selecting one full question from each module.

The SEE question paper will be set for 100 marks and marks scored will be proportionately reduced to 50 marks

Suggested Learning Resources:

- Human Physiology, Stuart Fox, Krista Rompolski, McGraw-Hill eBook. 16th Edition, 2022
- Biology for Engineers, Thyagarajan S., Selvamurugan N., Rajesh M.P., Nazeer R.A., Thilagaraj W., Barathi S., and Jaganthan M.K., Tata McGraw-Hill, New Delhi, 2012.
- Biology for Engineers, Arthur T. Johnson, CRC Press, Taylor and Francis, 2011
- Biomedical Instrumentation, Leslie Cromwell, Prentice Hall 2011.
- Biology for Engineers, Sohini Singh and Tanu Allen, Vayu Education of India, New Delhi, 2014.
- Biomimetics: Nature-Based Innovation, Yoseph Bar-Cohen, 1st edition, 2012, CRC Press.
- Bio-Inspired Artificial Intelligence: Theories, Methods and Technologies, D. Floreano and C. Mattiussi, MIT Press, 2008.
- Bioremediation of heavy metals: bacterial participation, by C R Sunilkumar, N Geetha A C Udayashankar Lambert Academic Publishing, 2019.
- 3D Bioprinting: Fundamentals, Principles and Applications by Ibrahim Ozbolat, Academic Press, 2016.
- Electronic Noses and Tongues in Food Science, Maria Rodriguez Mende, Academic Press, 2016

- Blood Substitutes, Robert Winslow, Elsevier, 2005

Web links and Video Lectures (e-Resources):

- VTU EDUSAT / SWAYAM / NPTEL / MOOCS / Coursera / MIT-open learning resource
- https://nptel.ac.in/courses/121106008
- https://freevideolectures.com/course/4877/nptel-biology-engineers-other-non-biologists
- https://ocw.mit.edu/courses/20-020-introduction-to-biological-engineering-design-spring-2009
- https://ocw.mit.edu/courses/20-010j-introduction-to-bioengineering-be-010j-spring-2006
- https://www.coursera.org/courses?query=biology
- https://onlinecourses.nptel.ac.in/noc19_ge31/preview
- https://www.classcentral.com/subject/biology
- https://www.futurelearn.com/courses/biology-basic-concepts

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Group Discussion of Case studies
- Model Making and seminar/poster presentations
- Design of novel device/equipment like Cellulose-based water filters, Filtration system mimicking the kidney, Bioremediation unit for E-waste management, AI and ML based Bioimaging,

Siddesh
H.O.D.
Dept. Of Electronics & Communication Engg.
Alva's Institute of Engg. & Technology,
Mijar, MOODBIDRI - 574 225

IV Semester

Communication Laboratory I			
Course Code	21ECL46	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Model an analog communication system signal transmission and reception.
- Realize the electronic circuits to perform analog and pulse modulations and demodulations.
- Verify the sampling theorem and relate the signal and its spectrum before and after sampling.
- Understand the process of PCM and delta modulations.
- Understand the PLL operation.

Sl.No.	Experiments
1	Design of active second order Butterworth low pass and high pass filters.
2	Amplitude Modulation and Demodulation of (a) Standard AM and (b) DSBSC (LM741 and LF398 ICs can be used)
3	Frequency modulation and demodulation
4	Design and test Time Division Multiplexing and Demultiplexing of two bandlimited signals.
5	Design and test i) Pulse sampling, flat top sampling and reconstruction. ii) Pulse amplitude modulation and demodulation.
6	Design and test BJT/FET Mixer
7	Pulse Code Modulation and demodulation
8	Phase locked loop Synthesis
9	Illustration of (a) AM modulation and demodulation and display the signal and its spectrum. (b) DSB-SC modulation and demodulation and display the signal and its spectrum. (Use MATLAB/SCILAB)
10	Illustration of FM modulation and demodulation and display the signal and its spectrum. (Use MATLAB/SCILAB)
11	Illustrate the process of sampling and reconstruction of low pass signals. Display the signals and its spectrums of both analog and sampled signals. (Use MATLAB/SCILAB).
12	Illustration of Delta Modulation and the effects of step size selection in the design of DM encoder. (Use MATLAB/SCILAB)

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Demonstrate the AM and FM modulation and demodulation by representing the signals in time and frequency domain.
2. Design and test the sampling, Multiplexing and PAM with relevant circuits.
3. Demonstrate the basic circuitry and operations used in AM and FM receivers.
4. Illustrate the operation of PCM and delta modulations for different input conditions.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by

[illegible]

[illegible]

Suggested Learning Resources

1. [illegible] Principles of Electronic Communication Systems, McGraw Hill Education (India) Private Limited, 2014.
2. B. P. Lathi, Zhi Ding, Modern Digital and Analog Communication Systems, Oxford University Press, 2010.

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III/IV Semester

Constitution of India and Professional Ethics (CIP)			
Course Code	21CIP37/47	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	L:0,T:2,P:0 = 02 Hours	SEE Marks	50
Total Hours of Pedagogy	02 Hours/Week	Total Marks	100
Credits	01	Exam Hours	01 Hours

Course objectives: This course will enable the students

1. To know about the basic structure of Indian Constitution.
2. To know the Fundamental Rights (FR's), DPSP's and Fundamental Duties (FD's) of our constitution.
3. To know about our Union Government, political structure & codes, procedures.
4. To know the State Executive & Elections system of India.
5. To learn the Amendments and Emergency Provisions, other important provisions given by the constitution.

Teaching-Learning Process

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes and make Teaching -Learning more effective: Teachers shall adopt suitable pedagogy for effective teaching - learning process. The pedagogy shall involve the combination of different methodologies which suit modern technological tools.

(i) Direct instructional method (Low/Old Technology), (ii) Flipped classrooms (High/advanced Technological tools), (iii) Blended learning (Combination of both), (iv) Enquiry and evaluation based learning, (v) Personalized learning, (vi) Problems based learning through discussion.

Apart from conventional lecture methods, various types of innovative teaching techniques through videos, animation films may be adapted so that the delivered lesson can progress the students In theoretical applied and practical skills.

Module - 1

Introduction to Indian Constitution: The Necessity of the Constitution, The Societies before and after the Constitution adoption. Introduction to the Indian constitution, The Making of the Constitution, The Role of the Constituent Assembly. The Preamble of Indian Constitution & Key concepts of the Preamble. Salient features of India Constitution.

Module - 2

FR's, FD's and DPSP's: Fundamental Rights and its Restriction and limitations in different Complex Situations. Directive Principles of State Policy (DPSP) and its present relevance in our society with examples. Fundamental Duties and its Scope and significance in Nation building.

Module - 3

Union Executive : Parliamentary System, Union Executive – President, Prime Minister, Union Cabinet, Parliament - LS and RS, Parliamentary Committees, Important Parliamentary Terminologies. Supreme Court of India, Judicial Reviews and Judicial Activism.

Module - 4

State Executive & Elections, Amendments and Emergency Provisions: State Executive, Election Commission, Elections & Electoral Process. Amendment to Constitution (How and Why) and Important Constitutional Amendments till today. Emergency Provisions.

Module-5

Professional Ethics: Ethics & Values. Types of Ethics. Scope & Aims of Professional & Engineering Ethics. Positive and Negative Faces of Engineering Ethics. Clash of Ethics, Conflicts of Interest. The impediments to Responsibility. Trust & Reliability in Engineering, IPRs (Intellectual Property Rights), Risks, Safety and liability in Engineering.

Course outcome (Course Skill Set) :

At the end of the course the student will be able to :

CO1	Analyse the basic structure of Indian Constitution.
CO2	Remember their Fundamental Rights, DPSP's and Fundamental Duties (FD's) of our constitution.
CO3	know about our Union Government, political structure & codes, procedures.
CO4	Understand our State Executive & Elections system of India.
CO5	Remember the Amendments and Emergency Provisions, other important provisions given by the constitution.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation:

Three Unit Tests each of 20 Marks (**duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of 10 Marks

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be scaled down to 50 marks

Total CIE : IA 20*3=60, Assignment 10+10=20, Quiz 20 = 100 /2 = 50

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject **(duration 02 hours)**

1. The question paper will have 50 questions. Each question is set for 01 mark.
2. Semester End Exam (SEE) Pattern will be in MCQ Model (Multiple Choice Questions) for 50 marks (60 minutes duration).

Suggested Learning Resources:

Textbook:

1. "Constitution of India" (for Competitive Exams) - Published by Naidhruva Edutech Learning Solutions, Bengaluru. – 2022.
2. "Engineering Ethics", M.Govindarajan, S.Natarajan, V.S.Senthilkumar, Prentice –Hall, 2004.

Reference Books:

1. "Samvidhana Odu" - for Students & Youths by Justice **HN Nagamohan Dhas, Sahayana, kerekon.**
2. "Constitution of India, Professional Ethics and Human Rights" by Shubham Singles, Charles E. Haries, and et al: published by Cengage Learning India, Latest Edition – 2019.
3. "Introduction to the Constitution of India", (Students Edition.) by Durga Das Basu (**DD Basu**): Prentice –Hall, 2008.
4. "The Constitution of India" by Merumandan K B: published by Merugu Publication, Second Edition, Bengaluru.

Siddesh
H. O. D.
Dept. Of Electronics & Communication
Alva's Institute of Engg. & Technology
Mijar MOODBIDRI 574 225

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering

NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 – 22)

IV Semester

C++ Basics			
Course Code	21EC482	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- Understand object-oriented programming concepts, and apply them in solving problems.
- To create, debug and run simple C++ programs.
- Introduce the concepts of functions, friend functions, inheritance, polymorphism and function overloading.
- Introduce the concepts of exception handling and multithreading.

Sl.No	Experiments
1	Write a C++ program to find largest, smallest & second largest of three numbers using inline functions MAX & Min.
2	Write a C++ program to calculate the volume of different geometric shapes like cube, cylinder and sphere using function overloading concept.
3	Define a STUDENT class with USN, Name & Marks in 3 tests of a subject. Declare an array of 10 STUDENT objects. Using appropriate functions, find the average of the two better marks for each student. Print the USN, Name & the average marks of all the students.
4	Write a C++ program to create class called MATRIX using two-dimensional array of integers, by overloading the operator == which checks the compatibility of two matrices to be added and subtracted. Perform the addition and subtraction by overloading + and – operators respectively. Display the results by overloading the operator <<. If (m1 == m2) then m3 = m1 + m2 and m4 = m1 – m2 else display error
5	Demonstrate simple inheritance concept by creating a base class FATHER with data members: *First Name, Surname, DOB & bank Balance* and creating a derived class SON, which inherits: Surname & Bank Balance feature from base class but provides its own feature: First Name & DOB. Create & initialize F1 & S1 objects with appropriate constructors & display the FATHER & SON details.
6	Write a C++ program to define class name FATHER & SON that holds the income respectively. Calculate & display total income of a family using Friend function.
7	Write a C++ program to accept the student detail such as name & 3 different marks by get_data() method & display the name & average of marks using display() method. Define a friend function for calculating the average marks using the method mark_avg().
8	Write a C++ program to explain virtual function (Polymorphism) by creating a base class polygon which has virtual function areas two classes rectangle & triangle derived from polygon & they have area to calculate & return the area of rectangle & triangle respectively.
9	Design, develop and execute a program in C++ based on the following requirements: An EMPLOYEE class containing data members & members functions: i) Data members: employee number (an integer), Employee_ Name (a string of characters), Basic_ Salary (in integer), All_ Allowances (an integer), Net_Salary (an integer). (ii) Member functions: To read the data of an employee, to calculate Net_Salary & to print the values of all the data members. (All_Allowances = 123% of Basic, Income Tax (IT) =30% of gross salary (=basic_ Salary_All_Allowances_IT).
10	Write a C++ program with different class related through multiple inheritance & demonstrate the use of different access specified by means of members variables & members functions.
11	Write a C++ program to create three objects for a class named count object with data members

	such as roll_no & Name. Create a members function set_data ( ) for setting the data values & display ( ) member function to display which object has invoked it using „this" pointer.
12	Write a C++ program to implement exception handling with minimum 5 exceptions classes including two built in exceptions.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Write C++ program to solve simple and complex problems
2. Apply and implement major object-oriented concepts like message passing, function overloading, operator overloading and inheritance to solve real-world problems.
3. Use major C++ features such as Templates for data type independent designs and File I/O to deal with large data set.
4. Analyze, design and develop solutions to real-world problems applying OOP concepts of C++

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and

result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.
The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Object oriented programming in TURBO C++, Robert Lafore, Galgotia Publications, 2002
2. The Complete Reference C++, Herbert Schildt, 4th Edition, Tata McGraw Hill, 2003.
3. Object Oriented Programming with C++, E Balaguruswamy, 4th Edition, Tata McGraw Hill, 2006.

Siddesh
H.O.D.
Dept. Of Electronics & Communication
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI-574 225

SAMPLE TEMPLATE

IV Semester

UNIVERSAL HUMAN VALUES-II: UNDERSTANDING HARMONY and ETHICAL HUMAN CONDUCT			
Title of the subject			
Course Code	21UHV49	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	2:0:0	SEE Marks	50
Total Hours of Pedagogy	20	Total Marks	100
Credits	01	Exam Hours	01

Course objectives:

This introductory course input is intended:

1. To help the students appreciate the essential complementarity between 'VALUES' and 'SKILLS' to ensure sustained happiness and prosperity which are the core aspirations of all human beings.
2. To facilitate the development of a Holistic perspective among students towards life and profession as well as towards happiness and prosperity based on a correct understanding of the Human reality and the rest of existence. Such a holistic perspective forms the basis of Universal Human Values and movement towards value-based living in a natural way.
3. To highlight plausible implications of such a Holistic understanding in terms of ethical human conduct, trustful and mutually fulfilling human behaviour and mutually enriching interaction with Nature.

This course is intended to provide a much-needed orientational input in value education to the young enquiring minds.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. The methodology of this course is explorational and thus universally adaptable. It involves a systematic and rational study of the human being vis-à-vis the rest of existence.
2. The course is in the form of 20 lectures (discussions)
3. It is free from any dogma or value prescriptions.
4. It is a process of self-investigation and self-exploration, and not of giving sermons. Whatever is found as truth or reality is stated as a proposal and the students are facilitated to verify it in their own right, based on their Natural Acceptance and subsequent Experiential Validation – the whole existence is the lab and every activity is a source of reflection.
5. This process of self-exploration takes the form of a dialogue between the teacher and the students to begin with, and then to continue within the student in every activity, leading to continuous self-evolution.
6. This self exploration also enables them to critically evaluate their pre-conditionings and present beliefs.

Module-1

Introduction to Value Education (4 hours)

Right Understanding, Relationship and Physical Facility (Holistic Development and the Role of Education)

Understanding Value Education, Self-exploration as the Process for Value Education, Continuous Happiness and Prosperity – the Basic Human Aspirations, Happiness and Prosperity – Current Scenario, Method to Fulfil the Basic Human Aspirations

Teaching-Learning Process	Introduction to Value Education- Chalk and talk method, Discussion, Sharing of experiences, Live Examples and videos

Module-2	
Harmony in the Human Being (4 hours) Understanding Human being as the Co-existence of the Self and the Body, Distinguishing between the Needs of the Self and the Body, The Body as an Instrument of the Self, Understanding Harmony in the Self, Harmony of the Self with the Body, Programme to ensure self-regulation and Health	
Teaching-Learning Process	Introduction to the concepts- Chalk and talk method, Discussion, Sharing of experiences, Live Examples and videos
Module-3	
Harmony in the Family and Society (4 hours) Harmony in the Family – the Basic Unit of Human Interaction, 'Trust' – the Foundational Value in Relationship, 'Respect' – as the Right Evaluation, Other Feelings, Justice in Human-to-Human Relationship, Understanding Harmony in the Society, Vision for the Universal Human Order	
Teaching-Learning Process	Introduction to the concepts- Chalk and talk method, Discussion, Sharing of experiences, Live Examples and videos
Module-4	
Harmony in the Nature/Existence (4 hours) Understanding Harmony in the Nature, Interconnectedness, self-regulation and Mutual Fulfilment among the Four Orders of Nature, Realizing Existence as Co-existence at All Levels, The Holistic Perception of Harmony in Existence	
Teaching-Learning Process	Introduction to the concepts- Chalk and talk method, Discussion, Sharing of experiences, Live Examples and videos
Module-5	
Implications of the Holistic Understanding – a Look at Professional Ethics (4 hours) Natural Acceptance of Human Values, Definitiveness of (Ethical) Human Conduct, A Basis for Humanistic Education, Humanistic Constitution and Universal Human Order, Competence in Professional Ethics Holistic Technologies, Production Systems and Management Models-Typical Case Studies, Strategies for Transition towards Value-based Life and Profession	
Teaching-Learning Process	Introduction to the concepts- Chalk and talk method, Discussion, Sharing of experiences, Live Examples and videos
Course outcome (Course Skill Set) By the end of the course, students are expected to become more aware of themselves, and their surroundings (family, society, nature); they would become more responsible in life, and in handling problems with sustainable solutions, while keeping human relationships and human nature in mind. They would have better critical ability. They would also become sensitive to their commitment towards what they have understood (human values, human relationship and human society). It is hoped that they would be able to apply what they have learnt to their own self in different day-to-day settings in real life, at least a beginning would be made in this direction.	

Therefore, the course and further follow up is expected to positively impact common graduate attributes like:

1. Holistic vision of life
2. Socially responsible behaviour
3. Environmentally responsible work
4. Ethical human conduct
5. Having Competence and Capabilities for Maintaining Health and Hygiene
6. Appreciation and aspiration for excellence (merit) and gratitude for all

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject / course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation:

Three Unit Tests each of 20 Marks (duration 01 hour)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of 10 Marks

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (duration **01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be scaled down to 50 marks

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (duration 01 hours)

1. The question paper will have 50 questions. Each question is set for 01 marks.
2. The students have to answer all the questions, selecting one full question from each module

Suggested Learning Resources:

Books

-READINGS:

Text Book and Teachers Manual

a. The Textbook

A Foundation Course in Human Values and Professional Ethics, R R Gaur, R Asthana, G P Bagaria, 2nd Revised Edition, Excel Books, New Delhi, 2019. ISBN 978-93-87034-47-1

b. The Teacher"s Manual

Teachers" Manual for *A Foundation Course in Human Values and Professional Ethics*, R R Gaur, R Asthana, G

Reference Books

1. JeevanVidya: EkParichaya, A Nagaraj, JeevanVidyaPrakashan, Amarkantak, 1999.
2. Human Values, A.N. Tripathi, New Age Intl. Publishers, New Delhi, 2004.
3. The Story of Stuff (Book).
4. The Story of My Experiments with Truth - by Mohandas Karamchand Gandhi
5. Small is Beautiful - E. F Schumacher.
6. Slow is Beautiful - Cecile Andrews
7. Economy of Permanence - J C Kumarappa
8. Bharat Mein Angreji Raj – Pandit Sunderlal
9. Rediscovering India - by Dharampal
10. Hind Swaraj or Indian Home Rule - by Mohandas K. Gandhi
11. India Wins Freedom - Maulana Abdul Kalam Azad
12. Vivekananda - Romain Rolland (English)
13. Gandhi - Romain Rolland (English)
14. Sussan George, 1976, How the Other Half Dies, Penguin Press. Reprinted 1986, 1991
15. Donella H. Meadows, Dennis L. Meadows, Jorgen Randers, William W. Behrens III, 1972, Limits to Growth – Club of Rome's report, Universe Books.
16. A Nagraj, 1998, Jeevan Vidya Ek Parichay, Divya Path Sansthan, Amarkantak.
17. P L Dhar, RR Gaur, 1990, Science and Humanism, Commonwealth Publishers.
18. A N Tripathy, 2003, Human Values, New Age International Publishers.
19. SubhasPalekar, 2000, How to practice Natural Farming, Pracheen (Vaidik) KrishiTantraShodh, Amravati.
20. E G Seebauer & Robert L. Berry, 2000, Fundamentals of Ethics for Scientists & Engineers , Oxford University Press
21. M Govindrajran, S Natrajan & V.S. Senthil Kumar, Engineering Ethics (including Human Values), Eastern Economy Edition, Prentice Hall of India Ltd.
22. B P Banerjee, 2005, Foundations of Ethics and Management, Excel Books.
23. B L Bajpai, 2004, Indian Ethos and Modern Management, New Royal Book Co., Lucknow. Reprinted 2008.

Web links and Video Lectures (e-Resources):

1. Value Education websites, https://www.uhv.org.in/uhv-ii, http://uhv.ac.in, http://www.uptu.ac.in
2. Story of Stuff, http://www.storyofstuff.com
3. Al Gore, An Inconvenient Truth, Paramount Classics, USA
4. Charlie Chaplin, Modern Times, United Artists, USA
5. IIT Delhi, Modern Technology – the Untold Story
6. Gandhi A., Right Here Right Now, Cyclewala Productions
7. https://www.youtube.com/channel/UCQxWr5QB_eZUnwxSwxXEkQw
8. https://dp-si.iicte-india.org/8dayUHV_download.php
9. https://www.youtube.com/watch?v=8ovkLRYXIjE
10. https://www.youtube.com/watch?v=OgdNx0X923I
11. https://www.youtube.com/watch?v=nGRcbRpvGoU
12. https://www.youtube.com/watch?v=sDxGXOgYEKM

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

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Siddesh

H. O. D.
Dept. Of Electronics & Communica[illegible]
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 2[illegible]

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E. in Electronics and Communication Engineering (ECE)

Scheme of Teaching and Examinations 2021

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 - 22)

III SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21MAT31	Mathematics Course (Common to all)	TD- Maths PSB-Maths					03	50	50	100	3
2	IPCC 21EC32	Digital System Design using Verilog	TD: ECE PSB: ECE	3	0	2		03	50	50	100	
3	IPCC 21EC33	Basic Signal Processing	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4
4	PCC 21EC34	Analog Electronic Circuits	TD: ECE PSB: ECE	3	0	0	1	03	50	50	100	3
5	PCC 21ECL35	Analog and Digital Electronics Lab	TD: ECE PSB: ECE	0	0	2		03	50	50	100	1
6	UHV 21UH36	Social Connect and Responsibility	Any Department	0	0	1		01	50	50	100	1
7	HSMC 21KSK37/47	Samskrutika Kannada	TD and PSB HSMC	1	0	0		01	50	50	100	1
	HSMC 21KBK37/47	Balake Kannada										
	OR											
	HSMC 21CIP37/47	Constitution of India and Professional Ethics										
8	AEC 21EC38X	Ability Enhancement Course - III	TD: Concerned department PSB: Concerned Board	If offered as Theory Course: 1	0	0		01	50	50	100	1
				If offered as lab. course: 0	0	2		02				
								Total	**400**	**400**	**800**	**18**

9	Scheduled activities for III to VIII semesters	NMDC 21NS83	National Service Scheme (NSS)	NSS	All students have to register for any one of the course namely National Service Scheme, Physical Education (PE)(Sports and Athletics) and Yoga with the concerned coordinator of the course during the first week of III semester. The activities shall be carried out between III semester to VIII semester (for 5 semesters). SEE in the above courses shall be conducted during VIII semester examinations and the accumulated CIE marks shall be added to the SEE marks. Successful completion of the registered course is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE and Yoga activities.
		NMDC 21PE83	Physical Education (PE)(Sports and Athletics)	PE	
		NMDC 21YO83	Yoga	Yoga	

Course prescribed to lateral entry Diploma holders admitted to III semester B.E./B.Tech programs

1	NCMC 21MATDIP31	Additional Mathematics - I	Maths	02	02	--	--	---	100	---	100	0

Note: BSC: Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course.
L –Lecture, **T** – Tutorial, P- Practical/ Drawing, **S** – Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination.**TD**-Teaching Department, **PSB**: Paper Setting department

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and **21KBK37/47** Balake Kannada is for non-Kannada speaking, reading, and writing students.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2021-22 may be referred.

21INT49Inter/Intra Institutional Internship: All the students admitted to engineering programs under the lateral entry category shall have to undergo a mandatory 21INT49 Inter/Intra Institutional Internship of 03 weeks during the intervening period of III and IV semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the IV semester grade card. The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequently after satisfying the internship requirements. The faculty coordinator or mentor shall monitor the students' internship progress and interact with them for the successful completion of the internship.

Non–credit mandatory courses (NCMC):

(A) Additional Mathematics I and II:

(1)These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3)Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

(B) National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses sha be mandatory for the award of degree.

Ability Enhancement Course - III			
21EC381	LD (Logic Design) Lab using Pspice / MultiSIM	21EC383	LIC (Linear Integrated Circuits) Lab using Pspice / MultiSIM
21EC382	AEC (Analog Electronic Circuits) Lab	21EC384	LabVIEW Programming Basics

VISVESVARAVA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

III Semester

Digital System Design Using Verilog			
Course Code	21EC32	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 13 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

1. To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques.
2. To impart the concepts of designing and analyzing combinational logic circuits.
3. To impart design methods and analysis of sequential logic circuits.
4. To impart the concepts of Verilog HDL-data flow and behavioral models for the design of digital systems.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class .
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
- Give Programming Assignments.

Module-1

Principles of Combinational Logic: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps- up to 4 variables, Quine-McCluskey Minimization Technique, Quine-McCluskey using Don't Care Terms. (Section 3.1 to 3.5 of Text 1).

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-2

Logic Design with MSI Components and Programmable Logic Devices: Binary Adders and Subtractors, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices (PLDs) (Section 5.1 to 5.7 of Text 2)

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-3	
Flip-Flops and its Applications: The Master-Slave Flip-flops (Pulse-Triggered flip-flops): SR flip-flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, JK, D and SR flip-flops. (Section 6.4, 6.6 to 6.9 (Excluding 6.9.3) of Text 2)	
Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-4	
Introduction to Verilog: Structure of Verilog module, Operators, Data Types, Styles of Description. (Section 1.1 to 1.6.2, 1.6.4 (only Verilog), 2 of Text 3) **Verilog Data flow description:** Highlights of Data flow description, Structure of Data flow description. (Section 2.1 to 2.2 (only Verilog) of Text 3)	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

Module-5	
Verilog Behavioral description: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers (2:1, 4:1, 8:1). (Section 3.1 to 3.4 (only Verilog) of Text 3) **Verilog Structural description**: Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder. (Section 4.1 to 4.2 of Text 3)	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Using suitable simulation software, demonstrate the operation of the following circuits:

Sl.No	Experiments
1	To simplify the given Boolean expressions and realize using Verilog program.
2	To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description.
3	To realize 4-bit ALU using Verilog program.
4	To realize the following Code converters using Verilog Behavioral description a) Gray to binary and vice versa b) Binary to excess3 and vice versa
5	To realize using Verilog Behavioral description: 8:1 mux, 8:3 encoder, Priority encoder
6	To realize using Verilog Behavioral description: 1:8 Demux, 3:8 decoder, 2-bit Comparator
7	To realize using Verilog Behavioral description: Flip-flops: a) JK type b) SR type c) T type and d) D type
8	To realize Counters - up/down (BCD and binary) using Verilog Behavioral description.
Demonstration Experiments (For CIE only – not to be included for SEE) Use FPGA/CPLD kits for downloading Verilog codes and check the output for interfacing experiments.	
9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
10	Verilog programs to interface a Relay or ADC to the FPGA/CPLD and demonstrate its working.
11	Verilog programs to interface DAC to the FPGA/CPLD for Waveform generation.
12	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

Course Outcomes

At the end of the course the student will be able to:

1. Simplify Boolean functions using K-map and Quine-McCluskey minimization technique.
2. Analyze and design for combinational logic circuits.
3. Analyze the concepts of Flip Flops (SR, D, T and JK) and to design the synchronous sequential circuits using Flip Flops.
4. Model Combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Second assignment at the end of 9th week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured out of 100 will be scaled down to 50 marks.

Suggested Learning Resources:

Text Books

1. Digital Logic Applications and Design by John M Yarbrough, Thomson Learning, 2001.
2. Digital Principles and Design by Donald D Givone, McGraw Hill, 2002.
3. HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dreamtech press.

Reference Books:

1. Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning
2. Logic Design, by Sudhakar Samuel, Pearson/ Sanguine, 2007
3. Fundamentals of HDL, by Cyril P R, Pearson/Sanguine 2010

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills.

H.O.D.
Dept. Of Electronics & Communicatio...
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

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B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

III Semester

Basic Signal Processing			
Course Code	21EC33	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 13 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

Preparation: To prepare students with fundamental knowledge/ overview in the field of Signal Processing with Familiarization with the concept of Vector spaces and orthogonality with a qualitative insight into applications in communications.

Core Competence: To equip students with a basic foundation of Signal Processing by delivering the basics of quantitative parameters for Matrices & Linear Transformations, the mathematical description of discrete time signals and systems, analyzing the signals in time domain using convolution sum, classifying signals into different categories based on their properties, analyzing Linear Time Invariant (LTI) systems in time and transform domains

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
- Give Programming Assignments.

Module-1

Vector Spaces: Vector spaces and Null subspaces, Rank and Row reduced form, Independence, Basis and dimension, Dimensions of the four subspaces, Rank-Nullity Theorem, Linear Transformations Orthogonality: Orthogonal Vectors and Subspaces, Projections and Least squares, Orthogonal Bases and Gram-Schmidt Orthogonalization procedure

(Refer Chapters 2 and 3 of Text 1)

Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Module-2	
Eigen values and Eigen vectors: Review of Eigen values and Diagonalization of a Matrix, Special Matrices (Positive Definite, Symmetric) and their properties, Singular Value Decomposition. **(Refer Chapter 5, Text 1)**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Module-3	
Introduction and Classification of signals: Definition of signal and systems with examples, Elementary signals/Functions: Exponential, sinusoidal, step, impulse and ramp functions **Basic Operations on signals:** Amplitude scaling, addition, multiplication, time scaling, time shift and time reversal. Expression of triangular, rectangular and other waveforms in terms of elementary signals **System Classification and properties:** Linear-nonlinear, Time variant -invariant, causal-noncausal, static-dynamic, stable-unstable, invertible. **(Text 2) [Only for Discrete Signals & Systems]**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Module-4	
Time domain representation of LTI System: Impulse response, convolution sum. Computation of convolution sum using graphical method for unit step and unit step, unit step and exponential, exponential and exponential, unit step and rectangular, and rectangular and rectangular. **LTI system Properties in terms of impulse response:** System interconnection, Memory less, Causal, Stable, Invertible and Deconvolution and step response **(Text 2) [Only for Discrete Signals & Systems]**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Module-5	
The Z-Transforms: Z transform, properties of the region of convergence, properties of the Z-transform, Inverse Z-transform by partial fraction, Causality and stability, Transform analysis of LTI systems. **(Text 2)**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC	
Sl.No	**Experiments**
1	a. Program to create and modify a vector (array). b. Program to create and modify a matrix.
2	Programs on basic operations on matrix.
3	Program to solve system of linear equations.
4	Program for Gram-Schmidt orthogonalization.
5	Program to find Eigen value and Eigen vector.
6	Program to find Singular value decomposition.

7	Program to generate discrete waveforms.
8	Program to perform basic operation on signals.
9	Program to perform convolution of two given sequences.
10	a. Program to perform verification of commutative property of convolution. b. Program to perform verification of distributive property of convolution. c. Program to perform verification of associative property of convolution.
11	Program to compute step response from the given impulse response.
12	Programs to find Z-transform and inverse Z-transform of a sequence.

Course outcomes (Course Skill Set)

At the end of the course the student will be able to :

1. Understand the basics of Linear Algebra
2. Analyse different types of signals and systems
3. Analyse the properties of discrete-time signals & systems
4. Analyse discrete time signals & systems using Z transforms

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Programming assignment at the end of 9th week of the semester, which can be implemented using programming languages like C++/Python/Java/Scilab

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured out of 100 will be scaled down to 50 marks.

Suggested Learning Resources:

Text Books

1. Gilbert Strang, "Linear Algebra and its Applications", Cengage Learning, 4th Edition, 2006, ISBN 97809802327
2. Simon Haykin and Barry Van Veen, "Signals and Systems", 2nd Edition, 2008, Wiley India. ISBN9971-51-239-4.

Reference Books:

1. **Michael Roberts,** "Fundamentals of Signals & Systems",2nd edition, Tata McGraw-Hill, 2010, ISBN978-0-07-070221-9.
2. **Alan V Oppenheim, Alan S Willsky and S Hamid Nawab,** "Signals and Systems" Pearson Education Asia / PHI, 2"" edition, 1997. Indian Reprint 2002.
3. **H P Hsu, R Ranjan,** "Signals and Systems", Schaum's outlines, TMH, 2006.
4. **B P Lathi,** "Linear Systems and Signals", Oxford University Press, 2005.
5. **Ganesh Rao and Satish Tunga,** "Signals and Systems", Pearson/Sanguine.
6. **Seymour Lipschutz, Marc Lipson,** "Schaums Easy Outline of Linear Algebra", 2020.

Web links and Video Lectures (e-Resources):

Video lectures on Signals and Systems by Alan V Oppenheim

Lecture 1, Introduction | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube

Lecture 2, Signals and Systems: Part 1 | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube

NPTEL video lectures signals and system:

https://www.youtube.com/watch?v=7Z3LE5uM-6Y&list=PLbMVogVj5nJQQZbah2uRZIRZ_9kfoqZyx

Video lectures on Linear Algebra by Gilbert Strang

https://www.youtube.com/watch?v=ZK3O402wf1c&list=PL49CF3715CB9EF31D&index=1

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

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VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

III Semester

Analog Electronic Circuits			
Course Code	21EC34	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives: This course will enable students to

- Explain various BJT parameters, connections and configurations.
- Design and demonstrate the diode circuits and transistor amplifiers.
- Explain various types of FET biasing and demonstrate the use of FET amplifiers.
- Analyze Power amplifier circuits in different modes of operation.
- Construct Feedback and Oscillator circuits using FET.

Teaching-Learning Process (General Instructions)
These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

BJT Biasing: Biasing in BJT amplifier circuits: The Classical Discrete circuit bias (Voltage-divider bias), Biasing using a collector to base feedback resistor.

Small signal operation and Models: Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain, Separating the signal and the DC quantities, The hybrid Π model, The T model.

MOSFETs: Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor.

Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model.

[Text 1: 3.5(3.5.1, 3.5.3), 3.6(3.6.1 to 3.6.7), 4.5(4.5.1, 4.5.2, 4.5.3), 4.6(4.6.1 to 4.6.7)]

Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Basic BJT Amplifier Configurations- Design of Common Emitter and Common collector amplifier circuits. **RBT Level:** L1, L2, L3

Module-2

MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance RS, Source follower.

MOSFET internal capacitances and High frequency model: The gate capacitive effect, Junction capacitances, High frequency model.

Frequency response of the CS amplifier: The three frequency bands, high frequency response, Low frequency response.

Oscillators: FET based Phase shift oscillator, LC and Crystal Oscillators (no derivation) [Text 1: 4.7(4.7.1 to 4.7.4, 4.7.6) 4.8(4.8.1, 4.8.2, 4.8.3), 4.9, 12.2.2, 12.3.1, 12,3,2]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Discrete Circuit MOS Amplifier – The common source amplifier and the source follower. **RBT Level:** L1, L2, L3
Module-3	
Feedback Amplifier: General feedback structure, Properties of negative feedback, The Four Basic Feedback Topologies, The series-shunt, series-series, shunt-shunt and shunt-series amplifiers (Qualitative Analysis). **Output Stages and Power Amplifiers:** Introduction, Classification of output stages, Class A output stage, Class B output stage: Transfer Characteristics, Power Dissipation, Power Conversion efficiency, Class AB output stage, Class C tuned Amplifier. [Text 1: 7.1, 7.2, 7.3, 7.4.1, 7.5.1, 7.6 (7.6.1 to 7.6.3), 13.1, 13.2, 13.3(13.3.1, 13.3.2, 13.3.3, 13.4, 13.7)]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Class D power amplifier. **RBT Level:** L1, L2, L3
Module-4	
Op-Amp Circuits: Op-amp DC and AC Amplifiers, DAC - Weighted resistor and R-2R ladder, ADC-Successive approximation type, Small Signal half wave rectifier, Absolute value output circuit, Active Filters, First and second order low-pass and high-pass Butterworth filters, Band-pass filters, Band reject filters. **555 Timer and its applications:** Monostable and Astable Multivibrators. [Text 2: 6.2, 8.11(8.11.1a, 8.11.1b), 8.11.2a, 8.12.2,8.13 7.2, 7.3, 7.4, 7.5, 7.6, 7.8, 7.9, 9.4.1, 9.4.1(a), 9.4.3, 9.4.3(a)]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Clippers and Clampers, Peak detector, Sample and hold circuit. **RBT Level:** L1, L2, L3
Module-5	
Overview of Power Electronic Systems: Power Electronic Systems, Power Electronic Converters and Applications. **Thyristors:** Static Anode-Cathode characteristics and Gate characteristics of SCR, Turn-ON methods, Turn-off Mechanism, Turn-OFF Methods: Natural and Forced Commutation – Class A without design consideration. **Gate Trigger Circuit:** Resistance Firing Circuit, Resistance capacitance firing circuit, Unijunction Transistor: Basic operation and UJT Firing Circuit. [Text 3: 1.3, 1.5,1.6, 2.2,2.3,2.4,2.6, 2.7,2.9, 2.10,3.2,3.5.1, 3.5.2, 3.6.1, 3.6.3,3.6.4]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Basic Construction, working and applications of DIAC, TRIAC, IGBT, GTO. **RBT Level:** L1, L2, L3
Course Outcomes (Course Skill Set) At the end of the course the student will be able to : 1. Understand the characteristics of BJTs and FETs for switching and amplifier circuits. 2. Design and analyze FET amplifiers and oscillatorswith different circuit configurations and biasing conditions. 3. Understand the feedback topologies and approximations in the design of amplifiers and oscillators. 4. Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers. 5. Understand the power electronic device components and its functions for basic power electronic circuits.	
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.	

The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject **(duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored out of 100 shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6thEdition, Oxford, 2015.ISBN:978-0-19-808913-1
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4thEdition, Pearson Education, 2018. ISBN: 978-93-325-4991-3
3. **MD Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897'**

Web links and Video Lectures (e-Resources):

- Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015.
- Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.

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III Semester

Analog and Digital Electronics Lab			
Course Code	21ECL35	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Understand the electronic circuit schematic and its working
- Realize and test amplifier and oscillator circuits for the given specifications
- Realize the opamp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers.
- Study the static characteristics of SCR and test the RC triggering circuit.
- Design and test the combinational and sequential logic circuits for their functionalities.
- Use the suitable ICs based on the specifications and functions.

Sl.No.	Experiments
1	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.
2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator and iii) RC Phase shift oscillator
3	Design and set up the circuits using opamp: i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator
4	Obtain the static characteristics of SCR and test SCR Controlled HWR and FWR using RC triggering circuit.
5	Design and implement (a) Half Adder & Full Adder using basic gates and NAND gates, (b) Half subtractor & Full subtractor using NAND gates, (c) 4-variable function using IC74151(8:1MUX).
6	Realize (i) Binary to Gray code conversion & vice-versa (IC74139), (ii) BCD to Excess-3 code conversion and vice versa
7	a) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop b) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.
8	Realize a) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop b) Mod-N Counter using IC7490 / 7476 c) Synchronous counter using IC74192

9	Design 4-bit R – 2R Op-Amp Digital to Analog Converter (i) for a 4-bit binary input using toggle switches (ii) by generating digital inputs using mod-16
10	Pseudorandom sequence generator using IC7495
11	Test the precision rectifiers using opamp: i) Half wave rectifier ii) Full wave rectifier
12	Design and test Monostable and Astable Multivibrator using 555 Timer

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Design and analyze the BJT/FET amplifier and oscillator circuits.
2. Design and test Opamp circuits to realize the mathematical computations, DAC and precision rectifiers.
3. Design and test the combinational logic circuits for the given specifications.
4. Test the sequential logic circuits for the given functionality.
5. Demonstrate the basic electronic circuit experiments using SCR and 555 timer.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Fundamentals of Electronic Devices and Circuits Lab Manual, David A Bell, 5th Edition, 2009, Oxford University Press.
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018. ISBN: 978-93-325-4991-3.
3. Fundamentals of Logic Design, Charles H Roth Jr., Larry L Kinney, Cengage Learning, 7th Edition.

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III Semester

LD (Logic Design) Lab using Pspice / MultiSIM			
Course Code	**21EC381**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- Impart the concepts of De Morgan's Theorem, SOP, POS forms.
- Impart the concepts of designing and analyzing combinational logic circuits.
- Impart the concepts of analysis of sequential logic circuits.
- Analyze and design any given synchronous sequential circuits.

Sl.No	Experiments
1	Implementation of De Morgan's theorem and SOP/POS expressions using Pspice/Multisim.
2	Implementation of Half Adder, Full Adder, Half Subtractor and Full Subtractor using Pspice/ Multisim.
3	Design and implementation of 4-bit Parallel Adder/ Subtractor using IC 7483 and BCD to Excess-3 code conversion and vice-versa using Pspice/Multisim.
4	Design and implement of IC 7485 5-bit magnitude comparator using Pspice/Multisim.
5	To Realize Adder & Subtractor using IC 74153 (4:1 MUX) and 4-variable function using IC74151 (8:1MUX) using Pspice/Multisim.
6	To realize Adder and Subtractor using IC 74139/ 74155N (Demux/Decoder) and Binary to Gray code conversion & vice versa using 74139/ 74155N using Pspice/Multisim.
7	SR, Master-Slave JK, D & T flip-flops using NAND Gates using Pspice/Multisim.
8	Design and realize the Synchronous counters (up/down decade/binary) using Pspice/Multisim.
9	Realize the shift registers and their modes (SISO, PISO, PIPO, SIPO) using 7474/7495 using Pspice/Multisim.
10	Design Pseudo Random Sequence generator using 7495 using Pspice/Multisim.
11	Design Serial Adder with Accumulator and simulate using Pspice/Multisim.
12	Design using Pspice/Multisim Mod-N Counters.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Demonstrate the truth table of various expressions and combinational circuits using logic gates.
2. Design various combinational circuits such as adders, subtractors, comparators, multiplexers and code converters.
3. Construct flips-flops, counters and shift registers.
4. Design and implement synchronous counters.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall

be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

- Digital Logic Applications and Design by John M Yarbrough, Thomson Learning, 2001
- Digital Principles and Design by Donald D Givone, McGraw Hill, 2002.

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02.10.2022

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III Semester

AEC (Analog Electronic Circuits) Lab			
Course Code	21EC382	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	2

Course objectives:

- To provide practical exposure to the students on designing, setting up, executing and debugging various electronic circuits using simulation software.
- To give the knowledge and practical exposure on simple applications of analog electronic circuits.

Sl.No	Experiments using Pspice/MultiSIM software
1	Experiments to realize diode clipping (single, double ended) circuits.
2	Experiments to realize diode clamping (positive, negative) circuits.
3	Experiments to realize Full wave rectifier without filter (and set-up to measure the ripple factor, Vp-p, Vrms, etc.).
4	Design and conduct an experiment on Series Voltage Regulator using Zener diode to determine line/load regulation characteristics.
5	Realize BJT Darlington Emitter follower without bootstrapping and determine the gain, input and output impedances (other configurations of emitter follower can also be considered).
6	Set-up and study the working of complementary symmetry class B push pull power amplifier (other power amplifiers can also be suitably considered) and calculate the efficiency.
7	Design and set-up the oscillator circuits (Hartley, Colpitts, etc. using BJT/FET) and determine the frequency of oscillation.
8	Design and set-up the crystal oscillator and determine the frequency of oscillation.
9	Experiment to realize Input and Output characteristics of BJT Common emitter configuration and evaluation of parameters.
10	Experiments to realize Transfer and drain characteristics of a MOSFET.
11	Experiments to realize UJT triggering circuit for Controlled Full wave Rectifier.
12	Design and simulation of Regulated power supply.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Understand the circuit schematic and its working.
2. Study the characteristics of different electronic devices.
3. Design and test simple electronic circuits as per the specifications using discrete electronic components.
4. Compute the parameters from the characteristics of active devices.
5. Familiarize with EDA software which can be used for electronic circuit simulation.

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Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours.

Rubrics suggested in Annexure-II of Regulation book.

Suggested Learning Resources:

1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual, 5th Edition, 2009, Oxford University Press.
2. Muhammed H Rashid, "Introduction to PSpice using OrCAD for circuits and electronics", 3rd Edition, Prentice Hall, 2003.

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III Semester

LIC (Linear Integrated Circuits) Lab using Pspice / MultiSIM			
Course Code	21EC383	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- To apply operational amplifiers in linear and nonlinear applications.
- To acquire the basic knowledge of special function ICs.
- To use Multisim/Pspice software for circuit design and simulation

Sl.No	Experiments using Pspice / MultiSIM Every experiment has to be designed, circuit to be drawn / constructed and executed in the specified software. Results are also to be noted and inferred.
	Note: Standard design procedure to be adopted.
1	To realize using op-amp an Inverting Amplifier and Non-Inverting Amplifier
2	To realize using op-amps i) Summing Amplifier ii)Difference amplifier
3	To realize using op-amps an Instrumentation Amplifier
4	To realize using op-amps i) Differentiator ii)Integrator
5	To realize using op-amps a Full wave Precision Rectifier
6	To realize using op-amps • Inverting and Non-Inverting Zero Crossing Detectors • Positive and Negative Voltage level detectors
7	To realize using op-amp an Inverting Schmitt Trigger
8	To realize using op-amp an Astable Multivibrator
9	To design and implement using op-amps • Butterworth I & II order Low Pass Filter • Butterworth I & II order High Pass Filter
10	To design and implement using op-amp a RC Phase Shift Oscillator
11	To design and implement Mono-stable Multivibrator using 555 timer
12	To design and implement 4 - bit R-2R Digital to Analog Converter

Course outcomes (Course Skill Set):

After studying this course, students will be able to;

1. Sketch/draw circuit schematics, construct circuits, analyze and troubleshoot circuits containing op-amps, resistors, diodes, capacitors and independent sources.
2. Relate to the manufacturer's data sheets of IC 555 timer and IC μa741 op-amp.
3. Realize and verify the operation of analog integrated circuits like Amplifiers, Precision Rectifiers, Comparators and Waveform generators.
4. Design and implement analog integrated circuits like Oscillators, Active filters, Timer circuits, Data converters and compare the experimental results with theoretical values.

H.O.D.
Dept. of Electronics & Communicat...
Alva's Institute of Engg. & Technology
Mijar, Moodbidri-574 225

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VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

III Semester

LabVIEW Programming Basics			
Course Code	21EC384	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- Aware of various front panel controls and indicators.
- Connect and manipulate nodes and wires in the block diagram.
- Locate various toolbars and pull-down menus for the purpose of implementing specific functions.
- Locate and utilize the context help window.
- Familiar with LabVIEW and different applications using it.
- Run a Virtual Instrument (VI).

Sl.No	VI Programs (using LabVIEW software) to realize the following:
1	Basic arithmetic operations: addition, subtraction, multiplication and division
2	Boolean operations: AND, OR, XOR, NOT and NAND
3	Sum of 'n' numbers using 'for' loop
4	Factorial of a given number using 'for' loop
5	Determine square of a given number
6	Factorial of a given number using 'while 'loop
7	Sorting even numbers using 'while' loop in an array
8	Finding the array maximum and array minimum
	Demonstration Experiments (For CIE)
9	Build a Virtual Instrument that simulates a heating and cooling system. The system must be able to be controlled manually or automatically.
10	Build a Virtual Instrument that simulates a Basic Calculator (using formula node).
11	Build a Virtual Instrument that simulates a Water Level Detector.
12	Demonstrate how to create a basic VI which calculates the area and perimeter of a circle.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Use Lab VIEW to create data acquisition, analysis and display operations
2. Create user interfaces with charts, graph and buttons
3. Use the programming structures and data types that exist in Lab VIEW
4. Use various editing and debugging techniques

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course.

The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Virtual Instrumentation using LABVIEW, Jovitha Jerome, PHI, 2011
2. Virtual Instrumentation using LABVIEW, Sanjay Gupta, Joseph John, TMH, McGraw Hill, Second Edition, 2011.

H.O.D.
Dept. Of Electronics & Communication
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225