SEMESTER – VII
COMPUTER NETWORKS

Course Code	: 18EC71	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs/module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand the layering architecture of OSI reference model and TCP/IP protocol suite.
- Understand the protocols associated with each layer.
- Learn the different networking architectures and their representations.
- Learn the functions and services associated with each layer.

Module-1

Introduction: Data communication: Components, Data representation, Data flow, Networks: Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet.

(1.1,1.2, 1.3(1.3.1to 1.3.4 of Text)

Network Models: Protocol Layering: Scenarios, Principles, Logical Connections, TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP.

(2.1, 2.2, 2.3 of Text) **L1, L2**

Module-2

Data-Link Layer: Introduction: Nodes and Links, Services, Two Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services: Framing, Flow and Error Control, Data Link Layer Protocols: Simple Protocol, Stop and Wait protocol, Piggybacking.

(9.1, 9.2(9.2.1, 9.2.2), 11.1, 11.2of Text)

Media Access Control: Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA.**(12.1 of Text)**

Wired and Wireless LANs: Ethernet Protocol, Standard Ethernet. Introduction to wireless LAN: Architectural Comparison, Characteristics, Access Control.

(13.1, 13.2(13.2.1 to 13.2.5), 15.1 of Text) **L1,L2, L3**

Module-3

Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution, Forwarding of IP Packets: Based on destination Address and Label.

(18.1, 18.2, 18.4, 18.5.1, 18.5.2 of Text)

Network Layer Protocols: Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams. **(19.1of Text).**

Unicast Routing: Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing.

(20.1, 20.2of Text) L1,L2, L3

Module-4

Transport Layer: Introduction: Transport Layer Services, Connectionless and Connection oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-Back-N Protocol, Selective repeat protocol. **(23.1, 23.2.1, 23.2.2, 23.2.3, 23.2.4 of Text)**

Transport-Layer Protocols in the Internet:

User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Flow control, Error control, TCP congestion control.

(24.2, 24.3.1, 24.3.2, 24.3.3, 24.3.4, 24.3.5, 24.3.6, 24.3.7, 24.3.8, 24.3.9 of Text) L1,L2, L3

Module-5

Application Layer: Introduction: providing services, Application- layer paradigms, Standard Client –Server Protocols: World wide web, Hyper Text Transfer Protocol, FTP: Two connections, Control Connection, Data Connection, Electronic Mail: Architecture, Wed Based Mail, Telnet: Local versus remote logging.Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS, security of DNS.

(25.1, 26.1, 26.2, 26.3, 26.4, 26.6 of Text) L1, L2

Course Outcomes: At the end of the course, the students will be able to:

1. Understand the concepts of networking.
2. Describe the various networking architectures.
3. Identify the protocols and services of different layers.
4. Distinguish the basic network configurations and standards associated with each network.
5. Analyze a simple network and measure its parameters.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOK:

- Behrouz A Forouzan, "Data Communications and Networking", 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.

REFERENCE BOOKS:

1. James J Kurose, Keith W Ross, "Computer Networks", Pearson Education.
2. Wayne Tomasi, "Introduction to Data Communication and Networking", Pearson Education.
3. Andrew S Tanenbaum, "Computer Networks", Prentice Hall.
4. William Stallings, "Data and Computer Communications", Prentice Hall.

VLSI DESIGN

Course Code	: 18EC72	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40(08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: The objectives of the course is to enable students to:

- Impart knowledge of MOS transistor theory and CMOS technologies
- Learn the operation principles and analysis of inverter circuits.
- Design Combinational, sequential and dynamic logic circuits as per the requirements
- Infer the operation of Semiconductors Memory circuits.
- Demonstrate the concepts of CMOS testing

Module-1

Introduction: A Brief History, MOS Transistors, CMOS Logic **(1.1 to 1.4 of TEXT2)**

MOS Transistor Theory: Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics **(2.1, 2.2, 2.4 and 2.5 of TEXT2).**, **L1, L2**

Module-2

Fabrication: CMOS Fabrication and Layout, VLSI Design Flow, Introduction, CMOS Technologies, Layout Design Rules, **(1.5 and 3.1 to 3.3 of TEXT2).**

MOSFET Scaling and Small-Geometry Effects, MOSFET Capacitances **(3.5 to 3.6 of TEXT1),** **L1, L2,**

Module-3

Delay: Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths **(4.1 to 4.5 of TEXT2, except sub-sections 4.3.7, 4.4.5, 4.4.6, 4.5.5 and 4.5.6).**

Combinational Circuit Design: Introduction, Circuit families **(9.1 to 9.2 of TEXT2, except subsection 9.2.4).**, **L1, L2, L3**

Module-4

Sequential Circuit Design: Introduction, Circuit Design for Latches and Flip-Flops **(10.1 and 10.3.1 to 10.3.4 of TEXT2)**

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques **(9.1, 9.2, 9.4 to 9.5 of TEXT1)**, **L1, L2, L3**

Module-5

Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM),
(10.1 to 10.3 of TEXT1)
Testing and Verification: Introduction, Logic Verification Principles, Manufacturing Test Principles, Design for testability
(15.1, 15.3, 15.5 15.6.1 to 15.6.3 of TEXT 2). L1, L2

Course outcomes: At the end of the course, the students will be able to:

1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
2. Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
3. Demonstrate ability to design Combinational, sequential and dynamic logic circuits as per the requirements
4. Interpret Memory elements along with timing considerations
5. Interpret testing and testability issues in VLSI Design

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOKS:

1. "CMOS Digital Integrated Circuits: Analysis and Design" - **Sung Mo Kang & Yosuf Leblebici,** Third Edition, Tata McGraw-Hill.
2. **"CMOS VLSI Design- A Circuits and Systems Perspective"-** Neil H. E. Weste and David Money Harris, 4th Edition, Pearson Education.

REFERENCE BOOKS:

1. Adel Sedra and K. C. Smith, "Microelectronics Circuits Theory and Applications", 6th or 7th Edition, Oxford University Press, International Version, 2009.
2. Douglas A Pucknell & Kamran Eshragian, "Basic VLSI Design", PHI 3rd Edition, (original Edition – 1994).
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.

REAL TIME SYSTEM

Course Code	: 18EC731	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This Course will enable students to:

- Understand the fundamentals of Real-time systems and its classifications.
- Describe the concepts of computer control and hardware components for Real-Time Application.
- Discuss the languages to develop software for Real-Time Applications.
- Explain the concepts of operating system and RTS development methodologies.

Module-1

Introduction to Real-Time Systems: Historical background, Elements of a Computer Control System, RTS- Definition, Classification of Real-time Systems, Time Constraints, Classification of Programs.

Concepts of Computer Control: Introduction, Sequence Control, Loop Control, Supervisory Control, Centralized Computer Control, Hierarchical Systems.

(Text: 1.1 to 1.6 and 2.1 to 2.6), L1, L2

Module-2

Computer Hardware Requirements for Real-Time Applications: Introduction, General Purpose Computer, Single Chip Microcomputers and Microcontrollers, Specialized Processors, Process-Related Interfaces, Data Transfer Techniques, Communications, Standard Interface.

(Text: 3.1 to 3.8). L1, L2

Module-3

Languages for Real-Time Applications: Introduction, Syntax Layout and Readability, Declaration and Initialization of Variables and Constants, Cutlass, Modularity and Variables, Compilation of Modular Programs, Data types, Control Structures, Exception Handling, Low-level facilities, Co-routines, Interrupts and Device Handling, Concurrency, Real-Time Support, Overview of Real-Time Languages.

(Text: 5.1 to 5.14)., L1,L2, L3

Module-4

Operating Systems: Introduction, Real-Time Multi-Tasking OS, Scheduling Strategies, Priority Structures, Task Management, Scheduler and Real-Time

Clock Interrupt Handler, Memory Management, Code Sharing, Resource Control, Task Co-Operation and Communication, Mutual Exclusion.
(Text: 6.1 to 6.11). **L1, L2**

Module-5

Design of RTS – General Introduction: Introduction, Specification Document, Preliminary Design, Single-Program Approach, Foreground/Background System.
RTS Development Methodologies: Introduction, Yourdon Methodology, Ward and Mellor Method, Hately and Pirbhai Method.
(Text: 7.1 to 7.5 and 8.1, 8.2, 8.4,8.5). **L1, L2, L3**

Course Outcomes: At the end of the course, students should be able to:

1. Explain the fundamentals of Real time systems and its classifications.
2. Understand the concepts of computer control and the suitable computer hardware requirements for real-time applications.
3. Describe the operating system concepts and techniques required for real time systems.
4. Develop the software algorithms using suitable languages to meet Real time applications.
5. Apply suitable methodologies to design and develop Real-Time Systems.

Text Book:

- Real-Time Computer Control, Stuart Bennet, 2nd Edn. Pearson Education. 2008.

Reference Books:

1. "Real –Time Systems", C.M. Krishna, Kang G. Shin, McGraw –Hill International Editions, 1997.
2. Real-Time Systems Design and Analysis, Phillip. A. Laplante, second edition, PHI, 2005.
3. Embedded Systems, Raj Kamal, Tata McGraw Hill, India, third edition, 2005.

SATELLITE COMMUNICATION

Course Code	: 18EC732	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to

- Understand the basic principle of satellite orbits and trajectories.
- Study of electronic systems associated with a satellite and the earth station.
- Understand the various technologies associated with the satellite communication.
- Focus on a communication satellite and the national satellite system.
- Study of satellite applications focusing various domains services such as remote sensing, weather forecasting and navigation.

Module-1

Satellite Orbits and Trajectories: Definition, Basic Principles, Orbital parameters, Injection velocity and satellite trajectory, Types of Satellite orbits, Orbital perturbations, Satellite stabilization, Orbital effects on satellite's performance, Eclipses, Look angles: Azimuth angle, Elevation angle. ,

L1, L2

Module-2

Satellite subsystem: Power supply subsystem, Attitude and Orbit control, Tracking, Telemetry and command subsystem, Payload.

Earth Station: Types of earth station, Architecture, Design considerations, Testing, Earth station Hardware, Satellite tracking.,

L1, L2

Module-3

Multiple Access Techniques: Introduction, FDMA (No derivation), SCPC Systems, MCPC Systems, TDMA, CDMA, SDMA.

Satellite Link Design Fundamentals: Transmission Equation, Satellite Link Parameters, Propagation considerations

L1,L2, L3

Module-4

Communication Satellites: Introduction, Related Applications, Frequency Bands, Payloads, Satellite Vs. Terrestrial Networks, Satellite Telephony, Satellite Television, Satellite radio, Regional satellite Systems, National Satellite Systems.

L1, L2

Module-5

Remote Sensing Satellites: Classification of remote sensing systems, orbits, Payloads, Types of images: Image Classification, Interpretation, Applications.
Weather Forecasting Satellites: Fundamentals, Images, Orbits, Payloads, Applications.
Navigation Satellites: Development of Satellite Navigation Systems, GPS system, Applications.,

L1,L2, L3

Course Outcomes: At the end of the course, the students will be able to:

1. Describe the satellite orbits and its trajectories with the definitions of parameters associated with it.
2. Describe the electronic hardware systems associated with the satellite subsystem and earth station.
3. Describe the communication satellites with the focus on national satellite system.
4. Compute the satellite link parameters under various propagation conditions with the illustration of multiple access techniques.
5. Describe the satellites used for applications in remote sensing, weather forecasting and navigation.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- Anil K. Maini, Varsha Agrawal, Satellite Communications, Wiley India Pvt. Ltd., 2015, ISBN: 978-81-265-2071-8.

Reference Books :

1. Dennis Roddy, Satellite Communications, 4th Edition, McGraw- Hill International edition, 2006
2. Timothy Pratt, Charles Bostian, Jeremy Allnutt, Satellite Communications, 2nd Edition, Wiley India Pvt. Ltd , 2017, ISBN: 978-81-265-0833-4

DIGITAL IMAGE PROCESSING

Course Code	: 18EC733	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to

- Understand the fundamentals of digital image processing.
- Understand the image transforms used in digital image processing.
- Understand the image enhancement techniques used in digital image processing.
- Understand the image restoration techniques and methods used in digital image processing.
- Understand the Morphological Operations used in digital image processing.

Module1

Digital Image Fundamentals: Whatis Digital Image Processing?, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition.

(Text: Chapter 1 and Chapter 2: Sections 2.1 to 2.2, 2.6.2) L1,L2

Module-2

Image Enhancement in the Spatial Domain: Image Sampling and Quantization, Some Basic Relationships Between Pixels, Linear and Nonlinear Operations. Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters

(Text:Chapter2: Sections 2.3 to 2.62, Chapter3: Sections3.2 to 3.6), L1,L2

Module-3

Frequency Domain: Preliminary Concepts, The Discrete Fourier Transform (DFT) of Two Variables, Properties of the 2-DDFT, Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters, Selective Filtering.

(Text: Chapter4: Sections 4.2, 4.5 to 4.10), L1,L2

Module-4

Restoration: Noise models, Restorationin the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Linear, Position-Invariant degradations Estimating the Degradation Function, Inverse Filtering, Minimum

Mean Square Error(Wiener) Filtering, Constrained Least Squares Filtering.
(Text: Chapter 5: Sections 5.2, to 5.9) **L1,L2**

Module-5

Morphological Image Processing: Preliminaries, Erosion and Dilation, Opening and Closing.

Image Processing: Color Fundamentals, Color Models, Pseudo color Image Processing.

(Text: Chapter 6: Sections 6.1 to 6.3 Chapter 9: Sections9.1to9.3)

L1,L2

Course Outcomes: At the end of the course, students should be able to:

1. Describe the fundamentals of digital image processing.
2. Understand image formation and the role human visual system plays in perception of gray and color image data.
3. Apply image processing techniques in both the spatial and frequency (Fourier) domains.
4. Design and evaluate image analysis techniques
5. Conduct independent study and analysis of Image Enhancement and restoration techniques.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- Digital Image Processing- Rafel C Gonzalez and Richard E. Woods, PHI 3rd Edition 2010.

Reference Books:

1. Digital Image Processing- S. Jayaraman, S. Esakkirajan,T. Veerakumar, Tata Mc Graw Hill 2014.
2. Fundamentals of Digital Image Processing- A. K. Jain, Pearson 2004.
3. Image Processing analysis and Machine vision with Mind Tap by Milan Sonka and Roger Boile, Cengage Publications, 2018.

DSP ALGORITHMS and ARCHITECTURE

Course Code	: 18EC734	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Figure out the knowledge and concepts of digital signal processing techniques.
- Understand the computational building blocks of DSP processors and its speed issues.
- Understand the various addressing modes, peripherals, interrupts and pipelining structure of TMS320C54xx processor.
- Learn how to interface the external devices to TMS320C54xx processor in various modes.
- Understand basic DSP algorithms with their implementation.

Module -1

Introduction to Digital Signal Processing:

Introduction, A Digital Signal – Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation.

Computational Accuracy in DSP Implementations:

Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementation.

L1,L2

Module -2

Architectures for Programmable Digital Signal – Processing Devices:

Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.

L1,L2

Module -3

Programmable Digital Signal Processors:

Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54XX, Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and

Programming, On – Chip Peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor.

L1,L2

Module -4

Implementation of Basic DSP Algorithms:

Introduction, The Q – notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case).

Implementation of FFT Algorithms:

Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit – Reversed Index. Generation & Implementation on the TMS32OC54xx.

L1,L2

Module -5

Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices:

Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA).

Interfacing and Applications of DSP Processors:

Introduction, Synchronous Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System.

L1,L2

Course Outcomes: At the end of this course, students would be able to:

1. Comprehend the knowledge and concepts of digital signal processing techniques.
2. Apply the knowledge of DSP computational building blocks to achieve speed in DSP architecture or processor.
3. Apply knowledge of various types of addressing modes, interrupts, peripherals and pipelining structure of TMS320C54xx processor.
4. Develop basic DSP algorithms using DSP processors.
5. Discuss about synchronous serial interface and multichannel buffered serial port (McBSP) of DSP device and demonstrate the programming of CODEC interfacing.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.

- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- "Digital Signal Processing", Avatar Singh and S. Srinivasan, Thomson Learning, 2004.

Reference Books:

1. "Digital Signal Processing: A practical approach", Ifeachor E. C., Jervis B. W Pearson-Education, PHI, 2002.
2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2nd, 2010
3. "Architectures for Digital Signal Processing", Peter Pirsch John Wiley, 2008

IoT & WIRELESS SENSOR NETWORKS

Course Code	: 18EC741	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Describe the OSI Model for IoT/M2M Systems.
- Understand the architecture and design principles for device supporting IoT.
- Develop competence in programming for IoT Applications.
- Identify the uplink and downlink communication protocols which best suits the specific application of IoT / WSNs.

Module-1

Overview of Internet of Things: IoT Conceptual Framework, IoT Architectural View, Technology Behind IoT, Sources of IoT,M2M communication, Examples of IoT. Modified OSI Model for the IoT/M2M Systems, data enrichment, data consolidation and device management at IoT/M2M Gateway, web communication protocols used by connected IoT/M2M devices, Message communication protocols (CoAP-SMS, CoAP-MQ, MQTT,XMPP) for IoT/M2M devices. – Refer Chapter 1, 2 and 3 of Text 1.

L1, L2

Module-2

Architecture and Design Principles for IoT: Internet connectivity, Internet-based communication,IPv4, IPv6,6LoWPAN protocol, IP Addressing in the IoT, Application layer protocols: HTTP, HTTPS,FTP,TELNET and ports.

Data Collection, Storage and Computing using a Cloud Platform: Introduction, Cloud computing paradigm for data collection, storage and computing, Cloud service models, IoT Cloud- based data collection, storage and computing services using Nimbits. - Refer Chapter 4 and 6 of Text 1.

L1, L2

Module-3

Prototyping and Designing Software for IoT Applications: Introduction, Prototyping Embedded device software, Programming Embedded Device Arduino Platform using IDE, Reading data from sensors and devices, Devices, Gateways, Internet and Web/Cloud services software development.

Programming MQTT clients and MQTT server. Introduction to IoT privacy

and security. Vulnerabilities, security requirements and threat analysis, IoT Security Tomography and layered attacker model. - Refer Chapter 9 and 10 of Text 1. **L1, L2, L3**

Module-4

Overview of Wireless Sensor Networks:

Challenges for Wireless Sensor Networks, Enabling Technologies for Wireless Sensor Networks.

Architectures: Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes, Operating Systems and Execution Environments, Network Architecture-Sensor Network Scenarios, Optimization Goals and Figures of Merit, Design principles for WSNs, Service interfaces of WSNs Gateway Concepts. - Refer Chapter 1, 2, 3 of Text 2.

L1, L2, L3

Module-5

Communication Protocols:

Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Contention based protocols(CSMA,PAMAS), Schedule based protocols (LEACH, SMACS, TRAMA) Address and Name Management in WSNs, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing, Hierarchical networks by clustering. - Refer Chapter 4, 5, 7 and 11 of Text 2.

L1, L2, L3

Course Outcomes: At the end of the course, students will be able to:

1. Understand choice and application of IoT & M2M communication protocols.
2. Describe Cloud computing and design principles of IoT.
3. Relate to MQTT clients, MQTT server and its programming.
4. Describe the architectures and its communication protocols of WSNs.
5. Identify the uplink and downlink communication protocols associated with specific application of IOT / WSNs

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4sub questions.
- There will be 2 full questions from each module covering all the topics of the module.

- Students will have to answer 5full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Raj Kamal, "Internet of Things-Architecture and design principles", McGraw Hill Education.
2. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless Sensor Networks", John Wiley, 2005.

Reference Books:

1. Feng Zhao & Leonidas J. Guibas, "Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
2. Kazem Sohraby, Daniel Minoli, & Taieb Znati, "Wireless Sensor Networks- Technology, Protocols and Applications", John Wiley, 2007.
3. Anna Hac, "Wireless Sensor Network Designs", John Wiley, 2003.

AUTOMOTIVE ELECTRONICS

Course Code	: 18EC742	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand the basics of automobile dynamics and design electronics to complement those features.
- Design and implement the electronics that attribute the reliability, safety, and smartness to the automobiles, providing add-on comforts.

Module -1

Automotive Fundamentals Overview – Evolution of Automotive Electronics, Automobile Physical Configuration, Survey of Major Automotive Systems, The Engine – Engine Block, Cylinder Head, Four Stroke Cycle, Engine Control, Ignition System - Spark plug, High voltage circuit and distribution, Spark pulse generation, Ignition Timing, Diesel Engine, Drive Train - Transmission, Drive Shaft, Differential, Suspension, Brakes, Steering System (Text 1: Chapter1), Starter Battery –Operating principle:
(Text 2: Pg. 407-410)

The Basics of Electronic Engine Control – Motivation for Electronic Engine Control – Exhaust Emissions, Fuel Economy, Concept of an Electronic Engine control system, Definition of General terms, Definition of Engine performance terms, Engine mapping, Effect of Air/Fuel ratio, spark timing and EGR on performance, Control Strategy, Electronic Fuel control system, Analysis of intake manifold pressure, Electronic Ignition.
(Text 1: Chapter 5) **L1, L2**

Module -2

Automotive Sensors – Automotive Control System applications of Sensors and Actuators – Variables to be measured, Airflow rate sensor, Strain Gauge MAP sensor, Engine Crankshaft Angular Position Sensor, Magnetic Reluctance Position Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Throttle Angle Sensor (TAS), Engine Coolant Temperature (ECT) Sensor, Exhaust Gas Oxygen (O2/EGO) Lambda Sensors, Piezoelectric Knock Sensor. **(Text 1: Chapter 6)**

Automotive Engine Control Actuators – Solenoid, Fuel Injector, EGR Actuator, Ignition System
(Text 1: Chapter 6) **L1, L2**

Module -3

Digital Engine Control Systems – Digital Engine control features, Control modes for fuel Control (Seven Modes), EGR Control, Electronic Ignition Control - Closed loop Ignition timing, Spark Advance Correction Scheme, Integrated Engine Control System - Secondary Air Management, Evaporative Emissions Canister Purge, Automatic System Adjustment, System Diagnostics. **(Text 1: Chapter 7)**

Control Units – Operating conditions, Design, Data processing, Programming, Digital modules in the Control unit, Control unit software.

(Text 2: Pg. 196-207) **L1, L2**

Module -4

Automotive Networking –Bus Systems – Classification, Applications in the vehicle, Coupling of networks, Examples of networked vehicles

(Text 2: Pg. 85-91),

Buses - CAN Bus, LIN Bus, MOST Bus, Bluetooth, Flex Ray, Diagnostic Interfaces. **(Text 2: Pg. 92-151)**

Vehicle Motion Control – Typical Cruise Control System, Digital Cruise Control System, Digital Speed Sensor, Throttle Actuator, Digital Cruise Control configuration, Cruise Control Electronics (Digital only), Antilock Brake System (ABS)

(Text 1: Chapter 8) **L1,L2**

Module -5

Automotive Diagnostics–Timing Light, Engine Analyzer, On-board diagnostics, Off-board diagnostics, Expert Systems, Occupant Protection Systems – Accelerometer based Air Bag systems. **(Text 1: Chapter 10)**

Future Automotive Electronic Systems – Alternative Fuel Engines, Electric and Hybrid vehicles, Fuel cell powered cars, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Heads Up display, Speech Synthesis, Navigation – Navigation Sensors - Radio Navigation, Signpost navigation, dead reckoning navigation, Voice Recognition Cell Phone dialing, Advanced Cruise Control, Stability Augmentation, Automatic driving Control

(Text 1: Chapter 11) **L1, L2,L3**

Course Outcomes: At the end of the course, students will be able to:

1. Describe the basics of automobile dynamics and design electronics.
2. Acquire an overview of automotive components, subsystems, and basics of Electronic Engine Control in today's automotive industry.
3. Use available automotive sensors and actuators while interfacing with microcontrollers / microprocessors during automotive system design.

4. Understand the networking of various modules in automotive systems, communication protocols and diagnostics of the sub systems.
5. Design and implement the electronics that attribute the reliability, safety, and smartness to the automobiles, providing add-on comforts and get fair idea on future Automotive Electronic Systems.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. William B. Ribbens, "Understanding Automotive Electronics", 6th Edition, Elsevier Publishing.
2. Robert Bosch GmbH (Ed.) Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive, 5th edition, John Wiley & Sons Inc., 2007.

MULTIMEDIA COMMUNICATION

Course Code	: 18EC743	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand the importance of multimedia in today's online and offline information sources and repositories.
- Understand the how Text, Audio, Image and Video information can be represented digitally in a computer so that it can be processed, transmitted and stored efficiently.
- Understand the Multimedia Transport in Wireless Networks
- Understand the Real-time multimedia network applications.
- Understand the Different network layer based application.

Module -1

Multimedia Communications: Introduction, Multimedia information representation, multimedia networks, multimedia applications, Application and networking terminology.

(Chapter 1 of Text 1) **L1,L2**

Module -2

Information Representation: Introduction, Digitization principles, Text, Images, Audio and Video.

(Chapter 2 of Text 1) **L1,L2**

Module -3

Text and Image Compression: Introduction, Compression principles, text compression, image Compression.**(Chapter 3 of Text 1)**

Distributed Multimedia Systems: Introduction, main Features of a DMS, Resource management of DMS, Networking, Multimedia Operating Systems.

(Chapter 4 - Sections 4.1 to 4.5 of Text 2), **L1,L2**

Module -4

Audio and video compression: Introduction, Audio compression, video compression, video compression principles, video compression.

(Chapter 4 of Text 1) **L1,L2**

Module -5

Multimedia Information Networks: Introduction, LANs, Ethernet, Token ring, Bridges, FDDI High-speed LANs, LAN protocol**(Chap. 8 of Text 1).**
The Internet: Introduction, IP Datagrams, Fragmentation, IPAddress, ARP and RARP, QoS Support, IPv8.
(Chap. 9 of Text 1), **L1,L2**

Course Outcomes: After studying this course, students will be able to:

1. Understand basics of different multimedia networks and applications.
2. Understand different compression techniques to compress audio and video.
3. Describe multimedia Communication across Networks.
4. Analyse different media types to represent them in digital form.
5. Compress different types of text and images using different compression techniques.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Multimedia Communications- Fred Halsall, Pearson Education, 2001, ISBN -9788131709948.
2. Multimedia Communication Systems- K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, Pearson Education, 2004. ISBN - 9788120321458.

Reference Book:

- Multimedia: Computing, Communications and Applications- Raifsteinmetz, Klara Nahrstedt, Pearson Education,2002.ISBN-978817758

CRYPTOGRAPHY

Course Code	: 18EC744	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand the basics of symmetric key and public key cryptography.
- Explain classical cryptography algorithms.
- Acquire knowledge of mathematical concepts required for cryptography.
- Describe pseudo random sequence generation technique.
- Explain symmetric and asymmetric cryptography algorithms.

Module -1

Classical Encryption Techniques: Symmetric cipher model, Substitution techniques, Transposition techniques **(Text 1: Chapter 1)**

Basic Concepts of Number Theory and Finite Fields: Euclidean algorithm, Modular arithmetic

(Text 1: Chapter 3) **L1,L2**

Module -2

SYMMETRIC CIPHERS: Traditional Block Cipher structure, Data encryption standard (DES), The AES Cipher.

(Text 1: Chapter 2: Section1, 2, Chapter 4:Section 2, 3, 4) L1,L2

Module -3

Basic Concepts of Number Theory and Finite Fields: Groups, Rings and Fields, Finite fields of the form GF(p), Prime Numbers, Fermat's and Euler's theorem, discrete logarithm.

(Text 1: Chapter 3 and Chapter 7: Section 1, 2, 5), L1,L2

Module -4

ASYMMETRIC CIPHERS: Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography

(Text 1: Chapter 8, Chapter 9: Section 1, 3, 4) L1,L2,L3

Module -5

Pseudo-Random-Sequence Generators and Stream Ciphers:

Linear Congruential Generators, Linear Feedback Shift Registers, Design and

analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/ KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M,PKZIP **(Text 2: Chapter 16)**, **L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:

1. Explain basic cryptographic algorithms to encrypt and decrypt the data.
2. Use symmetric and asymmetric cryptography algorithms to encrypt and decrypt the information.
3. Describe the mathematics associated with cryptography.
4. Apply concepts of modern algebra in cryptography algorithms.
5. Apply pseudo random sequence in stream cipher algorithms.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. William Stallings , "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X.

Reference Books:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

MACHINE LEARNING WITH PYTHON

Course Code	: 18EC745	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to

- Define machine learning and problems relevant to machine learning.
- Differentiate supervised, unsupervised and reinforcement learning
- Apply neural networks, Bayes classifier and k nearest neighbor, for problems appear in machine learning.
- Perform statistical analysis of machine learning techniques.

Module – 1

Introduction: Well posed learning problems, Designing a Learning system, Perspective and Issues in Machine Learning.

Concept Learning: Concept learning task, Concept learning as search, Find-S algorithm, Version space, Candidate Elimination algorithm, Inductive Bias.

Python libraries suitable for Machine Learning: Numerical Analysis and Data Exploration with NumPy Arrays, and Data Visualization with Matplotlib

Text Book1, Sections: 1.1 – 1.3, 2.1-2.5, 2.7 **L1 - L5**

Module – 2

Decision Tree Learning: Decision tree representation, Appropriate problems for decision tree learning, Basic decision tree learning algorithm, hypothesis space search in decision tree learning, Inductive bias in decision tree learning, Issues in decision tree learning. Example program in Python

Text Book1, Sections: 3.1-3.7 **L1 - L3**

Module – 3

Artificial Neural Networks : Introduction, Neural Network representation, Appropriate problems, Perceptrons, Back propagation algorithm. Example program in Python

Text book 1, Sections: 4.1 – 4.6 **L1 - L3**

Module – 4

Bayesian Learning: Introduction, Bayes theorem, Bayes theorem and concept learning, ML and LS error hypothesis, ML for predicting probabilities, MDL principle, Naive Bayes classifier, Bayesian belief networks, EM algorithm, Example program in Python.

Text book 1, Sections: 6.1 – 6.6, 6.9, 6.11, 6.12 **L1 - L4**

Module – 5

Evaluating Hypothesis: Motivation, Estimating hypothesis accuracy, Basics of sampling theorem, General approach for deriving confidence intervals, Difference in error of two hypothesis, Comparing learning algorithms.
Instance Based Learning: Introduction, k-nearest neighbor learning, locally weighted regression, radial basis function, cased-based reasoning,
Reinforcement Learning: Introduction, Learning Task, Q Learning Example program in Python.
Text book 1, Sections: 5.1-5.6, 8.1-8.5, 13.1-13.3 L1 - L3

Course Outcomes: After studying this course, students will be able to

1. Identify the problems in machine learning.
2. Select supervised, unsupervised or reinforcement learning for problem solving.
3. Apply theory of probability and statistics in machine learning
4. Apply concept learning, ANN, Bayes classifier, k nearest neighbor
5. Perform statistical analysis of machine learning techniques.

Question paper pattern:

- The question paper will have ten questions.
- There will be 2 questions from each module.
- Each question will have questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Tom M. Mitchell, Machine Learning, India Edition 2013, McGraw Hill Education.

Reference Books:

1. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning, 2nd edition, springer series in statistics.
2. Ethem Alpaydýn, Introduction to machine learning, second edition, MIT press.
3. https://www.analyticsvidhya.com/blog/2015/04/comprehensive-guide-data-exploration-sas-using-python-numpy-scipy-matplotlib-pandas/
4. https://www.oreilly.com/library/view/python-for-data/9781491957653/ch01.html

COMPUTER NETWORKS LAB

Course Code : **18ECL76**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:

- Choose suitable tools to model a network and understand the protocols at various OSI reference levels.
- Design a suitable network and simulate using a Network simulator tool.
- Simulate the networking concepts and protocols using C/C++ programming.
- Model the networks for different configurations and analyze the results.

Laboratory Experiments

PART-A: Simulation experiments using NS2/ NS3/ OPNET/ NCTUNS/ NetSim/QualNet or any other equivalent tool

1. Implement a point to point network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.
2. Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent by TCP/UDP.
3. Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.
4. Implement Ethernet LAN using n nodes and assign multiple traffic to the nodes and obtain congestion window for different sources/ destinations.
5. Implement ESS with transmission nodes in Wireless LAN and obtain the performance parameters.
6. Implementation of Link state routing algorithm.

PART-B: Implement the following in C/C++

1. Write a program for a HLDC frame to perform the following.
   i) Bit stuffing
   ii) Character stuffing.
2. Write a program for distance vector algorithm to find suitable path for transmission.
3. Implement Dijkstra's algorithm to compute the shortest routing path.

4. For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify the program for the cases
   a. Without error
   b. With error
5. Implementation of Stop and Wait Protocol and Sliding Window Protocol
6. Write a program for congestion control using leaky bucket algorithm.

Course outcomes: On the completion of this laboratory course, the students will be able to:

1. Choose suitable tools to model a network.
2. Use the network simulator for learning and practice of networking algorithms.
3. Illustrate the operations of network protocols and algorithms using C programming.
4. Simulate the network with different configurations to measure the performance parameters.
5. Implement the data link and routing protocols using C programming.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination one question from software and one question from hardware or only one hardware experiments based on the complexity to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

VLSI LABORATORY

Course Code : **18ECL77**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:

- Design, model, simulate and verify CMOS digital circuits
- Design layouts and perform physical verification of CMOS digital circuits
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist
- Perform RTL-GDSII flow and understand the stages in ASIC design

Experiments can be conducted using any of the following or equivalent design tools: Cadence/Synopsis/Mentor Graphics/Microwind

Laboratory Experiments

Part – A

Analog Design

Use any VLSI design tools to carry out the experiments, use library files and technology files below 180 nm.

1.a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following:

i. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time period of 20ns and plot the input voltage and output voltage of designed inverter?

ii. From the simulation results compute tpHL, tpLH and td for all three geometrical settings of width?

iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter?

1. b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

2. a) Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 1. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.

2. b) Draw layout of NAND with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

3. a) Capture schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measures the Unity Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB.

3. b) Draw layout of common source amplifier, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

4.a) Capture schematic of two-stage operational amplifier and measure the following:

i. UGB
ii. dB bandwidth
iii. Gain margin and phase margin with and without coupling capacitance
iv. Use the op-amp in the inverting and non-inverting configuration and verify its functionality
v. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations.

4.b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in 4.a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

Part - B

Digital Design

Carry out the experiments using semicustom design flow or ASIC design flow, use technology library 180/90/45nm and below

Note: The experiments can also be carried out using FPGA design flow, it is required to set appropriate constraints in FPGA advanced synthesis options

1. Write verilog code for 4-bit up/down asynchronous reset counter and carry out the following:
   a. Verify the functionality using test bench
   b. Synthesize the design by setting area and timing constraint. Obtain

the gate level netlist, find the critical path and maximum frequency of operation. Record the area requirement in terms of number of cells required and properties of each cell in terms of driving strength, power and area requirement.

c. Perform the above for 32-bit up/down counter and identify the critical path, delay of critical path, and maximum frequency of operation, total number of cells required and total area.

2. Write verilog code for 4-bit adder and verify its functionality using test bench. Synthesize the design by setting proper constraints and obtain the net list. From the report generated identify critical path, maximum delay, total number of cells, power requirement and total area required. Change the constraints and obtain optimum synthesis results.
3. Write verilog code for UART and carry out the following:
   a. Perform functional verification using test bench
   b. Synthesize the design targeting suitable library and by setting area and timing constraints
   c. For various constrains set, tabulate the area, power and delay for the synthesized netlist
   d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints
4. Write verilog code for 32-bit ALU supporting four logical and four arithmetic operations, use case statement and if statement for ALU behavioral modeling.
   a. Perform functional verification using test bench
   b. Synthesize the design targeting suitable library by setting area and timing constraints
   c. For various constrains set, tabulate the area, power and delay for the synthesized netlist
   d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints

   Compare the synthesis results of ALU modeled using IF and CASE statements.
5. Write verilog code for Latch and Flip-flop, Synthesize the design and compare the synthesis report (D, SR, JK).
6. For the synthesized netlist carry out the following for any two above experiments:
   a. Floor planning (automatic), identify the placement of pads
   b. Placement and Routing, record the parameters such as no. of layers used for routing, flip method for placement of standard cells, placement of standard cells, routes of power and ground, and routing of standard cells
   c. Physical verification and record the LVS and DRC reports

d. Perform Back annotation and verify the functionality of the design
e. Generate GDSII and record the number of masks and its color composition

Course Outcomes: On the completion of this laboratory course, the students will be able to:

1. Design and simulate combinational and sequential digital circuits using Verilog HDL
2. Understand the Synthesis process of digital circuits using EDA tool.
3. Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list
4. Design and simulate basic CMOS circuits like inverter, common source amplifier and differential amplifiers.
5. Perform RTL-GDSII flow and understand the stages in ASIC design.

COMMUNICATION THEORY

Course Code	: 18EC751	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs / Module)	Exam Hours	: 03
	CREDITS – 03		

Course Learning Objectives: This course will enable students to:

- Describe essential elements of an electronic communications.
- Understand Amplitude, Frequency & Phase modulations, and Amplitude demodulation.
- Explain the basics of sampling and quantization.
- Understand the various digital modulation schemes.
- The concepts of wireless communication.

Module -1

Introduction to Electronic Communications: Historical perspective, Electromagnetic frequency spectrum, signal and its representation, Elements of electronic communications system, primary communication resources, signal transmission concepts, Analog and digital transmission, Modulation, Concept of frequency translation, Signal radiation and propagation
(Text 1: 1.1 to1.10)

L1, L2

Module -2

Noise: Classification and source of noise **(TEXT 1:3.1)**
Amplitude Modulation Techniques: Types of analog modulation, Principle of amplitude modulation, AM power distribution, Limitations of AM,
(TEXT 1: 4.1,4.2, 4.4, 4.6)
Angle Modulation Techniques: Principles of Angle modulation, Theory of FM-basic Concepts, Theory of phase modulation **(TEXT 1: 5.1,5.2, 5.5)**
Analog Transmission and Reception: AM Radio transmitters, AM Radio Receivers
(TEXT 1:6.1,6.2)

L1, L2

Module -3

Sampling Theorem and pulse Modulation Techniques: Digital Versus analog Transmissions, Sampling Theorem, Classification of pulse modulation techniques, PAM, PWM, PPM, PCM, Quantization of signals
(TEXT 1: 7.1 to 7.8)

L1, L2

Module -4

Digital Modulation Techniques: Types of digital Modulation, ASK,FSK,PSK,QPSK

(TEXT 1: 9.1 to 9.5)

Source and Channel Coding: Objective of source coding, source coding technique, Shannon's source coding theorem, need of channel coding, Channel coding theorem, error control and coding

(TEXT 1: 11.1 to 11.3, 11.8, 11.9,11.12)

L1, L2

Module -5

Evolution of wireless communication systems: Brief History of wireless communications, Advantages of wireless communication, disadvantages of wireless communications, wireless network generations, Comparison of wireless systems, Evolution of next-generation networks, Applications of wireless communication

(TEXT 2: 1.1 to 1.7)

Principles of Cellular Communications: Cellular terminology, Cell structure and Cluster, Frequency reuse concept, Cluster size and system capacity, Method of locating cochannel cells, Frequecy reuse distance

(TEXT 2: 4.1 to 4.7)

L1, L2

Course Outcomes: At the end of the course, students will be able:

1. Describe operation of communication systems.
2. Understand the techniques of Amplitude and Angle modulation.
3. Understand the concept of sampling and quantization.
4. Understand the concepts of different digital modulation techniques.
5. Describe the principles of wireless communications system.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Analog and Digital Communications by T L Singal, McGraw Hill Education (India) Private Limited.
2. Wireless Communications by T L Singal, McGraw Hill Education (India) Private Limited.

Reference Books:

1. Modern Digital and Analog Communication Systems B. P. Lathi, Oxford University Press., 4th ed, 2010,
2. Communication Systems: Analog and Digital, R.P.Singh and S.Sapre: TMH 2nd edition, 2007
3. Introduction to Wireless Telecommunications systems and Networks by Gray J Mullett, Cengage learning.

NEURAL NETWORKS

Course Code	: 18EC752	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs / Module)	Exam Hours	: 03
	CREDITS – 03		

Course Learning Objectives: This course will enable students to:

- Understand the basics of ANN and comparison with Human brain.
- Acquire knowledge on Generalization and function approximation of various ANN architectures.
- Understand reinforcement learning using neural networks
- Acquire knowledge of unsupervised learning using neural networks.

Module -1

Introduction: Biological Neuron – Artificial Neural Model -Types of activation functions – **Architecture**: Feedforward and Feedback, Convex Sets, Convex Hull and Linear Separability, Non-Linear Separable Problem. XOR Problem, Multilayer Networks.

Learning: Learning Algorithms, Error correction and Gradient Descent Rules, Learning objective of TLNs, Perceptron Learning Algorithm, Perceptron Convergence Theorem. **L1,L2**

Module -2

Supervised Learning: Perceptron learning and Non Separable sets, α-Least Mean Square Learning, MSE Error surface, Steepest Descent Search, μ-LMS approximate to gradient descent, Application of LMS to Noise Cancelling, Multi-layered Network Architecture, Backpropagation Learning Algorithm, Practical consideration of BP algorithm.

L1,L2,L3

Module -3

Support Vector Machines and Radial Basis Function:

Learning from Examples, Statistical Learning Theory, Support Vector Machines, SVM application to Image Classification, Radial Basis Function Regularization theory, Generalized RBF Networks, Learning in RBFNs, RBF application to face recognition.

Module -4

Attractor Neural Networks: Associative Learning Attractor Associative Memory, Linear Associative memory, Hopfield Network, application of Hopfield

Network, Brain State in a Box neural Network, Simulated Annealing, Boltzmann Machine, Bidirectional Associative Memory.

L1,L2,L3

Module -5

Self -organization Feature Map: Maximal Eigenvector Filtering, Extracting Principal Components, Generalized Learning Laws, Vector Quantization, Self -organization Feature Maps, Application of SOM, Growing Neural Gas.

L1,L2,L3

Course Outcomes: At the end of the course, students should be able to:

1. Describe the basics of ANN and comparison with Human brain.
2. Understand the role of neural networks in engineering, artificial intelligence, and cognitive modelling.
3. Understand the concepts and techniques of neural networks through the study of the most important neural network models.
4. Evaluate whether neural networks are appropriate to a particular application.
5. Apply neural networks to particular application, and to know what steps to take to improve performance.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- **Neural Networks A Classroom Approach** –Satish Kumar, McGraw Hill Education (India) Pvt. Ltd, Second Edition.

Reference Books:

1. **Introduction to Artificial Neural Systems -** J.M. Zurada, Jaico Publications 1994.
2. **Artificial Neural Networks-** B. Yegnanarayana, PHI, New Delhi 1998.

ADDITIONAL OPEN ELECTIVES-B OFFERED BY EC/TC BOARD

B. E. EC/TE Choice Based Credit System (CBCS) and Outcome Based Education (OBE) SEMESTER – VII			
ARM EMBEDDED SYSTEMS			
Course Code	**18EC753**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40(8Hours/Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course objective: This course will enable students to:

- Understand the importance and applications of ARM Design
- Know the architecture of ARM processor
- Use instruction sets of ARM processor
- Analyze the adaptation of C code, firmware, OS, Interrupts, caches, etc. in ARM embedded systems

Module-1	RBT Level
ARM Embedded Systems Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications. **ARM Processor Fundamentals** ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions.	**L1, L2**
Module-2	
Introduction to the ARM Instruction set Introduction, Data processing instructions, Load - Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, Conditional Execution. ALP programming.	**L1, L2, L3**
Module-3	
Introduction to the THUMB instruction set Introduction, THUMB register usage, ARM – THUMB interworking, Other branch instructions, Data processing instructions, Stack instructions, Software interrupt instructions. ALP programming	**L1, L2, L3**
Module-4	
Efficient C Programming: Overview of C Compilers and optimization, Basic C data types, Local Variable Types, Portability issues **Exception and Interrupt Handling:** Exception Handling-ARM Processor Exceptions and Modes, Vector Table, Exception Priorities, Link Register Offset, Interrupts- Interrupt Latency, Basic Interrupt Stack design and implementation, Interrupt Handling Schemes (**general description only** of the schemes)	**L1, L2, L3, L4**
Module-5	
Firmware: Firmware and Bootloader **Embedded Operating Systems:** Fundamental Components **Caches:** The memory Hierarchy and caches memory-caches and memory management units, Cache architecture basic architecture of caches memory, basic operation of cache controller, the relationship between cache and main memory.	**L1, L2**

Course Outcomes: After studying this course, students will be able to:

1. Depict the organization, architecture, bus technology, memory and operation of the ARM processors
2. Employ the knowledge of Instruction set of ARM processors to develop basic Assembly Language Programs
3. Recognize the importance of the Thumb mode of operation of ARM processors
4. Describe the techniques involved in writing C code for ARM processors and Exception & Interrupt handling in ARM Processors
5. Describe the importance and use of Firmware, OS and cache in ARM Embedded systems

Students have to conduct the following experiments as a part of CIE marks along with other Activities:

Conduct the following experiments by writing Assembly Language Program (ALP) using ARM Cortex M3 Registers using an evaluation simulator and the required software tool.

1. Write an ALP to find the sum of 10 integer numbers.
2. Write an ALP to multiply two 16-bit binary numbers.
3. Write an ALP to find factorial of a number.
4. Write an ALP to add an array of 16-bit numbers and store the 32-bit result in internal RAM
5. Write an ALP to find the square of a number (1 to 10) using look-up table.
6. Write an ALP to find the largest/smallest number in an array of 32 numbers.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

"ARM System Developers Guide", Andrew N Sloss, Dominic System and Chris Wright, Elsevier, Morgan Kaufmann publisher, 1st Edition, 2008, ISBN:1758608745.

References:

1. "ARM System on chip Architecture", Furber S, Addison Wiley, 2nd Edition, 2008, ISBN:9780201675191
2. "Embedded System", Rajkamal, Tata McGraw-Hill Publishers, 2nd Edition, 2008, ISBN: 0070494703.

ADDITIONAL OPEN ELECTIVES-B OFFERED BY EC/TC BOARD

B. E. EC/TE Choice Based Credit System (CBCS) and Outcome Based Education (OBE) SEMESTER – VII			
DIGITAL SYSTEMS DESIGN USING VHDL			
Course Code	**18EC754**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40(8Hours/Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course objective: This course will enable students to:

- Use the industry-standard hardware description language VHDL into the digital design process.
- Design VHDL models ranging in complexity from a simple adder to more complex circuits.
- Understand the synthesis and testing of the models.

Module-1	**RBT Level**
Review of Logic Design Fundamentals: Combinational logic, Boolean Algebra and Algebraic Simplification, Karnaugh maps, Designing with NAND and NOR gates, Hazards in combinational Networks, Flipflop and Latches, Mealy Sequential Network Design, Design of Moore Sequential Network, Equivalent states and reduction of state Tables, Synchronous Design, Tristate Logic and Buses (Text 1, Chapter 1- 1.1 to 1.9, 1.12, 1.13)	**L1, L2, L3**
Module-2	
Introduction to VHDL: VHDL Description of Combinational Networks, Modeling Flip-flops using VHDL Processes, VHDL Models for a Multiplexer, Modeling a sequential Machine, Variables, signals, and constants, Arrays, VHDL operators, VHDL Functions, VHDL Procedures, Packages and Libraries. (Text 1, Chapter 2- 2.1, 2.2, 2.3, 2.5, 2.6, 2.7, 2.8, 2.9, 2.10, 2.11)	**L1, L2, L3**
Module-3	
Styles of Descriptions: VHDL Data types, VHDL Styles of Description (Text 2, Chapter 1- 1.5, 1.6) **Data flow Description**: Highlights of Data flow Description, Structure of Data flow Description, Data type-vectors, Common VHDL programming Errors (Text 2, Chapter 2- 2.1- to- 2.4)	**L1, L2, L3**
Module-4	
Designing with programmable Logic Devices: Read only memories, Programmable Logic Arrays, Programmable Array Logic, Other sequential programmable Logic Devices (PLDs), Generics, Generate statements. (Text 1, Chapter 3- 3.1, 3.2, 3.3, 3.4) **Design of Networks for Arithmetic Operations:** Design of serial Adder with Accumulator, Design of Binary Multiplier, Multiplication of signed Binary Numbers, Design of Binary Divider (Text 1, Chapter 4- 4.1, 4.3, 4.4, 4.5)	**L1, L2, L3**
Module-5	
Synthesis: Highlights of synthesis, synthesis information from entity and module, Mapping process in the hardware domain- Mapping of signal assignment, variable	**L1, L2, L3**

assignment, if statements, else-if statements, loop statement. (Text 2, Chapter5- 10.1, 10.2, 10.3) **Hardware Testing and Design for Testability**: Testing Combinational Logic, Testing Sequential Logic. (Text 1, Chapter 10- 10.1, 10.2))	

Course Outcomes: After studying this course, students will be able to:

1. Understand the basic concepts of Digital Design
2. Implement various Combinational and sequential circuits using VHDL descriptions. Write simple VHDL programs in different styles.
3. Design and verify the functionality of digital circuits (PLA, PAL, PLD) and Arithmetic Operations.
4. Identify the suitable Abstraction level for a particular digital design.
5. Write the programs more effectively using Verilog tasks and directives. Perform timing and delay Simulation.

Students have to conduct the following experiments as a part of CIE marks along with other Activities:

Conduct the following experiments using an suitable simulator and the required software tool.

1. Write a VHDL code to implement half and full adder using Data flow style.
2. Write a VHDL code to realize various logic gates.
3. Write a VHDL code to implement four-bit full adder using structural style.
4. Write a VHDL code to implement 2*2 unsigned combinational Array Multiplier.
5. Write a VHDL code to implement D Latch.
6. Implement JK flip flop modeling using VHDL process

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "Digital Systems Design using VHDL", Charles H. Roth, Jr., The University of Texas at Austin. 2006 reprint, Thomson Asia Pte Ltd, Singapore
2. "HDL Programming VHDL and Verilog", Nazeih M. Botros, 2009 reprint, Dreamtech press

Reference:

"VHDL for Programmable Logic", Kevin Skahill, Pearson education, 2006

SEMESTER – VIII

WIRELESS and CELLULAR COMMUNICATION

Course Code	: 18EC81	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs / Module)	Exam Hours	: 03
	CREDITS – 03		

Course Learning Objectives: This course will enable students to:

- Understand the concepts of propagation over wireless channels from a physics standpoint
- Application of Communication theory both Physical and networking to understand GSM systems that handle mobile telephony
- Application of Communication theory both Physical and networking to understand CDMA systems that handle mobile telephony.
- Application of Communication theory both Physical and networking to understand LTE-4G systems.

Module-1

Mobile Radio Propagation –
Large Scale Path Loss - Free Space Propagation Model, Relating Power to Electric Field, Three Basic Propagation Mechanisms – Reflection (Ground Reflection) , Diffraction, Scattering, Practical Link Budget,
(Text 1 - 2.2 and Ref1 - Chapter 4)
Fading and Multipath – Broadband wireless channel, Delay Spread and Coherence Bandwidth, Doppler Spread and Coherence Time, Angular spread and Coherence Distance **(Text 1 – 2.4)**
Statistical Channel Model of a Broadband Fading Channel
(Text 1 – 2.5.1)
The Cellular Concept – Cellular Concept , Analysis of Cellular Systems, Sectoring
(Text 1- 2.3) **L1, L2**

Module-2

GSM and TDMA Technology
GSM System overview – Introduction, GSM Network and System Architecture, GSM Channel Concept.

GSM System Operations – GSM Identities, System Operations –Traffic cases, GSM Infrastructure Communications (Um Interface)
(Text 2, Part1 and Part 2 of Chapter 5) **L1,L2,L3**

Module-3

CDMA Technology
CDMA System Overview – Introduction, CDMA Network and System Architecture
CDMA Basics – CDMA Channel Concepts, CDMA System (Layer 3) operations, 3G CDMA
(Text 2-Part 1, Part2 and Part 3 of Chapter 6) **L1,L2,L3**

Module-4

LTE – 4G
Key Enablers for LTE 4G – OFDM, SC-FDE, SC-FDMA, Channel Dependant Multiuser Resource Scheduling, Multi-Antenna Techniques, Flat IP Architecture, LTE Network Architecture. **(Text 1, Sec 1.4)**
Multi-Carrier Modulation – Multicarrier concepts, OFDM Basics, OFDM in LTE, Timing and Frequency Synchronization, Peak to Average Ration, SC-Frequency Domain Equalization, Computational Complexity Advantage of OFDM and SC-FDE.
(Text 1, Sec 3.1 – 3.7) **L1,L2,L3**

Module-5

LTE - 4G
OFDMA and SC-FDMA – Multiple Access for OFDM Systems, OFDMA, SCFDMA, Multiuser Diversity and Opportunistic Scheduling, OFDMA and SC-FDMA in LTE, OFDMA system Design Considerations.
(Text 1, Sec 4.1 – 4.6)
The LTE Standard – Introduction to LTE and Hierarchical Channel Structure of LTE, Downlink OFDMA Radio Resources, Uplink SC-FDMA Radio Resources.
(Text 1, Sec 6.1 – 6.4) **L1, L2,L3**

Course Outcomes: After studying this course, students will be able to:

1. Understand the Communication theory both Physical and networking associated with GSM, CDMA & LTE 4G systems.
2. Explain concepts of propagation mechanisms like Reflection, Diffraction, Scattering in wireless channels.
3. Develop a scheme for idle mode, call set up, call progress handling and call tear down in a GSM cellular network.

4. Develop a scheme for idle mode, call set up, call progress handling and call tear down in a CDMA cellular network.
5. Understand the Basic operations of Air interface in a LTE 4G system.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "Fundamentals of LTE" Arunabha Ghosh, Jan Zhang, Jefferey Andrews, Riaz Mohammed, Pearson education (Formerly Prentice Hall, Communications Engg and Emerging Technologies), ISBN-13: 978-0-13-703311-9.
2. "Introduction to Wireless Telecommunications Systems and Networks", Gary Mullet, First Edition, Cengage Learning India Pvt Ltd., 2006, ISBN - 13: 978-81-315-0559-5.

Reference Books:

1. "Wireless Communications: Principles and Practice" Theodore Rappaport, 2nd Edition, Prentice Hall Communications Engineering and Emerging Technologies Series, 2002, ISBN 0-13-042232-0.
2. LTE for UMTS Evolution to LTE-Advanced' Harri Holma and Antti Toskala, Second Edition - 2011, John Wiley & Sons, Ltd. Print ISBN: 9780470660003. 2

NETWORK SECURITY

Course Code	: 18EC821	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Describe network security services and mechanisms.
- Understand Transport Level Security and Secure Socket Layer
- Know about Security concerns in Internet Protocol security
- Discuss about Intruders, Intrusion detection and Malicious Software
- Discuss about Firewalls, Firewall characteristics, Biasing and Configuration

Module-1

Attacks on Computers and Computer Security: Need for Security, Security Approaches, Principles of Security Types of Attacks.
(Chapter1-Text2) **L1, L2**

Module-2

Transport Level Security: Web Security Considerations, Secure Sockets Layer, Transport Layer Security, HTTPS, Secure Shell (SSH)
(Chapter15- Text1) **L1,L2**

Module-3

IP Security: Overview of IP Security (IPSec),IP Security Architecture, Modes of Operation, Security Associations (SA), Authentication Header (AH), Encapsulating Security Payload (ESP), Internet Key Exchange.
(Chapter19-Text1) **L1,L2**

Module-4

Intruders, Intrusion Detection.**(Chapter20-Text1)**
MALICIOUS SOFTWARE: Viruses and Related Threats, Virus Counter measures,
(Chapter21-Text1) **L1,L2**

Module-5

Firewalls: The Need for firewalls, Firewall Characteristics, Types of Firewalls, Firewall Biasing, Firewall location and configuration
(Chapter22-Text 1) **L1, L2**

Course Outcomes: After studying this course, students will be able to:

1. Explain network security services and mechanisms and explain security concepts
2. Understand the concept of Transport Level Security and Secure Socket Layer.
3. Explain Security concerns in Internet Protocol security
4. Explain Intruders, Intrusion detection and Malicious Software
5. Describe Firewalls, Firewall Characteristics, Biasing and Configuration

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOKS:

1. Cryptography and Network Security Principles and Practice , Pearson Education Inc., William Stallings, 5th Edition, 2014, ISBN: 978-81-317- 6166-3.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

REFERENCE BOOKS:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.

MICRO ELECTRO MECHANICAL SYSTEMS

Course Code	: 18EC822	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (8 Hrs /Module)	Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand overview of microsystems, their fabrication and application areas.
- Working principles of several MEMS devices.
- Develop mathematical and analytical models of MEMS devices.
- Know methods to fabricate MEMS devices.
- Various application areas where MEMS devices can be used.

Module-1

Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.

L1, L2

Module-2

Working Principles of Microsystems: Introduction, Microsensors, Microactuation, MEMS with Microactuators, Microaccelerometers, Microfluidics.

Engineering Science for Microsystems Design and Fabrication: Introduction, Molecular Theory of Matter and Inter-molecular Forces, Plasma Physics, Electrochemistry.

L1,L2

Module-3

Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermo mechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.

L1,L2

Module-4

Scaling Laws in Miniaturization: Introduction, Scalingin Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling in Fluid Mechanics, Scaling in Heat Transfer.

L1,L2

Module-5

Overview of Micromanufacturing: Introduction, Bulk Micromanufacturing, Surface Micromachining, The LIGA Process, Summary on Micro manufacturing.

L1, L2

Course Outcomes: After studying this course, students will be able to:

1. Appreciate the technologies related to Micro Electro Mechanical Systems.
2. Understand design and fabrication processes involved with MEMS Devices.
3. Analyze the MEMS devices and develop suitable mathematical models.
4. Know various application areas for MEMS device.
5. Describe the Micromanufacturing.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- Tai-Ran Hsu, MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering, 2nd Ed, Wiley.

Reference Books:

1. Hans H. Gatzen,Volker Saile, JurgLeuthold, Micro and Nano Fabrication: Tools and Processes, Springer, 2015.
2. Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Microelectromechanical Systems (MEMS), Cengage Learning.

RADAR ENGINEERING

Course Code	: 18EC823	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand the Radar fundamentals and analyze the radar signals.
- Understand various technologies involved inthe designo fradar transmitters and receivers.
- Learn various radars like MTI, Doppler and tracking radars and their comparison

Module-1

Basics of Radar: Introduction, Maximum Unambiguous Range, Radar Waveforms, Definitions with respect to pulse wave form-PRF, PRI, Duty Cycle, Peak Transmitter Power, Average transmitter Power. Simple form of the Radar Equation, Radar Block Diagram and Operation, Radar Frequencies, Applications of Radar, The Origins of Radar, Illustrative Problems.

(Chapter 1 of Text) **L1, L2,L3**

Module-2

The Radar Equation: Prediction of Range 'Performance, Detection of signal in Noise, Minimum Detectable Signal, Receiver Noise, SNR, Modified Radar Range Equation, Envelope Detector - False Alarm Time and Probability, Probability of Detection, Radar Cross Section of Targets: simple targets – sphere, cone-sphere, Transmitter Power, PRF and Range Ambiguities, System Losses (qualitative treatment), Illustrative Problems.

(Chapter 2 of Text, Except 2.4, 2.6, 2.8 & 2.11) **L1,L2,L3**

Module-3

MTI and Pulse Doppler Radar: Introduction, Principle, Doppler Frequency Shift, Simple CW Radar, Sweep to Sweep subtraction and Delay Line Canceler, MTI Radar with– Power Amplifier Transmitter, Delay Line Cancelers— Frequency Response of Single Delay- Line Canceler, Blind Speeds, Clutter Attenuation, MTI Improvement Factor, N- Pulse Delay-Line Canceler, Digital MTI Processing–Blind phases, I and Q Channels, Digital MTI Doppler signal processor, Moving Target Detector- Original MTD.

(Chapter 3: 3.1, 3.2, 3.5, 3.6 of Text) **L1,L2,L3**

Module-4

Tracking Radar: Tracking with Radar- Types of Tracking Radar Systems,

Monopulse Tracking- Amplitude Comparison Monopulse (one-and two-coordinates), Phase Comparison Monopulse.
Sequential Lobing, Conical Scan Tracking, Block Diagram of Conical Scan Tracking Radar, Tracking in Range, Comparison of Trackers.
(Chapter4: 4.1, 4.2, 4.3 of Text), L1,L2,L3

Module-5

The Radar Antenna : Functions of The Radar Antenna, Antenna Parameters, Reflector Antennas and Electronically Steered Phase darray Antennas. (Chapter 9:9.1,9.29.4, 9.5 of Text)
Radar Receiver: The Radar Receiver, Receiver Noise Figure, Super Heterodyne Receiver, Duplexers and Receivers Protectors, Radar Displays. **(Chapter 11 of Text), L1, L2,L3**

Course Outcomes: At the end of the course, students will be able to:

1. Describe the radar fundamentals.
2. Analyze the radar signals.
3. Explain the working principle of pulse Doppler radars, their applications and limitations.
4. Describe the working of various radar transmitters and receivers.
5. Analyze the range parameters of pulse radar system which affect the system performance.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOK:

Introduction to Radar Systems- Merrill I Skolink, 3e, TMH, 2001

REFERENCE BOOKS:

1. Radar Principles, Technology, Applications—ByronEdde, Pearson Education, 2004.
2. Radar Principles–Peebles. Jr, P.Z. Wiley. New York, 1998.
3. Principles of Modem Radar: Basic Principles–Mark A. Rkhards, James A. Scheer, William A. HoIm. Yesdee, 2013

OPTICAL COMMUNICATION NETWORKS

Course Code	: 18EC824	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Learn the basic principle of optical fiber communication with different modes of light propagation.
- Understand the transmission characteristics and losses in optical fiber.
- Study of optical components and its applications in optical communication networks.
- Learn the network standards in optical fiber and understand the network architectures along with its functionalities.

Module -1

Optical fiber Communications: Historical development, The general system, Advantages of optical fiber communication, Optical fiber wave guides: Ray theory transmission, Modes in planar guide, Phase and group velocity, Cylindrical fiber: Modes, Step index fibers, Graded index fibers, Single mode fibers, Cutoff wavelength, Mode field diameter, effective refractive index. Fiber Materials, Photonic crystal fibers.

(Text 2) **L1, L2**

Module -2

Transmission characteristics of optical fiber: Attenuation, Material absorption losses, Linear scattering losses, Nonlinear scattering losses, Fiber bend loss, Dispersion, Chromatic dispersion, Intermodal dispersion: Multimode step index fiber.

Optical Fiber Connectors: Fiber alignment and joint loss, Fiber splices: Fusion Splices, Mechanical splices, Fiber connectors: Cylindrical ferrule connectors, Duplex and Multiple fiber connectors, Fiber couplers: three and four port couplers, star couplers, Optical Isolators and Circulators.

(Text 2) **L1, L2**

Module -3

Optical sources: Light Emitting diodes: LED Structures, Light Source Materials, Quantum Efficiency and LED Power, Modulation. Laser Diodes: Modes and Threshold conditions, Rate equation, External Quantum Efficiency, Resonant Frequencies.

Photodetectors: Physical principles of Photodiodes, Photo detector noise, Detector response time.

Optical Receiver: Optical Receiver Operation: Error sources, Front End Amplifiers, Receiver sensitivity, Quantum Limit.
(Text1)

L1, L2

Module -4

WDM Concepts and Components: Overview of WDM: Operational Principles of WDM, WDM standards, Mach-Zehnder Interferometer Multiplexers, Isolators and Circulators, Fiber grating filters, Dielectric Thin-Film Filters, Diffraction Gratings. Optical amplifiers: Basic application and Types, Semiconductor optical amplifiers, Erbium Doped Fiber Amplifiers, Raman Amplifiers, Wideband Optical Amplifiers.
(Text 1) **L1, L2**

Module -5

Optical Networks : Optical network evolution and concepts: Optical networking terminology, Optical network node and
switching elements, Wavelength division multiplexed networks, Public telecommunication network overview. Optical network transmission modes, layers and protocols: Synchronous networks, Asynchronous transfer mode, OSI reference model, Optical transport network, Internet protocol, Wavelength routing networks: Routing and wavelength assignment, Optical switching networks: Optical circuit switched networks, packet switched networks, Multiprotocol Label Switching, Optical burst switching networks.
(Text 2) **L1, L2**

Course Outcomes: At the end of the course, students will be able to:

1. Classify and describe working of optical fiber with different modes of signal propagation.
2. Describe the transmission characteristics and losses in optical fiber communication.
3. Describe the construction and working principle of optical connectors, multiplexers and amplifiers.
4. Describe the constructional features and the characteristics of optical Sources and detectors.
5. Illustrate the networking aspects of optical fiber and describe various standards associated with it.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.

- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Gerd Keiser, Optical Fiber Communication, 5th Edition, Mc Graw Hill Education (India) Private Limited, 2015. ISBN:1-25-900687-5.
2. John M Senior, Optical Fiber Communications, Principles and Practice, 3rd Edition, Pearson Education, 2010, ISBN:978-81-317-3266-3

Reference Book:

- Joseph C Palais, Fiber Optic Communication, Pearson Education, 2005, ISBN:0130085103.

BIOMEDICAL SIGNAL PROCESSING

Course Code	: 18EC825	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (8 Hrs /Module)	Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives:

This course will enable students to:

- Describe the origin, properties and suitable models of important biological signals such as ECG and EEG.
- Know the basic signal processing techniques in analysing biological signals.
- Acquire mathematical and computational skills relevant to the field of biomedical signal processing.
- Describe the basics of ECG signal compression algorithms.
- Know the complexity of various biological phenomena.
- Understand the promises, challenges of the biomedical engineering.

Module -1

Introduction to Biomedical Signals: The nature of Biomedical Signals, Examples of Biomedical Signals, Objectives and difficulties in Biomedical analysis.

Electrocardiography: Basic electrocardiography, ECG leads systems, ECG signal characteristics.

Signal Conversion :Simple signal conversion systems, Conversion requirements for biomedical signals, Signal conversion circuits

(Text-1) **L1,L2**

Module -2

Signal Averaging: Basics of signal averaging, signal averaging as a digital filter, a typical averager, software for signal averaging, limitations of signal averaging.

Adaptive Noise Cancelling: Principal noise canceller model, 60-Hz adaptive cancelling using a sine wave model, other applications of adaptive filtering

(Text-1) **L1,L2,L3**

Module -3

Data Compression Techniques: Turning point algorithm, AZTEC algorithm, Fan algorithm, Huffman coding, data reduction algorithms The Fourier transform, Correlation, Convolution, Power spectrum estimation, Frequency domain analysis of the ECG **(Text-1)** **L1,L2, L3**

Module -4

Cardiological signal processing:

Basic Electrocardiography, ECG data acquisition, ECG lead system, ECG signal characteristics (parameters and their estimation), Analog filters, ECG amplifier, and QRS detector, Power spectrum of the ECG, Bandpass filtering techniques, Differentiation techniques, Template matching techniques, A QRS detection algorithm, Real-time ECG processing algorithm, ECG interpretation, ST segment analyzer, Portable arrhythmia monitor.

(Text -2) **L1,L2, L3**

Module -5

Neurological signal processing: The brain and its potentials, The electrophysiological origin of brain waves, The EEG signal and its characteristics (EEG rhythms, waves, and transients), Correlation.

Analysis of EEG channels: Detection of EEG rhythms, Template matching for EEG, spike and wave detection

(Text-2)

L1,L2, L3

Course Outcomes: At the end of the course, students will be able to:

1. Possess the basic mathematical, scientific and computational skills necessary to analyse ECG and EEG signals.
2. Apply classical and modern filtering and compression techniques for ECG and EEG signals.
3. Develop a thorough understanding on basics of ECG and EEG feature extraction.
4. Evaluate various event detection techniques for the analysis of the EEG and ECG.
5. Develop algorithms to process and analyze biomedical signals for better diagnosis.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. **Biomedical Digital Signal Processing-** Willis J. Tompkins, PHI 2001.
2. **Biomedical Signal Processing Principles and Techniques-** D C Reddy, McGraw- Hill publications 2005.

Reference Book:

- **Biomedical Signal Analysis-**Rangaraj M. Rangayyan, John Wiley & Sons 2002.