18EC62
Embedded System

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A+, Accredited by NAAC & NBA (ECE & CSE)
Shobhavana Campus, MIJAR-574225, Moodbidri, D.K., Karnataka
Ph: 08258-262725; Mob:722262724,7026262725,mail:principalaiet08@gmail.com

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Course File –Check list	
1	Academic Calender
2	Time Table (Personal & Class)
3	Subject Syllabus
4	CO-PO-PSO Mapping and Justification
5	Student Name List
6	Internal Question Papers with Answer keys
7	Assignment Questions /Topics and Marks
8	Content Beyond the syllabus
9	Internal Bitwise Marks
10	University Result Analysis
11	CO-PO-PSO Attainment
12	VTU Model /Old Question Papers

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Verified by: HOD

Academic Year	Signature	Academic Year	Signature
2022-23			

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VISION

"Transformative education by pursuing excellence in Engineering and Management through enhancing skills to meet the evolving needs of the community"

MISSION

- To bestow quality technical education to imbibe knowledge, creativity and ethos to students community.
- To inculcate the best engineering practices through transformative education.
- To develop a knowledgeable individual for a dynamic industrial scenario.
- To inculcate research, entrepreneurial skills and human values in order to cater the needs of the society.

Week	Month	Days							Activities
		Mon	Tue	Wed	Thu	Fri	Sat	Sun	
1	FEB	13	14	15	16	17	18	19	13 : Commencement of VIII Semester
2		20	21	22	23	24	25	26	
3		27	28						
4	MAR			1	2	3	4	5	20 : Commencement of VI Semester 22nd : Chandramana Ugadi 27 – 31 : Technical Talk/Club and Social Activity 30 - 31 : 1st IA for VIII Semester
5		6	7	8	9	10	11	12	
6		13	14	15	16	17	18	19	
7		20	21	22	23	24	25	26	
8		27	28	29	30	31			
9	APR						1	2	3 : Mahaveera Jayanthi 7: Good Friday 14: Dr B.R. Ambedkar Jayanti 22: Khutha-e-Ramzan 20-21 – Student Mentoring 26 : College Level Project Exhibition 27-28 : 2nd IA for VIII Semester 24– 29 Technical Talk/Club / Social Activity
10		3	4	5	6	7	8	9	
11		10	11	12	13	14	15	16	
12		17	18	19	20	21	22	23	
13		24	25	26	27	28	29	30	
14	MAY	1	2	3	4	5	6	7	1 : Labor day 6 : Sports Day 8-9 : 3rd IA for VIII Semester 13 : Last Working Day of VIII Semester 17 : Commencement of IV Semester 20 : Traditional Day. 22 : College Day Celebration 25 : Commencement of II Semester 26 : Farewell Function to Final Years 22-23 : Student Mentoring 25 - 27 : 1st IA for VI Semester 29-31 : Technical Talk/Club / Social Activity
15		8	9	10	11	12	13	14	
16		15	16	17	18	19	20	21	
17		22	23	24	25	26	27	28	
18		29	30	31					
19	JUN				1	2	3	4	16 To 19 : 2nd IA for VI Semester 26-27 : Student Mentoring 20 - 24 : Technical Talk/Club / Social Activity 28 , 30 & 1st July : 1st IA for IV Semester 30/Jun to 4/July : 1st IA for II Semester 29- Bakrid
20		5	6	7	8	9	10	11	
21		12	13	14	15	16	17	18	
22		19	20	21	22	23	24	25	
23		26	27	28	29	30			
24	JULY						1	2	1-4 : 1st IA for II Semester 5– 7 : 3rd IA for VI Semester 10 : Last Working Day of VI Semester 17 - 22 : Technical Talk/Club / Social Activity 24-25 : Student Mentoring 29 : Last Day of Moharamm
25		3	4	5	6	7	8	9	
26		10	11	12	13	14	15	16	
27		17	18	19	20	21	22	23	
28		24	25	26	27	28	29	30	
29		31							
30	AUG		1	2	3	4	5	6	4 To 8 : 2nd IA for II Semester 4 To 7 : 2nd IA for IV Semester 15 : Independence Day 24-25 : Student Mentoring 28 - 31 : Technical Talk/Club / Social Activity
31		7	8	9	10	11	12	13	
32		14	15	16	17	18	19	20	
33		21	22	23	24	25	26	27	
34		28	29	30	31				
35	SEP					1	2	3	1 To 5 : 3rd IA for II Semester 8 To 11 : 3rd IA for IV Semester 9 : Last Working Day of II Semester 16 : Last Working Day of IV Semester
36		4	5	6	7	8	9	10	
37		11	12	13	15	16	17	18	

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(Accredited by NBA)

Time Table with effect from 02/05/2023(V2)

Academic Year	Scheme	Semester	Section	Class Coordinator	Room No
2022-23	2018	6th	A	Mrs. Ansha Prathibha	306

Time / Day	9.00 To 9.55	9.55 To 10.50	10.50 To 11.10	11.10 To 12.05	12.05 To 1.00	1.00 To 2.00	2.00 To 3.00	3.00 To 4.00	4.00 To 5.00
MON	ES	MWA	BREAK	DC	APT(ANP)	LUNCH	Soft Skill Training		OE
TUE	MWA	DC		OS	ES		Comm. Lab A2(VTS+NI) ES Lab A1 (ANP+ES)		OE
WED	OS	DC		MWA	Library Hour		Soft Skill Training		OE
THU	DC	MWA		OS	ES		Comm. Lab A2(VTS+NI) ES Lab A1 (ANP+ES)		OE
FRI	ES	DC		APT(ANP)	MENTOR MEETING		MINI PROJECT(GP)		OE
SAT	MWA	OS		ES	APT(SW)				

Allocation of Subjects

Subjects			Staffs	Staff Code
DC	18EC61	Digital Communication	Mrs. Vijetha T.S.	VTS
ES	18EC62	Embedded Systems	Mrs. Ansha Prathibha	ANP
MWA	18EC63	Microwave & Antennas	Dr.Guruprasad	GP
OS	18EC641	Operating System	Mrs. Vijetha T.S.	VTS
OE	18ME651	Non-Conventional Energy Sources	Prof.Srinivas C S - 504 CV	
	18ME653	Supply Chain Management	Prof.Pramod K N - 314 CSE	
	18CV653	Occupational Health & Safety	Prof.Anusha B Rao - 312 CSE	
	18CV651	Remote Sensing & GIS	Dr.Umeshchandra - 502 CV	
	18CS652	Introduction to DATA Structures & Algorithms	Dr.Sudheer Shetty - 301 EC	
ES-LAB	18ECL66	Embedded Systems Lab	Mrs. Ansha Prathibha	ANP
CS-LAB	18ECL67	Communication System Lab	Mrs. Vijetha T.S.	VTS

Time Table Coordinator

H.O.D

B. E. (EC / TC) Choice Based Credit System (CBCS) and Outcome Based Education (OBE) SEMESTER – VI			
EMBEDDED SYSTEMS			
Course Code	**18EC62**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03+2 (Tutorial)**	**SEE Marks**	**60**
		Exam Hours	**03**
CREDITS – 04			

Course Learning Objectives: This course will enable students to:

- Explain the architectural features and instructions of 32 bit microcontroller -ARM Cortex M3.
- Develop Programs using the various instructions of ARM Cortex M3 and C language for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Develop the hardware software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

Module 1	**RBT Level**
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence **(Text 1: Ch-1, 2, 3)**	**L1,L2**
Module 2	
ARM Cortex M3 Instruction Sets and Programming: Assembly basics, Instruction list and description, Thumb and ARM instructions, Special instructions, Useful instructions, CMSIS, Assembly and C language Programming **(Text 1: Ch-4, Ch-10.1 to 10.6)**	**L1,L2, L3**
Module 3	
Embedded System Components: Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Elements of an Embedded System (Block diagram and explanation), Differences between RISC and CISC, Harvard and Princeton, Big and Little Endian formats, Memory (ROM and RAM types), Sensors, Actuators, Optocoupler, Communication Interfaces (I2C, SPI, IrDA, Bluetooth, Wi-Fi, Zigbee only) **(Text 2: All the Topics from Ch-1 and Ch-2 (Fig and explanation before 2.1) 2.1.1.6 to 2.1.1.8, 2.2 to 2.2.2.3, 2.3 to 2.3.2, 2.3.3.3, selected topics of 2.4.1 and 2.4.2 only).**	**L1,L2**
Module 4	
Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modeling (excluding UML), Embedded firmware design and development (excluding C language). **Text 2: Ch-3, Ch-4 (4.1, 4.2.1 and 4.2.2 only), Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)**	**L1,L2, L3**
Module 5	
RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques **(Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch-12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)**	**L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.
- Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Develop the hardware software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", 2nd Edition, Newnes, (Elsevier), 2010.
2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2nd Edition.

Reference Books:

1. James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008, ISBN: 978-0-471-72180-2.
2. Yifeng Zhu, "Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C", 2nd E -Man Press LLC ©2015 ISBN:0982692633 9780982692639.
3. Embedded real time systems by K.V. K. K Prasad, Dreamtech publications, 2003.
4. Embedded Systems by Rajkamal, 2nd Edition, McGraw hill Publications, 2010.

EMBEDDED SYSTEMS

Course Code	: 18EC62	CIE Marks : 40
Lecture Hours/Week	: 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)		Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to:

- Explain the architectural features and instructions of 32 bit microcontroller -ARM Cortex M3.
- Develop Programs using the various instructions of ARM Cortex M3 and C language for different applications.
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- Develop the hardware software co-design and firmware design approaches.
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ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence **(Text 1: Ch-1, 2, 3)**

L1,L2

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L1,L2,L3

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(Text 2: All the Topics from Ch-1 and Ch-2 (Fig and explanation before 2.1) 2.1.1.6 to 2.1.1.8, 2.2 to 2.2.2.3, 2.3 to 2.3.2, 2.3.3.3, selected topics of 2.4.1 and 2.4.2 only).

L1, L2

Module 4

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L1,L2,L3

Module 5

RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques **(Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch-12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)**

L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.
2. Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
3. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
4. Develop the hardware software co-design and firmware design approaches.
5. Explain the need of real time operating system for embedded system applications.

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3. K.V. K. K Prasad, Embedded Real Time Systems, Dreamtech publications, 2003.
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Department of Electronics and Communication Engineering
3rd Year Student List

#	USN	Student Name
1	4AL20EC001	Aishwarya A P
2	4AL20EC002	Aishwarya Panchagavi
3	4AL20EC004	Akshay
4	4AL20EC005	Akshay Sonar
5	4AL20EC006	Aravinda Jogi
6	4AL20EC007	Bhavana M
7	4AL20EC008	Chaithrashree M G
8	4AL20EC010	Chethana.M
9	4AL20EC011	Darshan Madival
10	4AL20EC012	Disha H
11	4AL20EC013	Harshitha D K
12	4AL20EC014	Jyoti Phakkirannanavar
13	4AL20EC015	K.Vijay Bhanu
14	4AL20EC016	Karthik G Shet
15	4AL20EC017	Kishan Kumar
16	4AL20EC018	Krathika
17	4AL20EC019	Kshama Tc
18	4AL20EC020	Libina Lal
19	4AL20EC021	Manjunath Sajjan
20	4AL20EC023	Mohammed Sharfuddin
21	4AL20EC024	Mokshith
22	4AL20EC025	Monika. D. B.
23	4AL20EC026	Monisha P
24	4AL20EC027	Nagarjuna GS
25	4AL20EC028	Padala Sattibabu
26	4AL20EC029	P V Likhitha
27	4AL20EC030	Pavan Kh
28	4AL20EC031	Pooja P
29	4AL20EC032	Prajaktha Poojary
30	4AL20EC033	Prajwal R

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Department of Electronics and Communication Engineering
3rd Year Student List

31	4AL20EC034	Prashanth VK
32	4AL20EC035	Pratham Puthran
33	4AL20EC036	Prathish G Nayak
34	4AL20EC037	Praveen Vishwakarma
35	4AL20EC038	Preeti G M
36	4AL20EC039	Rakesh Sangshetty
37	4AL20EC040	Rakshitha S
38	4AL20EC041	Ramya K
39	4AL20EC042	Ranjitha R
40	4AL20EC043	Rohan H
41	4AL20EC045	Sangamesh Biradar
42	4AL20EC046	Sanjay Gk
43	4AL20EC048	Santhripti C S
44	4AL20EC049	Shravan V Upadhyaya
45	4AL20EC050	Shridevi Rao
46	4AL20EC051	Shruthi
47	4AL20EC052	Shubhashri S
48	4AL20EC053	Shwetha
49	4AL20EC054	Soumya N
50	4AL20EC055	spoorthi salaskar
51	4AL20EC056	Srujan
52	4AL20EC057	Umesh
53	4AL20EC058	Varshini K L
54	4AL20EC059	Veena Talawar
55	4AL20EC060	Vinod Raj G N
56	4AL20EC061	Vinyashree Jain
57	4AL20EC062	Vishanth
58	4AL20EC063	Vishwanath

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Department of Electronics & Communication Engineering

SEMESTER – VI	**Academic Year: 2022 -2023 (Even Semester)**
Course Code: 18EC62	**Course Name:** Embedded Systems
Course Teacher: Mrs.M.Ansha Prathiba	

Course Outcomes: After studying this course, students will be able to

CO Numbers	Course Outcomes	Blooms Level	Target Level
18EC62.1	Apply the Knowledge of architectural features and instructions of 32 bit microcontroller ARM Cortex M3-32 bit microcontroller in different application.	L1,L2	L2
18EC62.2	Apply the knowledge gained for Programming ARM Cortex M3 for different applications using C and assembly.	L2,L3	L2
18EC62.3	Analyze the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.	L1,L2,L3	L2
18EC62.4	Develop the hardware software co-design and firmware design approaches.	L1,L2,L3	L2
18EC62.5	Apply the knowledge of real time operating system for embedded system applications.	L2,L3	L2

CO-PO/PSO Mapping Matrix:

CO Numbers	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
18EC62.1	3	2	-	-	-	-	-	-	-	-	-	1	3	-	-
18EC62.2	3	3	-	-	3	-	-	-	2	-	-	2	3	-	3
18EC62.3	3	3	3	-	-	-	-	-		-	-	1	3	2	-
18EC62.4	3	3	3	-	-	-	-	-	2	-	-	1	3	2	-
18EC62.5	3	2	-	-	-	2	-	-		-	-	1	3	-	-
SUM	**15**	**11**	**6**	-	**3**	**2**	-	-	**4**	-	-	**6**	**15**	**4**	**3**
AVG	**3**	**2.2**	**3**	-	**3**	**2**	-	-	**2**	-	-	**1.2**	**3**	**2**	**3**

Justification of Course Outcome and Program Outcome mapping

CO Numbers	PO &PSO	Level	Justification
18EC62.1	PO1	3	Highly mapped as the student will be able to apply the knowledge gained to utilize the application of ARM Cortex M3 and understand the architectural features of ARM Cortex M3.
	PO2	2	Moderately mapped as the student will be able to identify the application of ARM Cortex M3 and analyze the architectural features of ARM Cortex M3.
	PO12	1	Slightly mapped as the student will be able to use research based knowledge to identify the application of ARM Cortex M3.
	PSO1	3	Highly mapped as the students will be able to understand and apply the features of ARM CortexM3.
18EC62.2	PO1	3	Highly mapped as the students will able to apply the knowledge gained to create and apply appropriate techniques and program ARM Cortex M3in assembly and C using Keil IDE.
	PO2	3	Highly mapped as the student will able to analyze programs of ARM Cortex M3 in assembly and C.
	PO5	3	Highly mapped as the student will able to program ARM Cortex M3 in assembly and C using Keil IDE
	PO9	2	Moderately mapped as the student will be able to write a program in assembly and C for different application and work as individual or team.
	PO12	2	Moderately mapped as the students will be able to research based knowledge to identify the application of ARM Cortex M3.
	PSO1	3	Highly mapped as the student will able to understand the principals of science to understand ARM Cortex M3.
	PSO3	3	Highly mapped as the student will be able to program ARM Cortex M3 in assembly And C by applying modern engineering tools.
18EC62.3	PO1	3	Highly mapped as the students will able to apply the knowledge gained to design system components by understanding how to select hardware based on the characteristics of an embedded system and specific tasks.
	PO2	3	Highly mapped as the student will able to design solution for complex engineering problems by understanding how to select hardware based on the characteristics of an embedded system.
	PO3	3	Highly mapped as the students will be able to design the basic hardware components for an embedded system.
	PO12	1	Slightly mapped as the students will able to use research based knowledge to design the basic hardware component for an embedded system.
	PSO1	3	Highly mapped as the students will able to apply the principles of science to understand how to select hardware component based on the characteristics and attributes of embedded system.
	PSO2	2	Moderately mapped as the student will be able to design the basic hardware components for an embedded system.

18EC62.4	PO1	3	Highly mapped as the student will be able to apply the knowledge gained to understand firmware design approaches and hardware software co-design.
	PO2	3	Highly mapped students will able to analyze the hardware software co-design and firmware design approaches.
	PO3	3	Highly mapped as the students will be able to develop the hardware software co-design and firmware design approaches.
	PO9	2	Moderately mapped as the student will able to work as individual to present hardware software co-design and firmware design.
	PO12	3	Highly mapped as the student will able to use researched based knowledge to develop hardware software co-design and firmware design approaches.
	PSO1	3	Highly mapped as the student will able to understand and apply the principles of hardware software co-design.
	PSO2	2	Moderately mapped as the student will able to design and implement systems using the concepts of hardware software co-design.
18EC62.5	PO1	3	Highly mapped as the student will able to apply the knowledge gained to understand the need of real time operating system for embedded system application.
	PO2	2	Moderately mapped as the student will able to design system with the help of real time operating system.
	PO6	2	Moderately mapped as the student will able to assess societal responsibilities relevant to the Embedded system professional engineering practices.
	PO12	1	Slightly mapped as the student will able to use research based knowledge of real time operating system and IDE for embedded system application.
	PSO1	3	Highly mapped as the student will able to understand and apply the principles of real time operating system for embedded system application.

Course Teacher
Mrs.Ansha Prathiba

IQAC Coordinator
Mr. Sudhakara H M

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ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

(Accredited by NAAC with A+ Grade)

Department of Electronics and Communication Engineering (Accredited by NBA)

Continuous Internal Evaluation Test- 1 AY 2022-23

Course Title : Embedded System		Course Code: 18EC62
Date:25/05/2023	Time:3.00PM to 4.30PM	Semester/Section:6th Sem
Faculty: Mrs.Ansha Prathiba		Max. Marks: 30

Note: Answer ONE FULL question from each Module.

Q. No.		Questions	Marks	COs	BTL
		Module 1			
1	a)	Briefly explain the Thumb-2 technology and its advantages over thumb instruction set with relevant diagram.	5	1	1
	b)	With a neat diagram, explain the architecture of ARM cortex M3 microcontroller.	10	1	2
		OR			
2	a)	What are the various registers in ARM Cortex M3? Specify the function of each of them.	10	1	2
	b)	Explain the stack operations using PUSH and POP instructions in ARM Cortex M3.	5	1	1
		Module 2			
3	a)	Explain the features of Nested vector Interrupt controller of ARM cortex M3	5	1	1
	b)	How the data definition directives are used in ARM Cortex-M3? Provide example instructions.	5	2	2
	c)	Explain the data movement instructions in ARM cortex M3.	5	2	2
		OR			
4	a)	How the suffixes are used in assembler language? Provide example instructions to use suffixes.	5	2	1
	b)	Write a note on LDR and ADR Pseudo-Instructions.	5	1	1
	c)	Describe the debugging support in ARM Cortex M3.	5	2	1

Levels of Bloom's Taxonomy

No.	L1	L2	L3	L4	L5	L6
Level	Remember	Understand	Apply	Analyze	Evaluate	Create

Course Outcomes

CO1	Apply the Knowledge of architectural features and instructions of 32 bit microcontroller ARM Cortex M3-32 bit microcontroller in different application.
CO2	Apply the knowledge gained for Programming ARM Cortex M3 for different applications using C and assembly.
CO3	Analyze the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
CO4	Develop the hardware software co-design and firmware design approaches.
CO5	Apply the knowledge of real time operating system for embedded system applications.

Faculty Incharge

U. ANSHA PRATHIBA

IQAC

HOD

Alva's Institute of Engineering and Technology, Mijar

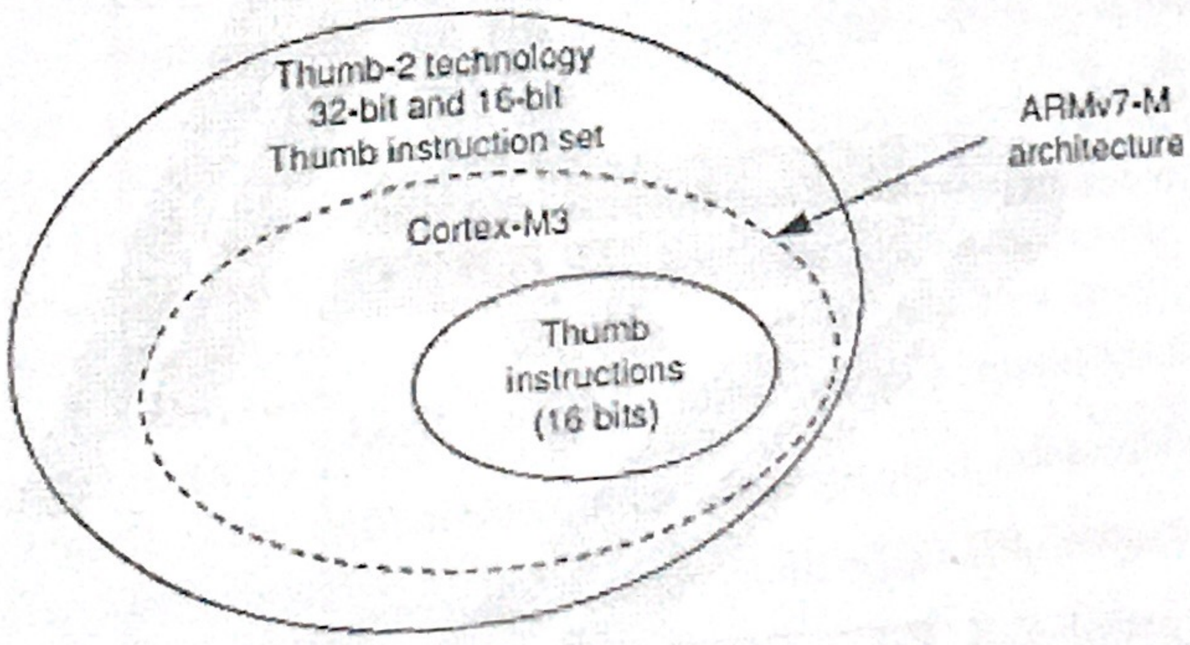
Department of Electronics & Communication Engineering

I – Internal Scheme of Evaluation

Semester: 6th Semester
Subject: Embedded System-18EC62
Faculty Name: Prof. Ansha Prathiba

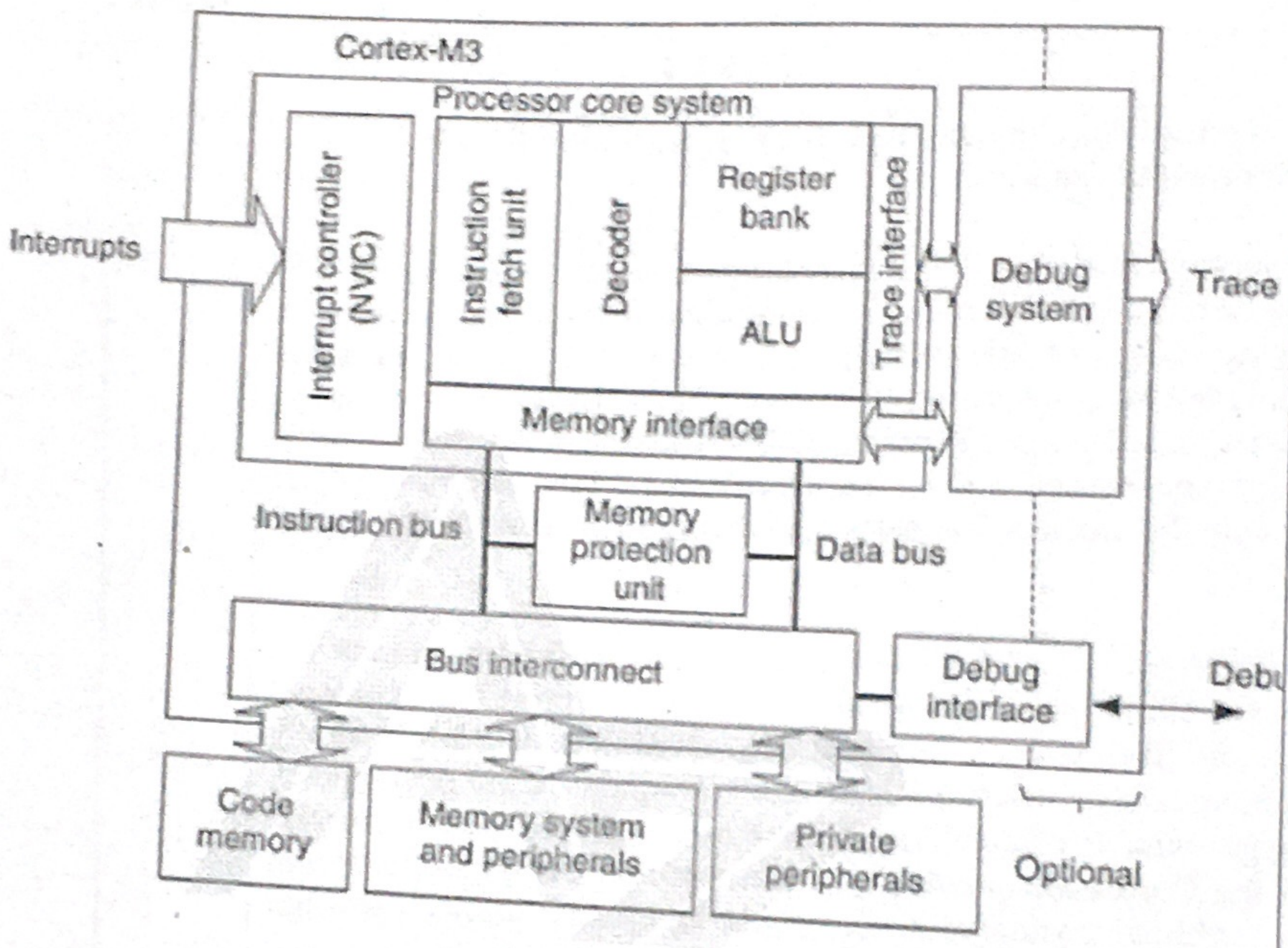
Date: 25/05/2023
Time: 3.00PM to 4.30PM
Max. Marks: 30

Note: Answer one full question from each PART

		Questions	Total Marks	CO	BT/CL
		PART I			
	a	**Briefly explain the Thumb-2 technology and its advantages over thumb instruction set with relevant diagram.** The Thumb-23 technology extended the Thumb Instruction Set Architecture (ISA) into a highly efficient and powerful instruction set that delivers significant benefits in terms of ease of use, code size, and performance (see Figure 1). The extended instruction set in Thumb-2 is a superset of the previous 16-bit Thumb instruction set, with additional 16-bit instructions alongside 32-bit instructions. It allows more complex operations to be carried out in the Thumb state, thus allowing higher efficiency by reducing the number of states switching between ARM state and Thumb state. With support for both 16-bit and 32-bit instructions in the Thumb-2 instruction set, there is no need to switch the processor between Thumb state (16-bit instructions) and ARM state (32-bit instructions). For example, in ARM7 or ARM9 family processors, you might need to switch to ARM state if you want to carry out complex calculations or a large number of conditional operations and good performance is needed, whereas in the Cortex-M3 processor, you can mix 32-bit instructions with 16-bit instructions without switching state, getting high code density and high performance with no extra complexity.	5	1	L1
1		**(3 Mark)**  **(2 Marks)**			

b **With a neat diagram, explain the architecture of ARM cortex M3 microcontroller.**

The Cortex™-M3 is a 32-bit microprocessor. It has a 32-bit data path, a 32-bit register bank, and 32- bit memory interfaces (see Figure 2). The processor has a Harvard architecture, which means that it has a separate instruction bus and data bus. This allows instructions and data accesses to take place at the same time, and as a result of this, the performance of the processor increases because data accesses do not affect the instruction pipeline. This feature results in multiple bus interfaces on Cortex-M3, each with optimized usage and the ability to be used simultaneously. However, the instruction and data buses share the same memory space (a unified memory system). In other words, you cannot get 8 GB of memory space just because you have separate bus interfaces.



(5 Marks)

The Cortex-M3 core contains a decoder for traditional Thumb and new Thumb-2 instructions, an advanced ALU with support for hardware multiply and divide, control logic, and interfaces to the other components of the processor.

- The Cortex-M3 processor is a 32-bit processor, with a 32-bit wide data path, register bank and memory interface. There are 13 general-purpose registers, two stack pointers, a link register, a program counter and a number of special registers including a program status register.
- The Cortex-M3 processor is a memory mapped system with a simple, fixed memory map for up to 4 gigabytes of addressable memory space with predefined, dedicated addresses for code (code space), SRAM(memory space), external memories/devices and internal/external peripherals. There is also a special region to provide for vendor specific addressability.

The MPU is an optional component of the Cortex-M3 processor that can improve

		the reliability of an embedded system by protecting critical data used by the operating system from user applications, separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system. □ The highly configurable NVIC is an integral part of the Cortex-M3 processor and provides the processor's outstanding interrupt handling abilities. In its standard implementation it supplies a NonMaskable Interrupt (NMI) and 32 general purpose physical interrupts with 8 levels of pre-emption priority. It can be configured to anywhere between 1 and 240 physical interrupts with up to 256 levels of priority though simple synthesis choices. □ The debug access into a Cortex-M3 processor based system is through the Debug Access Port (DAP) that can be implemented as either a Serial Wire Debug Port (SW-DP) for a two-pin (clock and data) Interface or a Serial Wire JTAG Debug Port (SWJ-DP) that enables either JTAG or SW protocol to be used. The SWJ-DP defaults to JTAG mode on power reset and can be made to switch protocols with a specific control sequence provided by the external debug hardware. □ The Cortex-M3 processor bus matrix connects the processor and debug interface to the external buses; the 32-bit AMBA® AHB-Lite based ICode, DCode and System interfaces and the 32-bit AMBA APB™ based Private Peripheral Bus (PPB). The bus matrix also implements unaligned data accesses and bit banding. **(5 Marks)**			
OR					
2	**a**	**What are the various registers in ARM Cortex M3? Specify the function of each of them.** The Cortex-M3 processor has registers R0 through R15. R13 (the stack pointer) is banked, with only one copy of the R13 visible at a time. R0–R12: General-Purpose Registers R0–R12 are 32-bit general-purpose registers for data operations. Some 16-bit Thumb® instructions can only access a subset of these registers (low registers, R0–R7). R13: Stack Pointers The Cortex-M3 contains two stack pointers (R13). They are banked so that only one is visible at a time. The two stack pointers are as follows: 1. Main Stack Pointer (MSP): The default stack pointer, used by the operating system (OS) kernel and exception handlers 2. Process Stack Pointer (PSP): Used by user application code. R14: The Link Register When a subroutine is called, the return address is stored in the link register. R15: The Program Counter The program counter is the current program address. This register can be written to control the program flow. **(5 Marks)**	5	1	L2

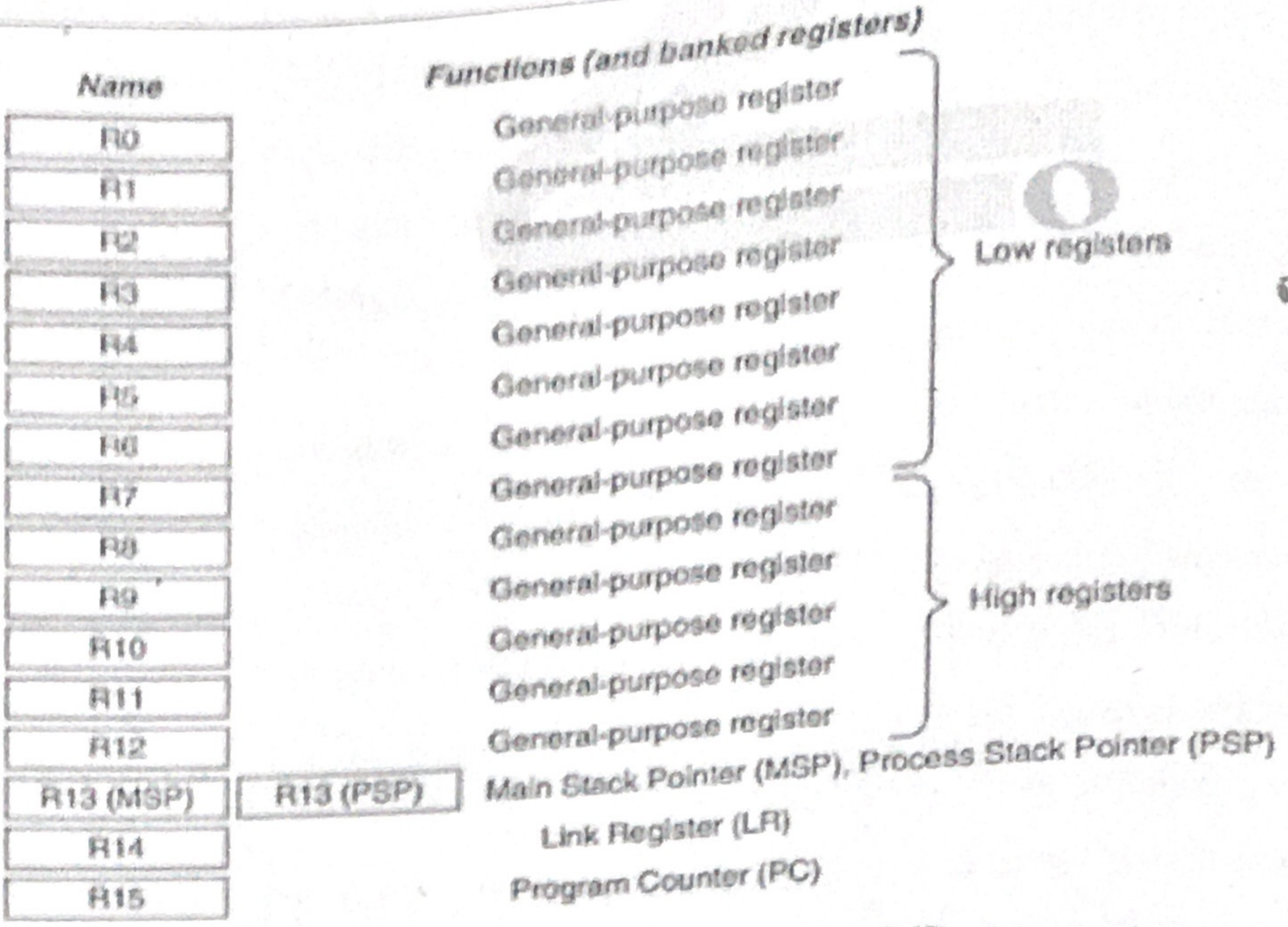
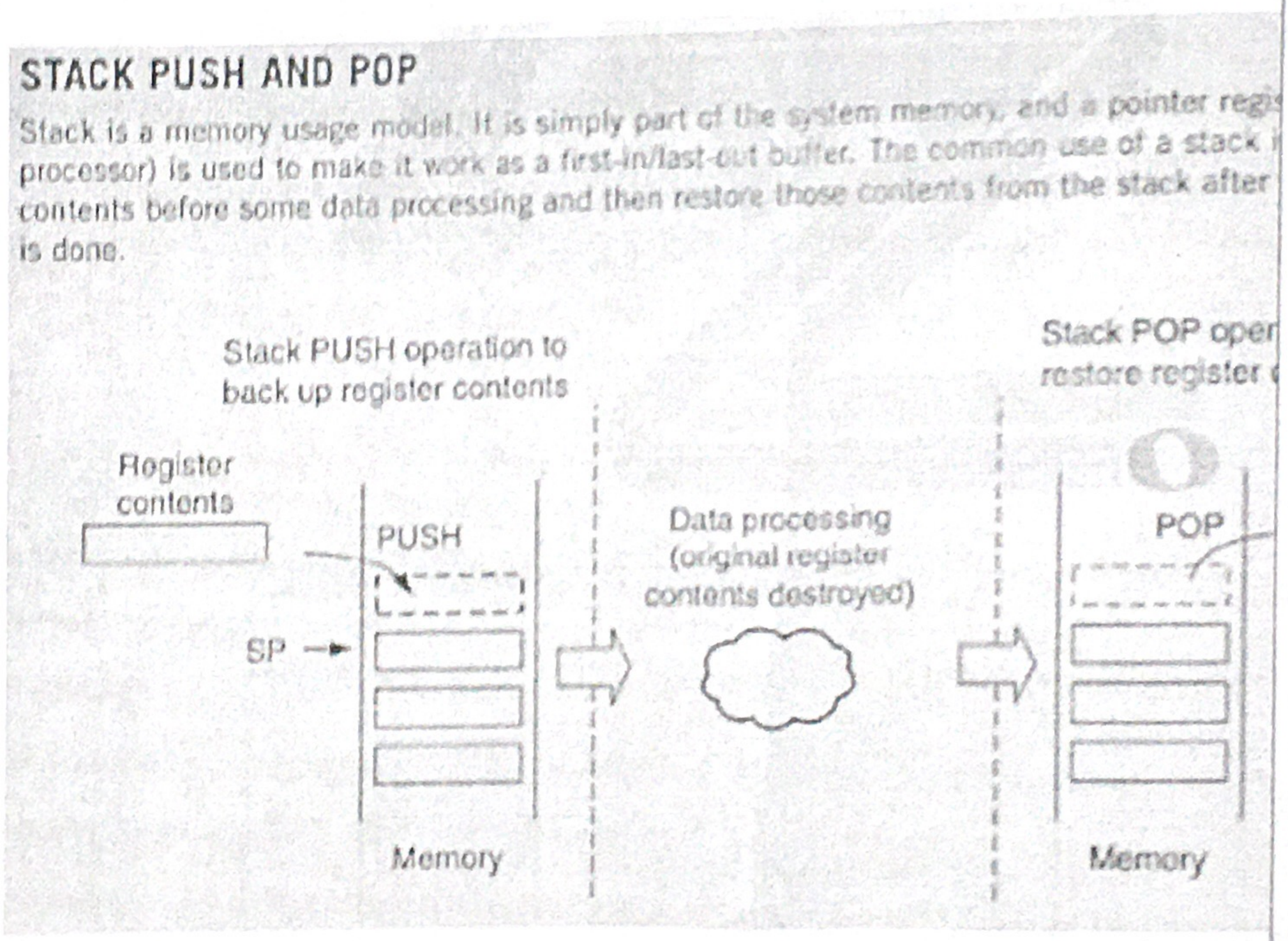


Fig1. 3. Registers in the Cortex-M3

(5 Marks)

b **Explain the stack operations using PUSH and POP instructions in ARM Cortex M3.**

(3 Marks)



(2 Marks)

In the Cortex-M3, the instructions for accessing stack memory are PUSH and POP. The assembly language syntax is as follows (text after each semicolon [;] is a comment):

PUSH {R0} ; R13=R13-4, then Memory[R13] = R0

POP {R0} ; R0 = Memory[R13], then R13 = R13 + 4

PART II

	Explain the features of Nested vector Interrupt controller of ARM cortex M3 The Cortex-M3 processor includes an interrupt controller called the Nested Vectored Interrupt Controller (NVIC). It is closely coupled to the processor core and provides a number of features as follows: Nested interrupt support Vectored interrupt support Dynamic priority changes support Reduction of interrupt latency Interrupt masking **Nested Interrupt Support:** The NVIC provides nested interrupt support. All the external interrupts and most of the system exceptions can be programmed to different priority levels. When an interrupt occurs, the NVIC compares the priority of this interrupt to the current running priority level. If the priority of the new interrupt is higher than the current level, the interrupt handler of the new interrupt will override the current running task. **Vectored Interrupt Support:** The Cortex-M3 processor has vectored interrupt support. When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is located from a vector table in memory. There is no need to use software to determine and branch to the starting address of the ISR. Thus, it takes less time to process the interrupt request. **Dynamic Priority Changes Support**: Priority levels of interrupts can be changed by software during run time. Interrupts that are being serviced are blocked from further activation until the ISR is completed, so their priority can be changed without risk of accidental reentry. **Reduction of Interrupt Latency:** The Cortex-M3 processor also includes a number of advanced features to lower the interrupt latency. These include automatic saving and restoring some register contents, reducing delay in switching from one ISR to another, and handling of late arrival interrupts **Interrupt Masking:** Interrupts and system exceptions can be masked based on their priority level or masked completely using the interrupt masking registers BASEPRI, PRIMASK, and FAULTMASK. They can be used to ensure that time-critical tasks can be finished on time without being interrupt **(1+1+1+1+1=5 Marks)**	5	1	L1
3					
b	How the data definition directives are used in ARM Cortex-M3? Provide example instructions. **(2 Marks)** Assembler Directives Assembler directives are instructions that direct the assembler to do something. Example: EQU(Equate) - Constants can be defined using EQU and then it can be used in program code Ex: NVIC_IRQ_SET EQU 0xE000E100 NVIC_IRQ_ENABLE EQU 0x1 A number of data definition directives are available for instruction of constants inside assembly code. Example: DCI (Define Constant Instruction) - is used to code an instruction if the assembler cannot generate the exact instruction that the user wants and if the user know the binary code for instruction. Ex: DCI 0xBE00 ; Breakpoint (BKPT 0) – 16 bit instruction **(1 mark)** DCB (Define Constant Byte) – Byte size constant values such as characters can be used to define using DCB. Ex: LDR R0, =hellotxt BL printtext Hellotxt DCB —hello\n‖, 0 ; null terminated string **(1 mark)** DCD (Define Constant Data) – Word size constant values to define binary data in assembler code is done through DCD. Ex: LDR R3, = my_num LDR R4, [R3]; my_num DCD 0x12345678 **(1 mark)**	5	2	L2

	c	Explain the data movement instructions in ARM cortex M3. Moving data within processor One of the most basic functions in a processor is transfer of data. In the Cortex-M3, data transfers can be of one of the following types: 1. Moving data between register and register. 2. Moving data between memory and register. 3. Moving data between special register and register. 4. Moving an immediate data value into a register. **(2 marks)** **Moving data between register and register** □ The command to move data between registers is MOV (move). Example MOV R8, R3; moving data from register R3 to register R8. □ Another instruction can generate the negative value of the original data is MVN (move negative). Example MVN R8, R3; The MVN instruction takes the value of R3, performs a bitwise logical NOT operation on the value, and places the result into R8. Table 2.2: Example of MOV and MVN instruction **Moving data between memory and register** i. LDR and STR, LDM and STM ii. PUSH and POP LDR and STR The basic instructions for accessing memory are Load and Store. □ Load (LDR) transfers data from memory to registers, □ Store (STR) transfers data from registers to memory. □ The transfers can be in different data sizes (byte, half word, word, and double word). **Moving data between special register and register** MSR and MRS Instructions MSR and MRS instructions are used to access the special registers in Cortex M3. **Moving an immediate data value into a register** □ Moving immediate data into a register is a common thing to do.□ □ For example, to access a peripheral register, we need to put the address value into a register beforehand.□ □ For small values (8 bits or less), MOVS (move with status update) can be used. Ex: MOV R0, #0xFFH ; Set R0 = 0xFF (hexadecimal) □ MOV R1, #'S' ; Set R1 = ASCII character S Ex: MOVS R0, # 0x12H ; Set R0 to 0x12. □ For a larger value (over 8 bits), we need to use a Thumb-2 move instruction. Ex: MOVW.W R0, #0x789AH ; Set R0 lower half to 0x789AH **(3 Marks)**	5	
	a	Write a short note on the applications of Cortex-M3 Cortex-M3 Processor Applications □ Low-cost microcontrollers: The Cortex-M3 processor is ideally suited for low-cost microcontrollers, which are commonly used in consumer products, from toys to electrical appliances. It is a highly competitive market due to the many well-known 8-bit and 16-bit microcontroller products on the market. Its lower power, high performance, and ease-of- use advantages enable embedded developers to migrate to 32-bit systems and develop products with the ARM architecture. □ Automotive: Another ideal application for the Cortex-M3 processor is in the automotive industry. The Cortex-M3 processor has very high-performance efficiency and low interrupt latency, allowing it to be used in real-time systems. The Cortex-M3 processor supports up to 240 external vectored interrupts, with a built-in interrupt controller with nested interrupt supports and an optional MPU, making it ideal for highly integrated and cost-sensitive automotive applications. □ Data communications: The processor's low power and high efficiency, coupled with instructions in Thumb-2 for bit-field manipulation, make the Cortex-M3 ideal for many communications applications, such as Bluetooth and ZigBee. □ Industrial control: In industrial control applications, simplicity, fast	5	2
	4			

interrupt feature, low interrupt latency, and enhanced fault-handling features make it a strong candidate in this area.

- Consumer products: In many consumer products, a high-performance microprocessor (or several of them) is used. The Cortex-M3 processor, being a small processor, is highly efficient and low in power and supports an MPU enabling complex software to execute while providing robust memory protection.

(1+1+1+1+1=5 Marks)

b **Write a note on LDR and STR Pseudo-Instructions.**

LDR and STR The basic instructions for accessing memory are Load and Store. Load (LDR) transfers data from memory to registers, Store (STR) transfers data from registers to memory. The transfers can be in different data sizes (byte, half word, word, and double word). **(3 Marks)**

Table 2.2: Commonly Used Memory Access Instructions

Example	Description
LDRB Rd, [Rn, #offset]	Read byte from memory location Rn+offset
LDRH Rd, [Rn, #offset]	Read half word from memory location Rn+offset
LDR Rd, [Rn, #offset]	Read word from memory location Rn+offset
LDRD Rd1,Rd2, [Rn, #offset]	Read double word from memory location Rn+offset
STRB Rd, [Rn, #offset]	Store byte to memory location Rn+offset
STRH Rd, [Rn, #offset]	Store half word to memory location Rn+offset
STR Rd, [Rn, #offset]	Store word to memory location Rn+offset
STRD Rd1,Rd2, [Rn, #offset]	Store double word to memory location Rn+offset

Examples on LDR instruction

Before Execution

R1 →

Address	Data
1000002A	0xABCDEF54H
1000002E	0x12345678H
10000032	0x24567893H
10000036	0x88564478H

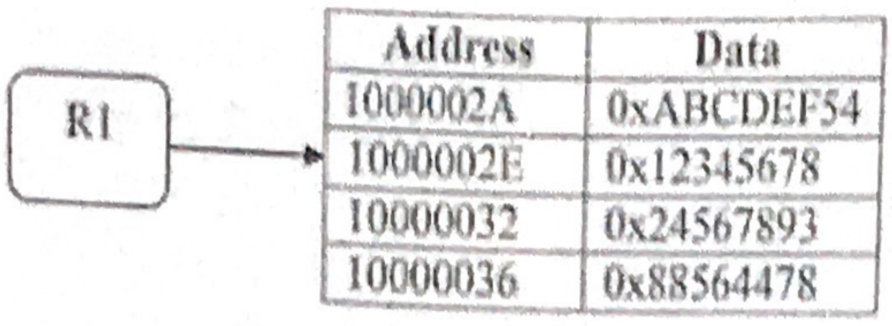
Example 1	Example 2	Example 3	Example 4
LDRB R2, [R1,#4]	LDRH R2, [R1, #4]	LDR R2, [R1, #4]	LDRD R2, R3, [R1, #4]
Operation: R2=mem8[R1+4]	*Operation*: R2= mem16[R1+4]	*Operation*: R2= mem32 [R1+4]	*Operation*: R2, R3= Word from memloc[R1+4], [R1+8] respectively
After Execution: R2=93H	*After Execution:* R2=7893H	*After Execution:* R2=0x24567893H	*After Execution:* R2=0x24567893H, R3=0x88564478H

(1 Mark)

5 1

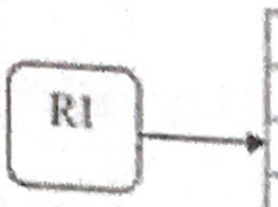
Examples on STR instruction

Before Execution

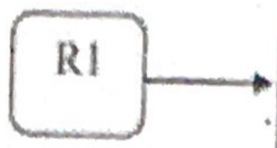


Address	Data
1000002A	0xABCDEF54
1000002E	0x12345678
10000032	0x24567893
10000036	0x88564478

Example 1	Example 2
STRB R2, [R1, #4]	STRH R2, [R1,#4]
Before Execution: R2=0x324565CDH	***Before Execution:*** R2=0x324565CDH
Operation: mem8[R1+4]=R2	***Operation:*** Mem16[R1+4]= R2
After Execution:	***After Execution:***



Address	Data
1000002A	0xABCDEF54H
1000002E	0x12345678H
10000032	0x245678***CDH***
10000036	0x88564478H



Address	Data
1000002A	0xABCDEF54H
1000002E	0x12345678H
10000032	0x245665***CDH***
10000036	0x88564478H

(1 Mark)

c	Describe the debugging support in ARM Cortex M3 **Debugging Support:** **(5 Marks)** The Cortex-M3 processor includes a number of debugging features, such as program execution controls, including halting and stepping, instruction breakpoints, data watchpoints, registers and memory accesses, profiling, and traces. The debugging hardware of the Cortex-M3 processor is based on the CoreSight™ architecture. Unlike traditional ARM processors, the CPU core itself does not have a Joint Test Action Group (JTAG) interface. Instead, a debug interface module is decoupled from the core, and a bus interface called the Debug Access Port (DAP) is provided at the core level. Through this bus interface, external debuggers can access control registers to debug hardware as well as system memory, even when the processor is running. The control of this bus interface is carried out by a Debug Port (DP) device. The DPs currently available are the Serial-Wire JTAG Debug Port (SWJ-DP) (supports the traditional JTAG protocol as well as the Serial-Wire protocol) or the SW-DP (supports the SerialWire protocol only). A JTAG-DP module from the ARM CoreSight product family can also be used. Chip manufacturers can choose to attach one of these DP modules to provide the debug interface. Chip manufacturers can also include an Embedded Trace Macrocell (ETM) to allow instruction trace. Trace information is output via the Trace Port Interface Unit (TPIU), and the debug host (usually a Personal Computer [PC]) can then collect the executed instruction information via external trace capturing hardware.	5	2	L1

(M. ANSHA PRATHIBA)

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

(Accredited by NAAC with A+Grade)

QUESTION PAPER REVIEW REPORT

Continuous Internal Evaluation (CIE) Test: 1 May AY 2022-23

Department: Electronics and Communication Engineering (Accredited by NBA)

Semester/Section: 6th

Max Marks: 30

Course Title: Embedded System

Course Code: 18EC62

Date: 02/06/2023

Faculty: Prof.M.Ansha prathiba

Qn. No.	Course Outcome (CO)	Bloom's Taxonomy Level	Marks
1a	1	2	5
1b	1	2	10
2a	1	2	10
2b	1	3	5
3a	1	2	5
3b	2	4	5
3c	2	3	5
4a	2	3	5
4b	1	3	5
4c	2	4	5
Total Marks			60

BT Level: L1-Remember, L2-Understand, L3 -Apply, L4 -Analyze, L5- Evaluate, L6- Create

Consolidated Marks for Different BT Levels:

BT Level	Marks for Each Level	% of Marks	Remarks
2	30	50%	
3	20	33%	
4	10	17%	

Scrutinizer/Reviewer Remark:

Approved		Approved with Correction		Rejected	
Reason for Rejection					

Name & Signature of the Scrutinizer

Date: 02/06/23

Name & Signature of the IQAC Coordinator

Date: 02/06/23

Signature of Head of the Department

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ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

(Accredited by NAAC with A+ Grade)

Department of Electronics and Communication Engineering (Accredited by NBA)

Continuous Internal Evaluation Test- 1I AY 2022-23

Course Title : Embedded System		Course Code: 18EC62
Date: 16/06/2023	Time:3.00PM to 4.30PM	Semester/Section:6th Sem
Faculty: Mrs.Ansha Prathiba		Max. Marks: 30

Note: Answer ONE FULL question from each Module.

Q. No.		Questions	Marks	COs	BTL
		Part A			
1	a)	Explain the elements of Embedded System with block diagram.	8	3	2
	b)	With a neat diagram explain the organization of CMSIS	7	2	2
		OR			
2	a)	Write the memory map and explain memory access attributes of cortex M3.	7	2	2
	b)	Differentiate between General Computing System and Embedded System.	8	3	2
		Part B			
3	a)	Differentiate between CISC and RISC architecture.	5	3	2
	b)	Classification of Embedded system based on Complexities and Give 2 examples for each category.	5	3	2
	c)	Describe the function of Internal communication interface device I^2C and SPI.	5	4	2
		OR			
4	a)	Explain any five characteristics of Embedded system.	5	3	2
	b)	Explain any five operational quality attributes of embedded system.	5	3	2
	c)	Draw the functional block diagram of Washing machine.	5	4	2

Levels of Bloom's Taxonomy

No.	L1	L2	L3	L4	L5	L6
Level	Remember	Understand	Apply	Analyze	Evaluate	Create

Course Outcomes

CO1	Apply the Knowledge of architectural features and instructions of 32 bit microcontroller ARM Cortex M3-32 bit microcontroller in different application.
CO2	Apply the knowledge gained for Programming ARM Cortex M3 for different applications using C and assembly.
CO3	Analyze the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
CO4	Develop the hardware software co-design and firmware design approaches.
CO5	Apply the knowledge of real time operating system for embedded system applications.

Faculty Incharge

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ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

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QUESTION PAPER REVIEW REPORT

Continuous Internal Evaluation (CIE) Test: 2 June AY 2022-23

Department: Electronics and Communication Engineering (Accredited by NBA)
Semester/Section: 6th
Max Marks: 30

Course Title: Embedded System
Course Code: 18EC62
Date: 23/06/2023

Faculty: M.Ansha Prathiba

Qn. No.	Course Outcome (CO)	Bloom's Taxonomy Level	Marks
1a	3	2	7
1b	2	2	8
2a	2	2	7
2b	3	1	8
3a	3	1	5
3b	3	1	5
3c	4	2	5
4a	3	2	5
4b	3	2	5
4c	4	3	5
Total Marks			60

BT Level: L1-Remember, L2-Understand, L3 -Apply, L4 -Analyze, L5- Evaluate, L6- Create

Consolidated Marks for Different BT Levels:

BT Level	Marks for Each Level	% of Marks	Remarks
1	18	30%	
2	37	61.6%	
3	5	0.08%	
4	0	0	
5	0	0	
6	0	0	

Scrutinizer/Reviewer Remark:

Approved		Approved with Correction		Rejected	
Reason for Rejection					

Name & Signature of the Scrutinizer 22/6/23

Date: 23/6/23

Name & Signature of the IQAC Coordinator

Date: 23/6/23

Signature of Head of the Department Siddesh

USN | | | | | | | | | | |

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

(Accredited by NAAC with A+ Grade)

Department of Electronics and Communication Engineering (Accredited by NBA)

Continuous Internal Evaluation Test- III AY 2022-23

Course Title : Embedded System Continuous Internal Evaluation Test-III EVEN Semester 2022-23		Course Code: 18EC62
Date: 05/07/2023	Time:3.00 to 4.30 PM	Semester/Section: 6th Sem
Faculty: Mrs.Ansha Prathiba		Max. Marks: 30

Note: Answer ONE FULL question from each Module.

Q. No.		Questions	Marks	COs	BTL
		Part A			
1	a)	Explain the Embedded Firmware Design with its disadvantage.	8	4	2
	b)	Describe the Coin operated telephone System with a FSM. Function of States and state transition diagram.	7	4	4
		OR			
2	a)	Explain the Hardware software Co-Design of the Embedded System	8	4	2
	b)	Describe the sequential program model for seat belt warning system along with the operation of the system.	7	4	4
		Part B			
3	a)	Describe the following terms (i) Task (ii) Process (iii)Threads (iv) Deadlock	8	5	2
	b)	Explain the Round Robin Scheduling with Example.	7	5	3
		OR			
4	a)	Describe the techniques used for interfacing and testing of Hardware and Firmware in Embedded system.	8	5	2
	b)	Explain the Embedded system Development Environment.	7	5	3

Levels of Bloom's Taxonomy

No.	L1	L2	L3	L4	L5	L6
Level	Remember	Understand	Apply	Analyze	Evaluate	Create

Course Outcomes

CO1	Apply the Knowledge of architectural features and instructions of 32 bit microcontroller ARM Cortex M3-32 bit microcontroller in different application.
CO2	Apply the knowledge gained for Programming ARM Cortex M3 for different applications using C and assembly.
CO3	Analyze the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
CO4	Develop the hardware software co-design and firmware design approaches.
CO5	Apply the knowledge of real time operating system for embedded system applications.

Faculty Incharge

IQAC

HOD

Dept. of Electronics Communication Alva's Institute of Engg. & Technology Mijar, MOODBIDRI 574 225

H. O. D.
Dept. Of Electronics & Communication
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

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QUESTION PAPER REVIEW REPORT

Continuous Internal Evaluation (CIE) Test: 3 July AY 2022-23

Department: Electronics and Communication Engineering (Accredited by NBA)

Semester/Section: 6th

Max Marks: 30

Course Title: Embedded System

Course Code: 18EC62

Date: 05/07/2023

Faculty: M.Ansha Prathiba

Qn. No.	Course Outcome (CO)	Bloom's Taxonomy Level	Marks
1a	4	2	8
1b	4	4	7
2a	4	2	8
2b	4	4	7
3a	5	2	8
3b	5	3	7
4a	5	2	8
4b	5	3	7
Total Marks			60

BT Level: L1-Remember, L2-Understand, L3 -Apply, L4 -Analyze, L5- Evaluate, L6- Create

Consolidated Marks for Different BT Levels:

BT Level	Marks for Each Level	% of Marks	Remarks
2	32	53.33%	
3	14	23.33%	
4	14	23.33%	

Scrutinizer/Reviewer Remark:

Approved		Approved with Correction		Rejected	
Reason for Rejection					

Name & Signature of the Scrutinizer

Date: 03/07/23

Siddesh

Signature of Head of the Department

H. O. D.
Dept. Of Electronics & Communication
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

Name & Signature of the IQAC Coordinator

Date: 03/07/23

I.Q.A.C
Dept. of Electronics Communication
Alva's Institute of Engg. & Technology
Mijar MOODBIDRI 574 225

Alva's Institute of Engineering and Technology, Mijar

Department of Electronics & Communication Engineering

III – Internal Scheme of Evaluation

Semester: 6th Semester
Subject: Embedded System-18EC62
Faculty Name: Prof. Ansha Prathiba

Date: 05/07/2023
Time: 3.00 PM TO 4.30PM
Max. Marks: 30

Note: Answer one full question from each PART

		Questions	Total Marks	CO	BT/CL
		PART I			
1	a	Super loop based approach - (4 mark) Operating System Based approach - (4 mark)	8	4	2
	b	Explanation - 4 mark State model - 3 mark.	7	4	4
		OR			
2	a	Explanation - 4 mark Computational model - 4 mark.	8	4	2
	b	Explanation - 2 mark. Program - 2 mark flow chart - 2 mark.	7	4	4

	Mark - 2 mark. Dead lock - 2 marks. Process - 2 mark Threads - 2 mark	8	5	2	
	Explanation - 2 mark. Example problem - 5 mark.	7	5	3	
4 a	out of circuit programming - 2 mark In system programming - 2 mark In Application Programming - 2 mark Factory Programmed chip - 2 mark.	8	5	2	
b	Cross Compiler - 2 mark. Simulator - 2 mark. Debugging - 2 mark. Emulator - 1 mark	7	5	3	

Faculty In charge

IQAC

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

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SEMESTER – VI	**Academic Year: 2022 -2023 (Even Semester)**
Course Code: 18EC62	**Course Name:** Embedded Systems
Course Teacher: Mrs.M.Ansha Prathiba	

Assignment 1

Date of Given: 25/05/2023 **Date of Submission: 01/06/2023**

Sl.No	Question	CO	Level
1	Arithmetic and Logic Instruction in ARM Cortex M3 Processors.	2	2
2	CMSIS-Cortex Microcontroller Software Interface Standard	2	2

No	L1	L2	L3	L4	L5	L6
Level	Remember	Understand	Apply	Analyze	Evaluate	Create

Course Outcomes

CO Numbers	Course Outcomes	Blooms Level	Target Level
18EC62.1	Apply the Knowledge of architectural features and instructions of 32 bit microcontroller ARM Cortex M3-32 bit microcontroller in different application.	L1	L2
18EC62.2	Apply the knowledge gained for Programming ARM Cortex M3 for different applications using C and assembly.	L1,L2	L2
18EC62.3	Analyze the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.	L1,L2	L2
18EC62.4	Develop the hardware software co-design and firmware design approaches.	L2,L3	L2
18EC62.5	Apply the knowledge of real time operating system for embedded system applications.	L2,L3	L2

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

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SEMESTER – VI	**Academic Year: 2022 -2023 (Even Semester)**
Course Code: 18EC62	**Course Name:** Embedded Systems
Course Teacher: Mrs.M.Ansha Prathiba	

Assignment 2

Date of Given: 19/06/2023 **Date of Submission: 28/06/2023**

Sl.No	Question	CO	Level
1	Classification of Embedded System	3	2
2	Quality attributes of Embedded System	3	2
3	Communication Interfaces of Embedded system.	3	2

No	L1	L2	L3	L4	L5	L6
Level	Remember	Understand	Apply	Analyze	Evaluate	Create

Course Outcomes

CO Numbers	Course Outcomes	Blooms Level	Target Level
18EC62.1	Apply the Knowledge of architectural features and instructions of 32 bit microcontroller ARM Cortex M3-32 bit microcontroller in different application.	L1	L2
18EC62.2	Apply the knowledge gained for Programming ARM Cortex M3 for different applications using C and assembly.	L1,L2	L2
18EC62.3	Analyze the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.	L1,L2	L2
18EC62.4	Develop the hardware software co-design and firmware design approaches.	L2,L3	L2
18EC62.5	Apply the knowledge of real time operating system for embedded system applications.	L2,L3	L2

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

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SEMESTER – VI	**Academic Year: 2022 -2023 (Even Semester)**
Course Code: 18EC62	**Course Name:** Embedded Systems
Course Teacher: Mrs.M.Ansha Prathiba	

Assignment 3

Date of Given: 28/06/2023 **Date of Submission: 05/07/2023**

Sl.No	Question	CO	Level
1	Hardware Software Co-Design of Embedded System.	4	4
2	Embedded Firmware Design.	4	4

No	L1	L2	L3	L4	L5	L6
Level	Remember	Understand	Apply	Analyze	Evaluate	Create

Course Outcomes

CO Numbers	Course Outcomes	Blooms Level	Target Level
18EC62.1	Apply the Knowledge of architectural features and instructions of 32 bit microcontroller ARM Cortex M3-32 bit microcontroller in different application.	L1	L2
18EC62.2	Apply the knowledge gained for Programming ARM Cortex M3 for different applications using C and assembly.	L1,L2	L2
18EC62.3	Analyze the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.	L1,L2	L2
18EC62.4	Develop the hardware software co-design and firmware design approaches.	L2,L3	L2
18EC62.5	Apply the knowledge of real time operating system for embedded system applications.	L2,L3	L2

Alva's Institute of Engineering & Technology

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Department of Electronics and Communication Engineering

REAL TIME APPLICATION OF EMBEDDED SYSTEM

BATCH.No	USN	NAME	TOPIC
B1	4AL20EC001	Aishwarya A P	**1. Automated teller Machine (ATM)**
	4AL20EC025	Monika. D. B.	
	4AL20EC054	Soumya N	
	4AL20EC029	P V Likhitha	
B2	4AL20EC010	Chethana.M	**2. Robotic vacuum cleaners**
	4AL20EC014	Jyoti P	
	4AL20EC058	Varshini K L	
	4AL20EC059	Veena Talawar	
B3	4AL20EC002	Aishwarya P	**3. Digital Camera**
	4AL20EC007	Bhavana M	
	4AL20EC013	Harshitha D K	
	4AL20EC019	Kshama Tc	
B4	4AL20EC006	Aravinda Jogi	**4. Microwave oven**
	4AL20EC004	Akshay	
	4AL20EC011	Darshan Madival	
	4AL20EC057	Umesh	
B5	4AL20EC005	Akshay Sonar	**5. Air conditioners**
	4AL20EC021	Manjunath Sajjan	
	4AL20EC023	Mohammed S	

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Department of Electronics and Communication Engineering

REAL TIME APPLICATION OF EMBEDDED SYSTEM

	4AL20EC039	Rakesh Sangshetty	
B6	4AL20EC012	Disha H	6. Closed circuit television (CCTV)
	4AL20EC050	Shridevi Rao	
	4AL20EC051	Shruthi	
	4AL20EC053	Shwetha	
B7	4AL20EC015	K.Vijay Bhanu	7. Refrigerators and freezers
	4AL20EC035	Pratham Puthran	
	4AL20EC034	Prashanth VK	
	4AL20EC030	Pavan Kh	
B8	4AL20EC031	Pooja P	8. Printers and scanners
	4AL20EC041	Ramya K	
	4AL20EC040	Rakshitha S	
	4AL20EC052	Shubhashri S	
B9	.4AL20EC028	Padala Sattibabu	9. ECG machines
	4AL20EC027	Nagarjuna GS	
	4AL20EC043	Rohan H	
	4AL20EC046	Sanjay Gk	
B10	4AL20EC018	Krathika	10. Currency counters
	4AL20EC020	Libina Lal	
	4AL20EC038	Preeti G M	

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Department of Electronics and Communication Engineering

REAL TIME APPLICATION OF EMBEDDED SYSTEM

	4AL20EC042	Ranjitha R	
B11	4AL20EC016	Karthik G Shet	**11. Smart card readers**
	4AL20EC033	Prajwal R	
	4AL20EC060	Vinod Raj G N	
	4AL20EC063	Vishwanath	
B12	4AL20EC008	Chaithrashree M G	**12. Smart watches and digital wrist watches**
	4AL20EC048	Santhripti C S	
	4AL20EC061	Vinyashree Jain	
B13	4AL20EC017	Kishan Kumar	**13. Smart phone**
	4AL20EC037	Praveen V	
	4AL20EC045	Sangamesh Biradar	
	4AL20EC056	Srujan	
B14	4AL20EC024	Mokshith	**14. Vending machines**
	4AL20EC036	Prathish G Nayak	
	4AL20EC049	Shravan V U	
	4AL20EC062	Vishanth	
B15	4AL20EC026	Monisha P	**15. Cars**
	4AL20EC032	Prajaktha Poojary	
	4AL20EC055	spoorthi salaskar	

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

6th semester- Academic year 2022-23 (Even)

1st IA AVERAGE MARKS AND ATTENDANCE

#	USN	Student Name	Digital Comunication		Operating system		Embedded System		Antena and Micro Waves		Data Structurtes		Occupational Safety and Health		Remote Sensing [18CV651]		Non Conventional Energy Source		Supply Chain Management	
			Marks	Atts	Marks	Atts	Marks	Atts	Marks	Atts	Marks	Atts	Marks	Atts	Marks	Atts	Marks	Atts	Marks	Atts
1	4AL20EC001	Aishwarya A P	14	79	17	80	16	64	28	78	-	-	AB	18	-	-	-	-	-	-
2	4AL20EC002	Aishwarya Panchagavi	AB	79	AB	73	AB	64	AB	69	-	-	AB	57	-	-	-	-	-	-
3	4AL20EC004	Akshay	29	79	27	73	25	71	30	78	25	81	-	-	-	-	-	-	-	-
4	4AL20EC005	Akshay Sonar	16	87	26	67	18	71	30	78	-	-	-	-	-	-	21	69	-	-
5	4AL20EC006	Aravinda Jogi	9	100	28	93	29	100	30	95	-	-	-	-	25	95	-	-	-	-
6	4AL20EC007	Bhavana M	AB	71	AB	80	AB	64	AB	65	-	-	-	-	-	-	-	-	AB	90
7	4AL20EC008	Chaithrashree M G	22	45	23	13	23	57	30	58	-	-	-	-	-	-	21	50	-	-
8	4AL20EC010	Chethana.M	24	92	28	80	23	78	30	79	-	-	-	-	-	-	-	-	30	85
9	4AL20EC011	Darshan Madival	21	87	27	80	28	85	30	79	25	94	-	-	-	-	-	-	-	-
10	4AL20EC012	Disha H	13	87	26	87	24	92	30	90	-	-	-	-	19	85	-	-	-	-
11	4AL20EC013	Harshitha D K	20	79	29	73	20	78	30	87	-	-	-	-	-	-	8	63	-	-
12	4AL20EC014	Jyoti Phakkirannanavar	14	92	28	67	24	64	27	96	-	-	-	-	-	-	23	63	-	-
13	4AL20EC015	K.Vijay Bhanu	13	58	23	60	24	71	AB	71	7	63	-	-	-	-	-	-	-	-
14	4AL20EC016	Karthik G Shet	17	75	28	80	15	64	27	75	12	75	-	-	-	-	-	-	-	-
15	4AL20EC017	Kishan Kumar	22	87	28	100	26	78	30	92	-	-	-	-	29	92	-	-	-	-
16	4AL20EC018	Krathika	26	87	27	87	19	78	29	87	-	-	-	-	-	-	28	63	-	-
17	4AL20EC019	Kshama Tc	AB	79	AB	87	AB	64	AB	87	-	-	AB	61	-	-	-	-	-	-
18	4AL20EC020	Libina Lal	27	96	29	87	29	85	30	80	-	-	-	-	24	85	-	-	-	-
19	4AL20EC021	Manjunath Sajjan	26	75	28	73	25	57	30	92	-	-	-	-	-	-	27	81	-	-
20	4AL20EC023	Mohammed Sharfuddin	22	66	29	73	28	71	30	70	26	63	-	-	-	-	-	-	-	-
21	4AL20EC024	Mokshith	19	87	28	87	27	85	30	75	-	-	-	-	-	-	28	69	-	-
22	4AL20EC025	Monika. D. B.	11	70	25	60	18	64	27	87	-	-	-	-	-	-	9	57	-	-
23	4AL20EC026	Monisha P	12	58	28	67	24	64	30	87	-	-	-	-	-	-	-	-	29	70
24	4AL20EC027	Nagarjuna GS	10	58	27	73	27	71	28	79	27	88	-	-	-	-	-	-	-	-
25	4AL20EC028	Padala Sattibabu	10	91	25	87	25	85	29	96	0	75	-	-	-	-	-	-	-	-

26	4AL20EC029	P V Likhitha	25	83	25	73	26	71	30	75	-	-	-	-	23	85	-	-	-	-
27	4AL20EC030	Pavan Kh	21	54	26	73	29	50	29	66	23	56	-	-	-	-	-	-	-	-
28	4AL20EC031	Pooja P	21	66	27	73	18	85	30	87	-	-	-	-	-	-	22	50	-	-
29	4AL20EC032	Prajaktha Poojary	AB	96	AB	87	AB	85	AB	70	-	-	AB	74	-	-	-	-	-	-
30	4AL20EC033	Prajwal R	8	75	26	80	18	71	30	62	11	75	-	-	-	-	-	-	-	-
31	4AL20EC034	Prashanth VK	11	83	27	93	18	78	30	64	8	69	-	-	-	-	-	-	-	-
32	4AL20EC035	Pratham Puthran	12	75	25	80	28	93	30	91	-	-	-	-	-	-	-	-	28	80
33	4AL20EC036	Prathish G Nayak	15	100	28	87	29	93	30	83	27	100	-	-	-	-	-	-	-	-
34	4AL20EC037	Praveen Vishwakarma	21	62	28	33	29	57	30	62	-	-	-	-	25	65	-	-	-	-
35	4AL20EC038	Preeti G M	26	87	27	93	24	78	30	66	-	-	-	-	-	-	21	69	-	-
36	4AL20EC039	Rakesh Sangshetty	17	50	25	73	26	78	30	96	-	-	-	-	-	-	22	50	-	-
37	4AL20EC040	Rakshitha S	14	79	26	80	15	64	28	75	-	-	13	31	-	-	-	-	-	-
38	4AL20EC041	Ramya K	25	62	24	67	29	57	30	83	-	-	29	53	-	-	-	-	-	-
39	4AL20EC042	Ranjitha R	23	83	30	87	29	78	30	75	-	-	-	-	18	85	-	-	-	-
40	4AL20EC043	Rohan H	8	41	26	53	29	50	30	50	28	75	-	-	-	-	-	-	-	-
41	4AL20EC045	Sangamesh Biradar	10	37	27	13	25	50	20	62	5	50	-	-	-	-	-	-	-	-
42	4AL20EC046	Sanjay Gk	10	50	26	80	27	93	30	62	22	81	-	-	-	-	-	-	-	-
43	4AL20EC048	Santhripti C S	16	100	26	100	28	100	30	83	-	-	-	-	-	-	20	100	-	-
44	4AL20EC049	Shravan V Upadhyaya	13	79	27	87	21	71	30	41	27	94	-	-	-	-	-	-	-	-
45	4AL20EC050	Shridevi Rao	11	87	24	100	16	93	30	37	-	-	-	-	12	85	-	-	-	-
46	4AL20EC051	Shruthi	28	100	29	93	26	86	30	50	-	-	-	-	18	86	-	-	-	-
47	4AL20EC052	Shubhashri S	23	58	27	60	16	78	30	75	-	-	-	-	-	-	28	50	-	-
48	4AL20EC053	Shwetha	26	100	29	100	26	93	30	79	-	-	-	-	20	85	-	-	-	-
49	4AL20EC054	Soumya N	28	87	28	80	26	78	30	87	-	-	-	-	-	-	30	63	-	-
50	4AL20EC055	spoorthi salaskar	AB	91	AB	93	AB	78	AB	85	-	-	AB	74	-	-	-	-	-	-
51	4AL20EC056	Srujan	15	83	24	87	18	93	30	94	21	100	-	-	-	-	-	-	-	-
52	4AL20EC057	Umesh	15	79	26	87	26	93	29	95	-	-	-	-	-	-	-	-	30	80
53	4AL20EC058	Varshini K L	8	83	27	80	29	78	30	80	-	-	-	-	-	-	27	63	-	-
54	4AL20EC059	Veena Talawar	21	97	25	100	29	78	30	85	-	-	-	-	-	-	21	75	-	-
55	4AL20EC060	Vinod Raj G N	26	33	27	73	28	50	30	60	23	75	-	-	-	-	-	-	-	-
56	4AL20EC061	Vinyashree Jain	17	100	27	93	29	100	30	87	-	-	-	-	-	-	30	100	-	-
57	4AL20EC062	Vishanth	20	87	27	80	29	78	25	80	26	100	-	-	-	-	-	-	-	-
58	4AL20EC063	Vishwanath	18	33	27	53	28	42	29	40	-	-	27	35	-	-	-	-	-	-
No. of students present			53		53		53		52		18		3		10		17		4	
No. of students absent			5		5		5		6		0		5		0		0		1	

No. of students who got 0-12	13	0	0	0	6	0	1	2	0
No. of students who got 13 - 20	18	1	14	1	0	1	4	0	0
No. of students who got 21-30	22	52	39	51	12	2	5	15	4
Faculty name	Mrs.Vijettha T	Dr.Siddesh G	Mrs.Ansha Prathiba	Dr.Guru Prasad	Dr. Sudheer Shetty	Prof.Anusha B Rao	Dr.H.G.Umeshchandra	Prof.Srinivas C S	Prof.Pramod KN
Faculty sign									

Class Co-ordinator

HOD

ALVA'S INSTITUTE OF ENGINEERING TECHNOLOGY

(Unit of Alva's Education Foundation (R), Moodbidri)
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

6th semester- Academic year 2022-23 (Even)

III IA AVERAGE MARKS AND ATTENDANCE

#	USN	Student Name	Digital Comunication (18EC61)		Operating system(18EC641)		Embedded System(18EC62)		Antena and Micro Waves (18EC63)		Data Structurtes (18CS652)		Occupational Safety and Health		Remote Sensing [18CV651]		Non Conventional Energy Source(18ME651)		Supply Chain Management(18ME653)	
			Marks	Atts	Marks	Atts	Marks	Atts	Marks	Atts	Marks	Atts	Marks	Atts	Marks	Atts	Marks	Atts	Marks	Atts
1	4AL20EC001	Aishwarya A P	18	85	16	86	17	82	25	83	-	-	7	86	-	-	-	-	-	-
2	4AL20EC002	Aishwarya Panchagavi	25	90	27	89	26	87	30	83	-	-	16	86	-	-	-	-	-	-
3	4AL20EC004	Akshay	25	90	24	86	28	90	30	86	19	88	-	-	-	-	-	-	-	-
4	4AL20EC005	Akshay Sonar	16	91	25	83	28	85	28	88	-	-	-	-	-	-	30	85	-	-
5	4AL20EC006	Aravinda Jogi	24	98	28	97	29	98	30	100	-	-	-	-	30	90	-	-	-	-
6	4AL20EC007	Bhavana M	15	86	27	91	29	85	30	92	-	-	-	-	-	-	-	-	30	92
7	4AL20EC008	Chaithrashree M G	18	93	27	83	28	82	30	94	-	-	-	-	-	-	30	85	-	-
8	4AL20EC010	Chethana.M	20	95	25	89	26	90	30	92	-	-	-	-	-	-	-	-	30	92
9	4AL20EC011	Darshan Madival	28	93	27	91	26	87	30	96	20	95	-	-	-	-	-	-	-	-
10	4AL20EC012	Disha H	13	90	23	91	29	92	27	94	-	-	-	-	23	86	-	-	-	-
11	4AL20EC013	Harshitha D K	16	100	29	89	27	92	30	92	-	-	-	-	-	-	30	85	-	-
12	4AL20EC014	Jyoti Phakkirannanavar	24	95	28	83	26	87	30	90	-	-	-	-	-	-	30	87	-	-
13	4AL20EC015	K.Vijay Bhanu	25	79	26	83	28	87	30	92	-	-	-	-	-	-	30	85	-	-
14	4AL20EC016	Karthik G Shet	19	88	21	91	29	85	30	92	16	85	-	-	-	-	-	-	-	-
15	4AL20EC017	Kishan Kumar	30	90	27	94	27	92	28	94	-	-	-	-	30	90.0	-	-	-	-
16	4AL20EC018	Krathika	23	90	27	91	29	85	30	88	-	-	-	-	-	-	30	85	-	-
17	4AL20EC019	Kshama Tc	13	90	27	91	27	85	30	90	-	-	18	86	-	-	-	-	-	-
18	4AL20EC020	Libina Lal	23	97	29	91	27	92	30	92	-	-	-	-	29	86.7	-	-	-	-
19	4AL20EC021	Manjunath Sajjan	18	88	29	89	26	80	30	94	-	-	-	-	-	-	30	87	-	-
20	4AL20EC023	Mohammed Sharfuddin	21	85	28	89	26	71	30	80	21	85	-	-	-	-	-	-	-	-
21	4AL20EC024	Mokshith	23	91	26	89	26	85	30	82	-	-	-	-	-	-	30	85	-	-
22	4AL20EC025	Monika. D. B.	5	85	22	75	23	82	14	88	-	-	-	-	-	-	30	85	30	70
23	4AL20EC026	Monisha P	10	78	22	80	29	85	30	92	-	-	-	-	-	-	-	-	-	-
24	4AL20EC027	Nagarjuna GS	14	97	25	86	24	79	30	96	21	85	-	-	-	-	-	-	-	-
25	4AL20EC028	Padala Sattibabu	17	97	26	94	26	95	28	94	-	-	-	-	-	-	30	85	-	-
26	4AL20EC029	P V Likhitha	25	97	29	89	29	85	30	92	-	-	-	-	28	86.7	-	-	-	-
27	4AL20EC030	Pavan Kh	19	88	25	86	24	74	30	90	23	85	-	-	-	-	-	-	-	-
28	4AL20EC031	Pooja P	15	93	26	89	22	87	30	92	-	-	-	-	-	-	30	85	-	-
29	4AL20EC032	Prajaktha Poojary	23	97	29	94	26	95	30	92	-	-	24	91	-	-	-	-	-	-
30	4AL20EC033	Prajwal R	15	88	29	89	28	87	30	94	19	88	-	-	-	-	-	-	-	-

31	4AL20EC034	Prashanth VK	21	93	17	94	29	87	30	85	-	-	-	-	-	-	30	87	-	-
32	4AL20EC035	Pratham Puthran	25	88	25	89	28	87	30	93	-	-	-	-	-	-	-	-	30	85.6
33	4AL20EC036	Prathish G Nayak	23	95	29	91	29	98	30	85	25	95	-	-	-	-	-	-	-	-
34	4AL20EC037	Praveen Vishwakarma	28	85	29	75	29	85	30	85	-	-	-	-	30	87	-	-	-	-
35	4AL20EC038	Preeti G M	21	95	22	94	27	92	30	93	-	-	-	-	-	-	30	92	-	-
36	4AL20EC039	Rakesh Sangshetty	21	97	29	83	28	82	30	96	-	-	-	-	-	-	30	85	-	-
37	4AL20EC040	Rakshitha S	15	91	27	89	29	87	30	83	-	-	26	86	-	-	-	-	-	-
38	4AL20EC041	Ramya K	30	85	29	86	29	85	30	83	-	-	28	86	-	-	-	-	-	-
39	4AL20EC042	Ranjitha R	30	93	29	94	28	82	30	86	-	-	-	-	30	86.7	-	-	-	-
40	4AL20EC043	Rohan H	9	76	29	75	25	71	30	88	23	85	-	-	-	-	-	-	-	-
41	4AL20EC045	Sangamesh Biradar	13	76	25	60	27	82	25	100	-	-	-	-	-	-	-	-	30	82.0
42	4AL20EC046	Sanjay Gk	19	93	24	89	24	87	AB	92	20	85	-	-	-	-	-	-	-	-
43	4AL20EC048	Santhripti C S	18	95	27	97	26	92	30	94	-	-	-	-	-	-	30	94	-	-
44	4AL20EC049	Shravan V Upadhyaya	16	85	29	89	26	74	30	89	19	90	-	-	-	-	-	-	-	-
45	4AL20EC050	Shridevi Rao	12	95	28	94	29	98	30	82	-	-	-	-	27	86.7	-	-	-	-
46	4AL20EC051	Shruthi	28	100	30	97	29	92	30	93	-	-	-	-	28	90.0	-	-	-	-
47	4AL20EC052	Shubhashri S	20	85	29	80	25	87	30	85	-	-	-	-	-	-	30	87	-	-
48	4AL20EC053	Shwetha	25	100	27	97	28	95	30	89	-	-	-	-	29	90	-	-	-	-
49	4AL20EC054	Soumya N	28	90	30	89	28	87	30	93	-	-	-	-	-	-	30	89	-	-
50	4AL20EC055	spoorthi salaskar	22	97	26	94	28	90	30	96	-	-	28	91	-	-	-	-	-	-
51	4AL20EC056	Srujan	15	91	26	91	21	95	30	92	19	95	-	-	-	-	-	-	-	-
52	4AL20EC057	Umesh	15	90	28	94	27	98	30	92	-	-	-	-	-	-	-	-	30	86.8
53	4AL20EC058	Varshini K L	25	88	26	91	29	87	28	94	-	-	-	-	-	-	30	89	-	-
54	4AL20EC059	Veena Talawar	15	97	20	97	27	87	30	85	-	-	-	-	-	-	30	89	-	-
55	4AL20EC060	Vinod Raj G N	14	71	30	83	27	74	30	93	18	85	-	-	-	-	-	-	-	-
56	4AL20EC061	Vinyashree Jain	10	100	15	94	29	92	30	85	-	-	-	-	-	-	23	87	-	-
57	4AL20EC062	Vishanth	14	93	27	91	29	79	25	85	29	90	-	-	-	-	-	-	-	-
58	4AL20EC063	Vishwanath	8	57	29	66	26	61	30	85	-	-	24	86	-	-	-	-	-	-

No. of students present	58	58	58	58	14	8	10	20	6
No. of students absent	0	0	0	1	0	0	0	0	0
No. of students who got 0-12	5	0	0	0	0	1	0	0	0
No. of students who got 13 - 20	27	3	1	1	8	2	0	0	0
No. of students who got 21-30	26	55	57	57	6	5	10	20	6
Faculty name	Mrs.Vijettha T.S	Dr.Siddesh G K	Mrs.Ansha Prathiba	Dr.Guru Prasad	Dr. Sudheer Shetty	Prof. Anusha B Rao	Dr.H.G.Umeshchandra	Prof.Srinivas C S	Prof.Pramod KN
Faculty sign									

Class Co-ordinator

HOD

Accademic Dean

18/7/23

Principal

PRINCIPAL
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225, D.K

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

6th semester- Academic year 2022-23 (Even)

FINAL IA AVERAGE MARKS AND ATTENDANCE

#	USN	Student Name	Digital Comunication (18EC61)		Operating system(18EC641)		Embedded System(18EC62)		Antena and Micro Waves (18EC63)		Data Structurtes (18CS652)		Occupational Safety and Health (18CV653)		Remote Sensing [18CV651]		Non Conventional Energy Source(18ME651)		Supply Chain Management (18ME653)		Embedded System Lab(18ECL66)	Digital Communication Lab18ECL67)	Mini Project
			Marks	Atts	Marks	Atts	Marks	Atts	Mark	Atts	Marks	Atts	Mark	Atts	Marks	Atts	Marks	Atts	Marks	Atts			
1	4AL20EC001	Aishwarya A P	28	85	25	86	30	85	35	85	-	-	22	86	-	-	-	-	-	-	33	26	37
2	4AL20EC002	Aishwarya Panchagavi	37	90	33	89	33	87	40	85	-	-	32	86	-	-	-	-	-	-	40	32	38
3	4AL20EC004	Akshay	38	90	36	86	35	90	39	86	34	88	-	-	-	-	-	-	-	-	35	38	37
4	4AL20EC005	Akshay Sonar	30	91	36	86	32	85	37	88	-	-	-	-	-	-	35	85	-	-	35	37	38
5	4AL20EC006	Aravinda Jogi	35	98	38	97	38	98	40	100	-	-	-	-	38	95	-	-	-	-	40	39	38
6	4AL20EC007	Bhavana M	31	86	38	91	33	85	39	92	-	-	-	-	-	-	-	-	40	92	35	31	38
7	4AL20EC008	Chaithrashree M G	33	93	34	83	33	85	39	94	-	-	-	-	-	-	33	85	-	-	37	29	37
8	4AL20EC010	Chethana.M	35	95	36	89	33	90	40	92	-	-	-	-	-	-	-	-	40	92	35	33	38
9	4AL20EC011	Darshan Madival	37	93	37	91	37	87	40	96	35	95	-	-	-	-	-	-	-	-	40	32	38
10	4AL20EC012	Disha H	29	90	34	91	35	92	35	94	-	-	-	-	32	87	-	-	-	-	37	27	37
11	4AL20EC013	Harshitha D K	31	100	38	89	33	92	39	92	-	-	-	-	-	-	37	85	-	-	40	36	37
12	4AL20EC014	Jyoti Phakkirannanavar	33	95	38	89	36	87	39	90	-	-	-	-	-	-	30	87	-	-	37	34	38
13	4AL20EC015	K.Vijay Bhanu	33	79	35	83	35	87	40	92	-	-	-	-	-	-	36	85	-	-	35	30	37
14	4AL20EC016	Karthik G Shet	31	88	38	91	33	85	39	92	27	85	-	-	-	-	-	-	-	-	36	28	37
15	4AL20EC017	Kishan Kumar	38	90	36	94	35	92	40	94	-	-	-	-	40	87	-	-	-	-	35	40	37
16	4AL20EC018	Krathika	34	90	35	91	35	85	40	88	-	-	-	-	-	-	40	85	-	-	35	38	37
17	4AL20EC019	Kshama Tc	29	90	36	91	35	85	38	90	-	-	32	86	-	-	-	-	-	-	35	38	38
18	4AL20EC020	Libina Lal	37	97	38	91	37	92	40	92	-	-	-	-	37	95	-	-	-	-	35	38	37
19	4AL20EC021	Manjunath Sajjan	35	88	38	89	34	85	40	94	-	-	-	-	-	-	38	87	-	-	40	33	38
20	4AL20EC023	Mohammed Sharfuddin	36	85	38	89	35	85	40	80	36	85	-	-	-	-	-	-	-	-	40	40	38
21	4AL20EC024	Mokshith	34	91	37	89	36	85	40	85	-	-	-	-	-	-	40	85	-	-	37	40	37
22	4AL20EC025	Monika. D. B.	24	85	33	89	30	85	32	88	-	-	-	-	-	-	27	85	-	-	35	28	39
23	4AL20EC026	Monisha P	27	78	33	91	34	85	35	92	-	-	-	-	-	-	-	-	39	70	36	28	32
24	4AL20EC027	Nagarjuna GS	27	97	37	86	34	85	39	96	36	85	-	-	-	-	-	-	-	-	40	31	38
25	4AL20EC028	Padala Sattibabu	29	97	36	94	34	95	38	94	-	-	-	-	-	-	35	85	-	-	35	29	38
26	4AL20EC029	P V Likhitha	37	97	38	89	36	85	40	92	-	-	-	-	37	95	-	-	-	-	37	40	39
27	4AL20EC030	Pavan Kh	34	88	37	86	37	85	40	90	35	85	-	-	-	-	-	-	-	-	40	35	37
28	4AL20EC031	Pooja P	29	93	35	89	36	87	39	92	-	-	-	-	-	-	36	85	-	-	35	34	38
29	4AL20EC032	Prajaktha Poojary	34	97	37	94	35	95	40	92	-	-	37	91	-	-	-	-	-	-	36	30	38
30	4AL20EC033	Prajwal R	27	88	38	89	33	87	40	94	29	88	-	-	-	-	-	-	-	-	40	28	39
31	4AL20EC034	Prashanth VK	30	93	32	94	31	87	39	85	-	-	-	-	-	-	37	87	-	-	40	28	38
32	4AL20EC035	Pratham Puthran	35	88	36	89	34	87	40	93	-	-	-	-	-	-	-	-	39	85.6	37	37	37
33	4AL20EC036	Prathish G Nayak	33	95	38	91	36	98	40	85	38	95	-	-	-	-	-	-	-	-	40	40	37
34	4AL20EC037	Praveen Vishwakarma	36	85	38	75	38	85	40	85	-	-	-	-	39	87	-	-	-	-	36	34	37

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

6th semester- Academic year 2022-23 (Even)

Embedded System -18EC62 Interanl Marks

#	USN	Student Name	Internal Marks				Assignments					Total(40)	Attendence%
			Internal 1	Internal 2	Interanl 3	Average (30)	Ass 1	Ass 2	Ass 3	Application Assignment	Average(10)		
1	4AL20EC001	Aishwarya A P	16	23	20	20	10	10	10	10	10	30	82
2	4AL20EC002	Aishwarya Panchagavi	21	22	26	23	10	10	10	10	10	33	87
3	4AL20EC004	Akshay	25	24	28	26	10	9	9	10	10	35	90
4	4AL20EC005	Akshay Sonar	18	22	28	23	10	9	9	10	10	32	85
5	4AL20EC006	Aravinda Jogi	29	26	29	28	10	10	10	10	10	38	98
6	4AL20EC007	Bhavana M	21	23	29	24	10	8	8	10	9	33	85
7	4AL20EC008	Chaithrashree M G	23	22	28	24	10	8	8	10	9	33	85
8	4AL20EC010	Chethana.M	23	23	26	24	10	8	8	10	9	33	90
9	4AL20EC011	Darshan Madival	28	26	26	27	10	10	10	10	10	37	87
10	4AL20EC012	Disha H	24	22	29	25	10	10	10	9	10	35	92
11	4AL20EC013	Harshitha D K	20	23	27	23	9	10	10	10	10	33	92
12	4AL20EC014	Jyoti Phakkirannanavar	24	27	26	26	10	10	10	10	10	36	87
13	4AL20EC015	K.Vijay Bhanu	24	23	28	25	10	10	10	10	10	35	87
14	4AL20EC016	Karthik G Shet	15	26	29	23	9	9	9	10	9	33	85
15	4AL20EC017	Kishan Kumar	26	22	27	25	10	10	10	10	10	35	92
16	4AL20EC018	Krathika	24	24	29	26	10	9	10	10	10	35	85
17	4AL20EC019	Kshama Tc	24	23	27	25	10	10	10	10	10	35	85
18	4AL20EC020	Libina Lal	29	26	27	27	10	10	10	10	10	37	92
19	4AL20EC021	Manjunath Sajjan	25	22	26	24	10	10	10	10	10	34	85
20	4AL20EC023	Mohammed Sharfuddin	28	22	26	25	10	10	10	10	10	35	85
21	4AL20EC024	Mokshith	27	26	26	26	10	10	10	9	10	36	85

22	4AL20EC025	Monika. D. B.	18	22	23	21	8	8	8	10	9	30	85
23	4AL20EC026	Monisha P	24	27	29	27	5	8	8	10	8	34	85
24	4AL20EC027	Nagarjuna GS	27	23	24	25	10	9	9	8	9	34	85
25	4AL20EC028	Padala Sattibabu	25	22	26	24	10	10	10	8	10	34	95
26	4AL20EC029	P V Likhitha	26	23	29	26	10	10	10	10	10	36	85
27	4AL20EC030	Pavan Kh	29	22	24	27	10	9	9	10	10	37	85
28	4AL20EC031	Pooja P	23	28	27	26	10	10	10	10	10	36	87
29	4AL20EC032	Prajaktha Poojary	25	26	26	26	8	10	10	10	10	35	95
30	4AL20EC033	Prajwal R	18	26	28	24	10	7	7	10	9	33	87
31	4AL20EC034	Prashanth VK	18	23	29	23	9	6	6	10	8	31	87
32	4AL20EC035	Pratham Puthran	28	22	28	26	10	6	6	10	8	34	87
33	4AL20EC036	Prathish G Nayak	29	22	29	27	10	9	9	9	9	36	98
34	4AL20EC037	Praveen Vishwakarma	29	26	29	28	10	9	9	10	10	38	85
35	4AL20EC038	Preeti G M	24	23	27	25	9	10	10	10	10	34	92
36	4AL20EC039	Rakesh Sangshetty	26	25	28	26	10	10	10	10	10	36	85
37	4AL20EC040	Rakshitha S	20	23	29	24	10	9	10	10	10	34	87
38	4AL20EC041	Ramya K	29	26	29	28	10	9	10	10	10	38	85
39	4AL20EC042	Ranjitha R	29	29	29	29	10	10	10	10	10	39	85
40	4AL20EC043	Rohan H	29	24	25	26	8	7	7	8	8	34	71
41	4AL20EC045	Sangamesh Biradar	25	22	27	25	6	6	6	10	7	32	82
42	4AL20EC046	Sanjay Gk	27	26	26	26	7	7	7	8	7	34	87
43	4AL20EC048	Santhripti C S	28	23	26	26	10	10	10	10	10	36	92
44	4AL20EC049	Shravan V Upadhyaya	21	26	26	24	10	9	9	9	9	34	85
45	4AL20EC050	Shridevi Rao	16	23	29	23	10	10	10	9	10	32	98
46	4AL20EC051	Shruthi	28	28	29	28	10	10	10	9	10	38	92
47	4AL20EC052	Shubhashri S	21	27	25	24	10	10	10	10	10	34	87
48	4AL20EC053	Shwetha	29	29	29	29	10	10	10	9	10	39	95
49	4AL20EC054	Soumya N	26	22	28	25	10	10	10	10	10	35	87
50	4AL20EC055	spoorthi salaskar	26	22	28	25	8	10	10	10	10	35	90
51	4AL20EC056	Srujan	18	23	21	21	10	10	10	10	10	31	95
52	4AL20EC057	Umesh	26	27	27	27	10	10	10	10	10	37	98
53	4AL20EC058	Varshini K L	29	22	29	27	5	8	10	10	8	35	87
54	4AL20EC059	Veena Talawar	29	27	27	28	9	9	10	10	10	37	87
55	4AL20EC060	Vinod Raj G N	28	26	27	27	9	10	10	10	10	37	80

56	4AL20EC061	Vinyashree Jain	29	26	29	28	10	10	10	10	10	38	92
57	4AL20EC062	Vishanth	29	23	29	27	10	9	9	9	9	36	85
58	4AL20EC063	Vishwanath	28	26	26	27	10	10	10	10	10	37	75

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Siddesh
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Branch : EC Semester : 6

Sl NO.	USN	18ECL66
1	4AL20EC001	33
2	4AL20EC002	40
3	4AL20EC004	35
4	4AL20EC005	35
5	4AL20EC006	40
6	4AL20EC007	35
7	4AL20EC008	37
8	4AL20EC010	35
9	4AL20EC011	40
10	4AL20EC012	37
11	4AL20EC013	40
12	4AL20EC014	37
13	4AL20EC015	35
14	4AL20EC016	36
15	4AL20EC017	35
16	4AL20EC018	35
17	4AL20EC019	35
18	4AL20EC020	35
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24	4AL20EC027	40
25	4AL20EC028	35
26	4AL20EC029	37
27	4AL20EC030	40
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30	4AL20EC033	40
31	4AL20EC034	40
32	4AL20EC035	37
33	4AL20EC036	40
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35	4AL20EC038	40
36	4AL20EC039	38

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Sl NO.	USN	18ECL66
37	4AL20EC040	38
38	4AL20EC041	40
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52	4AL20EC057	40
53	4AL20EC058	36
54	4AL20EC059	40
55	4AL20EC060	40
56	4AL20EC061	35
57	4AL20EC062	38
58	4AL20EC063	35

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Branch : EC Semester : 6

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1	4AL20EC001	30
2	4AL20EC002	33
3	4AL20EC004	35
4	4AL20EC005	32
5	4AL20EC006	38
6	4AL20EC007	33
7	4AL20EC008	33
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11	4AL20EC013	33
12	4AL20EC014	36
13	4AL20EC015	35
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15	4AL20EC017	35
16	4AL20EC018	35
17	4AL20EC019	35
18	4AL20EC020	37
19	4AL20EC021	34
20	4AL20EC023	35
21	4AL20EC024	36
22	4AL20EC025	30
23	4AL20EC026	34
24	4AL20EC027	34
25	4AL20EC028	34
26	4AL20EC029	36
27	4AL20EC030	37
28	4AL20EC031	36
29	4AL20EC032	35
30	4AL20EC033	33
31	4AL20EC034	31
32	4AL20EC035	34
33	4AL20EC036	36
34	4AL20EC037	38
35	4AL20EC038	34
36	4AL20EC039	36

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Sl NO.	USN	18EC62
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38	4AL20EC041	38
39	4AL20EC042	40
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51	4AL20EC056	31
52	4AL20EC057	37
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54	4AL20EC059	37
55	4AL20EC060	37
56	4AL20EC061	38
57	4AL20EC062	36
58	4AL20EC063	37

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18EC62

Sixth Semester B.E. Degree Examination, July/August 2022
Embedded Systems

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice

Module-1

1 a. With a block Schematic, explain the function of various units in ARM cortex M3 processor architecture, in brief. (10 Marks)
b. Explain any 5 application of ARM cortex M3 based on its features. (05 Marks)
c. With diagram, explain 2 operation modes and 2 privilege levels in cortex M3, when exceptions are to be handled. (05 Marks)

OR

2 a. With tables, describe the various interrupts and exception along with the vector addresses. (10 Marks)
b. Explain Program Status Registers (PSRs) in cortex M3 along with the 2 instructions used for accessing PSRS, with a diagram. (05 Marks)
c. Describe the reset sequence with a diagram. (05 Marks)

Module-2

3 a. Explain the 16 bit instructions: CMP, ASR, SBC and LDMIA, with an example for each. (08 Marks)
b. Describe signed and unsigned saturation instructions with diagram and examples. (08 Marks)
c. Explain IT instruction with an example to convert a High level language instruction to its equivalent assembly instructions in cortex M3. (04 Marks)

OR

4 a. Explain the following 32 bit instructions with an example for each : ADC, BFC, LSL and PUSH. (08 Marks)
b. Describe CMSIS with diagram and its functions, organization and scope. (08 Marks)
c. Write an ALP to add the first 10 integer numbers using cortex M3 processor. (04 Marks)

Module-3

5 a. Describe the elements of an embedded system with a block diagram. (10 Marks)
b. Classify the embedded systems based on the complexities and give 2 examples for each category. (06 Marks)
c. Differentiate between RISC and CISC architectures. (04 Marks)

OR

6 a. Describe the functions of Optocoupler, I2C and IrDA for embedded system. (10 Marks)
b. Explain EPROM, EEPROM, FLASH, DRAM, NVRAM and Sensors required for embedded systems. (06 Marks)
c. Differentiate between Embedded and general computing systems. (04 Marks)

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Module-4

7 a. Describe coin operated telephone system with a FSM, function of states and state transition diagram. **(08 Marks)**

b. Explain any 5 characteristics of embedded systems. **(05 Marks)**

c. With a block schematic, explain the ALP based embedded firmware design with its disadvantages. **(07 Marks)**

OR

8 a. Describe the sequential program model for seat belt warning system along with the operation of the system. **(08 Marks)**

b. Explain any 5 operational quality attributes of embedded systems. **(05 Marks)**

c. With a functional block diagram, explain the working of a washing machine. **(07 Marks)**

Module-5

9 a. With the state transition diagram, structure of a process and memory organization, explain the functions of status and the scheduler function for process management. **(10 Marks)**

b. With an example, describe preemptive SJF scheduling and calculate all the performance factors. **(10 Marks)**

OR

10 a. Describe out-of-circuit programming and In-system-programming. **(10 Marks)**

b. With a block diagram, explain the embedded system development environment with the functions of the components used in brief. **(10 Marks)**

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18EC62

Sixth Semester B.E. Degree Examination, Jan./Feb. 2023
Embedded Systems

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. With a neat diagram, explain the architecture of ARM crotox M_3 processor. **(10 Marks)**

b. Explain two stack model and reset sequence of ARM cortex M_3. **(10 Marks)**

OR

2 a. With the help of neat diagram, explain operation modes and privilege levels of cortex M_3. **(10 Marks)**

b. With the help of register bit format, explain XPSR register in detail. **(06 Marks)**

c. Explain the function of special registers PRIMASK, BASEPRI, CONTROL, FAULTMASK. **(04 Marks)**

Module-2

3 a. Explain the operation of following instructions with syntax and an example for each:
i) ADD.W ii) LDMIA iii) BEQ iv) LSR v) IF-THEN. **(10 Marks)**

b. Explain different rotate and reverse instructions of cortex M_3 with example for each. **(10 Marks)**

OR

4 a. Explain SSAT and USAT saturation instructions with an example. **(05 Marks)**

b. Write an assembly language program to multiply two numbers. **(05 Marks)**

c. With a neat diagram, explain the CMSIS organization, operation, benefits and disadvantages. **(10 Marks)**

Module-3

5 a. Define embedded system. Classify an embedded system based on i) Generation ii) Complexity iii) Triggering. **(10 Marks)**

b. Explain the purpose of an embedded system. **(06 Marks)**

c. Mention the application of an embedded system in different domains. **(04 Marks)**

OR

6 a. Differentiate between RISC and CISC. **(06 Marks)**

b. With a neat interface diagram, explain the onboard I^2C communication bus. **(08 Marks)**

c. Explain the following:
i) Optocoupler ii) Zig-bee iii) Wi-fi, **(06 Marks)**

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Module-4

7 a. Define and explain operational and non operational quality attributes of an embedded system. **(10 Marks)**

b. With a block diagram, explain the role of different components of washing machine. **(07 Marks)**

c. Explain super loop based approach for embedded firmware design. **(03 Marks)**

OR

8 a. With a neat flow diagram, explain high level language source file to machine language conversion. **(06 Marks)**

b. Compare DFG and CDFG models with an example. **(06 Marks)**

c. With the help of FSM model, explain the design and operation of automatic seat belt warning system. **(08 Marks)**

Module-5

9 a. Define the term operating system, with a neat diagram, explain the operating system architecture. **(07 Marks)**

b. Define process, explain in detail the structure, memory organization and state transitions of the process/task. **(07 Marks)**

c. Three processes with process IDs P_1, P_2, P_3 with estimated completion time 10, 5, 7 miliseconds respectively enters the ready queue together. A new process P_4 with estimated completion time 2ms enters the ready queue after 2ms. Calculate the waiting time for all the processes and the turn around time for all the processes. Also, calculate the average waiting time and turn around time. Algorithm used is SJF (Shortest Job First) based preemptive scheduling. Assume all the process contain only CPU operation and no I/O operation are involved. **(06 Marks)**

OR

10 a. Explain the concept of 'deadlock' with a neat diagram. Mention the different conditions which favors a deadlock situation. **(08 Marks)**

b. Write a block schematic of IDE environment for embedded system design and explain their functions in brief. **(08 Marks)**

c. Write a note on IAP [In Application Programming] and in system programming. **(04 Marks)**

* * * * *

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#	USN	Student Name	Conduction & Write up (30)	Viva(5)	Record(5)	Total(40)
1	4AL20EC001	Aishwarya A P	25	3	5	33
2	4AL20EC002	Aishwarya Panchagavi	30	5	5	40
3	4AL20EC004	Akshay	27	3	5	35
4	4AL20EC005	Akshay Sonar	27	3	5	35
5	4AL20EC006	Aravinda Jogi	30	5	5	40
6	4AL20EC007	Bhavana M	27	3	5	35
7	4AL20EC008	Chaithrashree M G	29	3	5	37
8	4AL20EC010	Chethana.M	27	3	5	35
9	4AL20EC011	Darshan Madival	30	5	5	40
10	4AL20EC012	Disha H	29	3	5	37
11	4AL20EC013	Harshitha D K	30	5	5	40
12	4AL20EC014	Jyoti Phakkirannanavar	29	3	5	37
13	4AL20EC015	K.Vijay Bhanu	27	3	5	35
14	4AL20EC016	Karthik G Shet	28	3	5	36
15	4AL20EC017	Kishan Kumar	27	3	5	35
16	4AL20EC018	Krathika	27	3	5	35
17	4AL20EC019	Kshama Tc	27	3	5	35

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18	4AL20EC020	Libina Lal	27	3	5	35
19	4AL20EC021	Manjunath Sajjan	30	5	5	40
20	4AL20EC023	Mohammed Sharfuddin	30	5	5	40
21	4AL20EC024	Mokshith	29	3	5	37
22	4AL20EC025	Monika. D. B.	27	3	5	35
23	4AL20EC026	Monisha P	28	3	5	36
24	4AL20EC027	Nagarjuna GS	30	5	5	40
25	4AL20EC028	Padala Sattibabu	27	3	5	35
26	4AL20EC029	P V Likhitha	29	3	5	37
27	4AL20EC030	Pavan Kh	30	5	5	40
28	4AL20EC031	Pooja P	27	3	5	35
29	4AL20EC032	Prajaktha Poojary	28	3	5	36
30	4AL20EC033	Prajwal R	30	5	5	40
31	4AL20EC034	Prashanth VK	30	5	5	40
32	4AL20EC035	Pratham Puthran	29	3	5	37
33	4AL20EC036	Prathish G Nayak	30	5	5	40
34	4AL20EC037	Praveen Vishwakarma	28	3	5	36
35	4AL20EC038	Preeti G M	30	5	5	40

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36	4AL20EC039	Rakesh Sangshetty	29	4	5	38
37	4AL20EC040	Rakshitha S	29	4	5	38
38	4AL20EC041	Ramya K	30	5	5	40
39	4AL20EC042	Ranjitha R	30	5	5	40
40	4AL20EC043	Rohan H	30	5	5	40
41	4AL20EC045	Sangamesh Biradar	30	5	5	40
42	4AL20EC046	Sanjay Gk	30	5	5	40
43	4AL20EC048	Santhripti C S	29	4	5	38
44	4AL20EC049	Shravan V Upadhyaya	30	5	5	40
45	4AL20EC050	Shridevi Rao	27	3	5	35
46	4AL20EC051	Shruthi	30	5	5	40
47	4AL20EC052	Shubhashri S	28	3	5	36
48	4AL20EC053	Shwetha	30	5	5	40
49	4AL20EC054	Soumya N	29	3	5	37
50	4AL20EC055	spoorthi salaskar	30	5	5	40
51	4AL20EC056	Srujan	30	5	5	40
52	4AL20EC057	Umesh	30	5	5	40
53	4AL20EC058	Varshini K L	28	3	5	36

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54	4AL20EC059	Veena Talawar	30	5	5	40
55	4AL20EC060	Vinod Raj G N	30	5	5	40
56	4AL20EC061	Vinyashree Jain	27	3	5	35
57	4AL20EC062	Vishanth	29	4	5	38
58	4AL20EC063	Vishwanath	27	3	5	35

19/7/24

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18ECL66 Embedded System Lab Viva Questions

1) Mention what are the essential components of embedded system?

Essential components of embedded system includes

- **Hardware**
- Processor
- Memory
- Timers
- I/O circuits
- System application specific circuits
- **Software**
- It ensures the availability of System Memory
- It checks the Processor Speed availability
- The need to limit power lost when running the system continuously
- **Real Time Operating System**
- It runs a process as per scheduling and do the switching from one process to another

2) Mention how I/O devices are classified for embedded system?

The I/O devices of embedded system are classified into two categories

- Serial
- Parallel

3) Explain what are real-time embedded systems?

Real-time embedded systems are computer systems that monitor, respond or control an external environment. This environment is connected to the computer system through actuators, sensors, and other input-output interfaces.

4) Explain what is microcontroller?

The microcontroller is a self-contained system with peripherals, memory and a processor that can be used as embedded system.

5) Mention what is the difference between microprocessor and microcontroller?

Microprocessor is managers of the resources (I/O, memory) which lie outside of its architecture

Microcontroller have I/O, memory, etc. built into it and specifically designed for control

6) What does DMA address will deal with?

DMA address deals with physical addresses. It is a device which directly drives the data and address bus during data transfer. So, it is purely physical address.

7) Explain what is interrupt latency? How can you reduce it?

Interrupt latency is a time taken to return from the interrupt service routine post handling a specific interrupt. By writing minor ISR routines, interrupt latency can be reduced.

8) Mention what are buses used for communication in embedded system?

For embedded system, the buses used for communication includes

- **I2C**: It is used for communication between multiple ICs
- **CAN**: It is used in automobiles with centrally controlled network
- **USB**: It is used for communication between CPU and devices like mouse, etc.

While ISA, EISA, PCI are standard buses for parallel communication used in PCs, computer network devices, etc.

9) List out various uses of timers in embedded system?

Timers in embedded system are used in multiple ways

- Real Time Clock (RTC) for the system
- Initiating an event after a preset time delay
- Initiating an even after a comparison of preset times
- Capturing the count value in timer on an event
- Between two events finding the time interval
- Time slicing for various tasks
- Time division multiplexing
- Scheduling of various tasks in RTOS

10) Explain what is a Watchdog Timer?

A watchdog timer is an electronic device or electronic card that execute specific operation after certain time period if something goes wrong with an electronic system.

11) Explain what is the need for an infinite loop in embedded systems?

Embedded systems require infinite loops for repeatedly processing or monitoring the state of the program. For instance, the case of a program state continuously being verified for any exceptional errors that might just happen during run-time such as memory outage or divide by zero, etc.

12) List out some of the commonly found errors in Embedded Systems?

Some of the commonly found errors in embedded systems are

- Damage of memory devices static discharges and transient current
- Address line malfunctioning due to a short in circuit
- Data lines malfunctioning
- Due to garbage or errors some memory locations being inaccessible in storage
- Inappropriate insertion of memory devices into the memory slots
- Wrong control signals

13) Explain what is semaphore?

A semaphore is an abstract datatype or variable that is used for controlling access, by multiple processes to a common resource in a concurrent system such as multiprogramming operating system. Semaphores are commonly used for two purposes

- To share a common memory space
- To share access to files

14. What do you understand about ARM processors?

ARM processors are a type of microprocessor that is used in many small devices, such as cell phones and PDAs. They are known for their low power consumption and high performance.

15. Can you give me some examples of companies that use and sell ARM processors?

Some of the most popular companies that use ARM processors include Apple, Samsung, and Qualcomm. These companies all manufacture devices that use ARM processors, and they also sell these processors to other companies who then use them in their own devices.

16. What are the primary reasons for using an ARM processor over other types of processors such as Intel x86 or IBM PowerPC?

The main reasons for using an ARM processor are its low power consumption, small size, and low cost. ARM processors are used in a wide variety of devices including cell phones, PDAs, and digital cameras.

17. What are the three main families of ARM microcontrollers?

The three main families of ARM microcontrollers are the Cortex-M series, the Cortex-R series, and the Cortex-A series.

18. Can you explain what bit sizes mean in the context of ARM processors?

The bit size of an ARM processor refers to the width of the data bus. A 32-bit data bus can transfer 4 bytes of data at a time, while a 64-bit data bus can transfer 8 bytes of data. The bit size also determines the maximum addressable memory, so a 32-bit processor can address 4 GB of memory, while a 64-bit processor can address 16 GB of memory.

19. What are the different ARM architectures available?

The different ARM architectures available are:

– ARMv5
– ARMv6
– ARMv7
– ARMv8

20. What type of interrupts can be handled by an ARM processor?

An ARM processor can handle both hardware and software interrupts.

21. What is the purpose of the Link Register (LR) in an ARM processor?

The Link Register is used to store the address of the instruction following the current instruction. This allows the processor to return to the correct location after a subroutine has been executed.

22. What is the MMU present in ARM processors?

The Memory Management Unit is a hardware component present in ARM processors that is responsible for managing memory and providing memory protection. The MMU allows the processor to map virtual memory addresses to physical memory addresses, and it also enforces memory protection by preventing access to memory that is not supposed to be accessible.

23. What is the purpose of the Program Status Register (PSR) in ARM processors?

The PSR is a register that holds status information for the processor. This information includes things like the current processor mode, the condition code flags, and whether interrupts are enabled or disabled.

24. What is the purpose of the floating point coprocessor in ARM processors?

The floating point coprocessor in an ARM processor is responsible for executing all floating point instructions. This includes operations such as addition, subtraction, multiplication, and division. Without this coprocessor, these operations would need to be performed by the main processor, which would be much slower.

25. What is the purpose of the Thumb instruction set in ARM processors?

The Thumb instruction set is designed to provide more efficient code for certain types of operations. It is especially useful for code that is frequently executed or that is time-critical.

EMBEDDED SYSTEM LAB INTERAL EXAM QUESTION

Sub Code: 18ECL66

Exam Hours: 03 Hrs

Max Marks: 50

1. (i) ALP to multiply two 16 bit binary numbers.

   (ii) Display "Hello World" message using Internal UART.

2. (i) ALP to find the sum of first 10 integers.

   (ii) Interface and Control a DC Motor.

3. (i) ALP to find the number of 0's and 1's in a 32 bit data.

   (ii) Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.

4. (i) ALP to determine the given 16 bit number is ODD or EVEN.

   (ii) Demonstrate the use of an external interrupt to toggle an LED On/Off.

5. (i) ALP to write data in RAM.

   (ii) Display the Hex digits 0 to F on a 7-segment LED interface, with an appropriate delay in