ALVA'S
Education Foundation®

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

Information Science and Engineering (ISE)

Course Name: Analog and Digital Electronics

Subject/Course Code: 21CS33

Class: III - A Section

Mr. Sharan Lional Pais

Senior Assistant Professor

Dept. of ISE

2022-23

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Information Science and Engineering

Faculty Details

Name	:	Mr Sharan Lional Pais
Designation	:	Assistant Professor
Qualification	:	BE, M.Tech
Department	:	ISE
Permanent Address	:	Christa Kiran House, Marody Village, Belthangady, 574236, India
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Alva's Institute of Engineering & Technology
Shobhavana Campus, Mijar, Moodbidri, D.K – 574225
Phone: 08258-262725, Fax: 08258-262726

INSTITUTION VISION STATMENT and MISSION STATMENT

VISION STAMENT

"Transformative education by pursuing excellence in engineering and management through enhancing skills to meet the evolving needs of the community"

MISSION STATMENTS

- To bestow quality technical education to imbibe knowledge, creativity and ethos to students community.
- To inculcate the best engineering practices through transformative education.
- To develop a knowledgeable individual for a dynamic industrial scenario.
- To inculcate research, entrepreneurial skills and human values in order to cater the needs of the society.

HOD
H.O.D.
Dept. Of Information Science & Engineering
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

Dr. Dattathreya
NBA Coordinator

Dr. Peter Fernandes
PRINCIPAL
Principal
Alva's Institute of Engg. & Technology,
Mijar, MOODBIDRI - 574 225, D.K.

THE VISION

To Impart quality learning and nurture students to become successful technocrats by achieving excellence in information science and engineering field for addressing the evolving needs of the industry as well as the society.

THE MISSION

M1: To provide quality technical education and research training for preparing competent professionals in the Information technology field.

M2: To provide a suitable infrastructure and environment that inculcates the best engineering practices for the Socio-economic development of society.

M3: To foster the students to become successful technocrats to meet the global competency in the field of IT industry.

M4: To develop entrepreneurship skills with active research and innovation by inculcating ethical values among students.

PROGRAM EDUCATIONAL OBJECTIVES

PEO 1 : . Apply the principles of Information Science & engineering and fundamentals of mathematics toprovide solutions to the societal needs.

PEO 2 : Pursue higher education and engage in research to meet the challenges of the cutting edgetechnologies.

PEO 3 : Design and develop reliable software systems to satisfy the industrial needs throughmultidisciplinary projects

PEO 4 : Able to work in various IT related fields and contribute to the society.

PROGRAM OUTCOMES (PO's)

1. **Engineering knowledge :** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems

2. **Problem analysis :** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences

3. **Design/development of solutions :** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the publichealth and safety, and the cultural, societal, and environmental considerations

4. **Conduct investigations of complex problems :** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions

Sharan L Pais.

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

(A Unit of Alva's Education Foundation)
Shobhavana Campus, Mijar-574225, Moodbidri , D.K - 574225
Phone: 08258-262725, Fax: 08258-262726
Affiliated to VTU Belagavi and Approved by AICTE, New Delhi, Recognized by Govt. of Karnataka

CALENDAR OF EVENTS (ODD SEMESTER 2022-23) BE & MBA

VISION

"Transformative education by pursuing excellence in Engineering and Management through enhancing skills to meet the evolving needs of the community"

MISSION

- To bestow quality technical education to imbibe knowledge, creativity and ethos to students community.
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Week	Month	Days							Activities
		Mon	Tue	Wed	Thu	Fri	Sat	Sun	
1	SEP				1	2	3	4	19th : Commencement of VII Semester BE 22-23 : Student Mentoring 26 – 30 : Technical Talk/Club and Social Activity
2		5	6	7	8	9	10	11	
3		12	13	14	15	16	17	18	
4		19	20	21	22	23	24	25	
		26	27	28	29	30			
6	OCT						1	2	4th : Maha Navami & 5th : Vijaya Dashami 10th : Commencement of V Semester BE 20-21 : Student Mentoring 24th : Naraka Chaturdashi 24 – 29 : Technical Talk/Club and Social Activity 26th : Deepavali 31st : Commencement of III Semester BE
7		3	4	5	6	7	8	9	
8		10	11	12	13	14	15	16	
9		17	18	19	20	21	22	23	
10		24	25	26	27	28	29	30	
11		31							
12	NOV		1	2	3	4	5	6	1st : Kannada Rajyothsava 10th -12th : 1nd IA for VII Semester BE 24-25 – Student Mentoring 20– 25 Technical Talk/Club / Social Activity 28th : Commencement of 3rd Sem MBA
13		7	8	9	10	11	12	13	
14		14	15	16	17	18	19	20	
15		21	22	23	24	25	26	27	
16		28	29	30					
17	DEC				1	2	3	4	8 - 10 : 2nd IA for VII Semester / 1st IA V Semester BE 15 - 17 : 1st IA for BE III Semester BE 22-23 : Student Mentoring 29 - 31 : 3nd IA for VII Semester BE 26 - 31 : Technical Talk/Club / Social Activity **30-31 Second International Conference on Data Analytics & Learning-2022 (DAL'22)** 31 : Last Working Day of VII Semester BE
18		5	6	7	8	9	10	11	
19		12	13	14	15	16	17	18	
		19	20	21	22	23	24	25	
21		26	27	28	29	30	31		
22	JAN-2023							1	2 - 4 : 2nd IA for V Semester BE / 1st IA for MBA 3rd Sem 14- Makara Sankranti 16 -18 : 2nd IA for III Semester BE 20-21 : Student Mentoring 23 - 28 : Technical Talk/Club / Social Activity 24th,25th and 27th : 3nd IA for V Sem BE 26-Republic Day 27 : Last Working Day of V Semester BE
23		2	3	4	5	6	7	8	
24		9	10	11	12	13	14	15	
25		16	17	18	19	20	21	22	
26		23	24	25	26	27	28	29	
27		30	31						
28	FEB-2023			1	2	3	4	5	8 - 10 : 3nd IA for III Semester BE / 2nd IA for MBA 3rd sem 18- Maha Shivaratri 11 : Last Working Day of III Semester BE
29		6	7	8	9	10	11	12	
30		13	14	15	16	17	18	19	
31		20	21	22	23	24	25	26	
32		27	28						
33	MAR-2023			1	2	3	4	5	9 -11 : 3nd IA for MBA 3rd sem 18 : Last Working Day of MBA 3rd Sem
34		6	7	8	9	10	11	12	
35		13	14	15	16	17	18	19	

Approved by IQAC Chairman

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY
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Time Table
DEPARTMENT OF INFORMATION SCIENCE AND ENGINEERING

Academic Year	Scheme	Semester	Section	Class Coordinator	Room No
2022-23	2021	III	A	Ms. Lolakshi P K	301

Time / Day	9.00 To 9.50	9.50 To 10.40	10.40 To 11.00	11.00 To 11.50	11.50 To 12.40	12.40 To 1.40	1.40 To 2.30	2.30 To 3.20	3.30 To 4.50
MON	M3	ADE	BREAK	CO	C++	LUNCH	ADE LAB/ DS LAB		
TUE	APT	OOC LAB/ MO LAB		OOC LAB/ MO LAB			ADE LAB/ DS LAB		
WED	C++	ADE		CO	M3		M3	CIP	APT
THU	CO	DS		APT	CO		DS	ADE	M3
FRI	DS	SCR		CO	ADE		OOC LAB/MO LAB		
SAT	DS	ADE		M3	DS				

Allocation of Subjects

Subjects			Staffs	Staff Code
21MAT31	M3	Transform Calculus, Fourier Series and Numerical Techniques	Mrs. Rashmi R	RR
21CS32	DS	Data Structures and Applications	Mr. Pradeep V	PV
21CS33	ADE	Analog and Digital Electronics	Mr. sharan L Pais	SLP
21CS34	COA	Computer Organization and Architecture	Dr. Manjunath H R	MHR
21CSL35	OOC LAB	Object Oriented Programming with JAVA Laboratory	Ms. Lolakshi P K Dr. Manjunath H R	LPK MHR
21UH36	SCR	Social Connect and Responsibility	Dr. Sapna	SA
21CIP37	CIP	Constitution of India and Professional Ethics	Mr. Ramesh Billava	RB
21CSL381	MO	Mastering Office	Ms. Lolakshi P K	LPK
21CS382	C++	C++ Programming	Ms. Lolakshi P K/Mr. Pradeep Nayak	LPK
21CS832	DS LAB	Data Structures and Applications LAB	Mr.Pradeep V Prof. Sudheer Shetty	SS/PV
21CS33	ADE	Analog and Digital Electronics Lab	Mr. Sharan L Pais /Mr. Nagesh U B	SLP

Time Table Coordinator

H.O.D.
Dept. Of Information Science & Engineering
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

Principal
Alva's Institute of Engg. & Technol
Mijar, MOODBIDRI - 574 225, D.

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Individual Faculty Time Table
DEPARTMENT OF INFORMATION SCIENCE & ENGINEERING

Academic Year	2022-23	Faculty Name	MR. Sharan L Pais
Semester	ODD	Designation	Sr. Assistant Professor

Time / Day	9.00 To 9.50	9.50 To 10.40	11.00 To 11.50	11.50 To 12.40	LUNCH BREAK	1.40 To 2.30	2.30 To 3.20	3.30 To 5.00
MON		ADE				ADE LAB		
TUE	RPA					ADE LAB		
WED		ADE	RPA			AIML LAB		
THU			RPA				ADE	
FRI	RPA	RPA		ADE		PROJECT WORK		
SAT		ADE						

UNITS:	Theory: 20	LAB: 12	Others: 10	TOTAL UNITS: 42

Allocation of Subjects (Subjects with Subject Code)

21CS33	Analog and Digital Electronics
18CS745	Robotic Process Automation Design & Development
18CSL76	ADE LAB, AIML LAB

Additional Responsibilities

Internship coordinator, Training Coordinator, 7th sem Class Coodinator, Alumni Coodinator, Industrial Visit Coodinator, Coders of Alvas club(Main), Infosys Java Trainer (MoU), NAAC Criteria-5 Coordinator

Time Table Coordinator

H.O.D.
Head of the Department
Dept. Of Information Science & Engineering
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E. in Information Science and Engineering

Scheme of Teaching and Examinations2021

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 - 22)

III SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self-Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21MAT31	Transform Calculus, Fourier Series and Numerical Techniques	Maths	3	0	0		03	50	50	100	3
2	IPCC 21CS32	Data Structures and Applications	Any CS Board Department	3	0	2		03	50	50	100	4
3	IPCC 21CS33	Analog and Digital Electronics		3	0	2		03	50	50	100	4
4	PCC 21CS34	Computer Organization and Architecture		3	0	0		03	50	50	100	3
5	PCC 21CSL35	Object Oriented Programming with JAVA Laboratory		0	0	2		03	50	50	100	1
6	UHV 21UH36	Social Connect and Responsibility	Any Department	0	0	1		01	50	50	100	1
7	HSMC 21KSK37/47	Samskrutika Kannada	TD and PSB: HSMC	1	0	0		01	50	50	100	1
	HSMC 21KBK37/47	Balake Kannada										
		OR										
	HSMC 21CIP37/47	Constitution of India and Professional Ethics										
8	AEC 21CS38X/21 CSL38X	Ability Enhancement Course - III	TD: Concerned department PSB: Concerned Board	If offered as Theory Course: 1	0	0		01	50	50	100	1
				If offered as lab. course: 0	0	2		02				
								Total	**400**	**400**	**800**	**18**
9	**Scheduled activities for III to VIII semesters**	NMDC 21NS83	National Service Scheme (NSS)	NSS	All students have to register for any one of the course namely National Service Scheme, Physical Education (PE)(Sports and Athletics) and Yoga with the concerned coordinator of the course during the first week of III semester. The activities shall be carried out from (for 5 semesters) between III semester to VIII semester. SEE in the above courses shall be conducted during VIII semester examinations and the accumulated CIE marks shall be added to the SEE marks. Successful completion of the registered course is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the colander prepared for the NSS, PE and Yoga activities.								
		NMDC 21PE83	Physical Education (PE) (Sports and Athletics)	PE								
		NMDC 21YO83	Yoga	Yoga								

Course prescribed to lateral entry Diploma holders admitted to III semester B.E./B.Tech programs

1	NCMC 21MATDIP31	Additional Mathematics - I	Maths	02	02	--	--	---	100	---	100	0

Note: BSC: Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course.
L –Lecture, **T** – Tutorial, P- Practical/ Drawing, **S** – Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination. **TD**-Teaching Department, **PSB**: Paper Setting department

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and **21KBK37/47** Balake Kannada is for non-Kannada speaking, reading, and writing students.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with Practical's of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech.) 2021-22 may be referred.

III Semester

ANALOG AND DIGITAL ELECTRONICS			
Course Code	**21CS33**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 T + 20 P	Total Marks	100
Credits	04	Exam Hours	03

Course Learning Objectives:

CLO 1. Explain the use of photo electronics devices, 555 timer IC, Regulator ICs and uA741
CLO 2. Make use of simplifying techniques in the design of combinational circuits.
CLO 3. Illustrate combinational and sequential digital circuits
CLO 4. Demonstrate the use of flipflops and apply for registers
CLO 5. Design and test counters, Analog-to-Digital and Digital-to-Analog conversion techniques.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

BJT Biasing: Fixed bias, Collector to base Bias, voltage divider bias

Operational Amplifier Application Circuits: Peak Detector, Schmitt trigger, Active Filters, Non-Linear Amplifier, Relaxation Oscillator, Current-to-Voltage and Voltage-to-Current Converter, Regulated Power Supply Parameters, adjustable voltage regulator, D to A and A to D converter.

Textbook 1: Part A: Chapter 4 (Sections 4.2, 4.3, 4.4), Chapter 7 (Sections 7.4, 7.6 to 7.11), Chapter 8 (Sections 8.1 and 8.5), Chapter 9.

Laboratory Component:

1. Simulate BJT CE voltage divider biased voltage amplifier using any suitable circuit simulator.
2. Using ua 741 Opamp, design a 1 kHz Relaxation Oscillator with 50% duty cycle
3. Design an astable multivibrator circuit for three cases of duty cycle (50%, <50% and >50%) using NE 555 timer IC.
4. Using ua 741 opamap, design a window comparator for any given UTP and LTP.

Teaching-Learning Process	1. Demonstration of circuits using simulation. 2. Project work: Design a integrated power supply and function generator operating at audio frequency. Sine, square and triangular functions are to be generated. 3. Chalk and Board for numerical

Module-2

Karnaugh maps: minimum forms of switching functions, two and three variable Karnaugh maps, four variable Karnaugh maps, determination of minimum expressions using essential prime implicants, Quine-McClusky Method: determination of prime implicants, the prime implicant chart, Petricks method, simplification of incompletely specified functions, simplification using map-entered variables **Textbook 1: Part B: Chapter 5 (Sections 5.1 to 5.4) Chapter 6 (Sections 6.1 to 6.5)**
Laboratory Component: 1. Given a 4-variable logic expression, simplify it using appropriate technique and inplement the same using basic gates.
Teaching-Learning Process 1. Chalk and Board for numerical 2. Laboratory Demonstration
Module-3
Combinational circuit design and simulation using gates: Review of Combinational circuit design, design of circuits with limited Gate Fan-in, Gate delays and Timing diagrams, Hazards in combinational Logic, simulation and testing of logic circuits Multiplexers, Decoders and Programmable Logic Devices: Multiplexers, three state buffers, decoders and encoders, Programmable Logic devices. **Textbook 1: Part B: Chapter 8, Chapter 9 (Sections 9.1 to 9.6)**
Laboratory Component: 1. Given a 4-variable logic expression, simplify it using appropriate technique and realize the simplified logic expression using 8:1 multiplexer IC. $Em(0,2,3,7,8,12,13)$ 2. Design and implement code converter I) Binary to Gray (II) Gray to Binary Code
Teaching-Learning Process 1. Demonstration using simulator 2. Case study: Applications of Programmable Logic device 3. Chalk and Board for numerical
Module-4
Introduction to VHDL: VHDL description of combinational circuits, VHDL Models for multiplexers, VHDL Modules. Latches and Flip-Flops: Set Reset Latch, Gated Latches, Edge-Triggered D Flip Flop 3,SR Flip Flop, J K Flip Flop, T Flip Flop. **Textbook 1: Part B: Chapter 10(Sections 10.1 to 10.3), Chapter 11 (Sections 11.1 to 11.7)**
Laboratory Component: 1. Given a 4-variable logic expression, simplify it using appropriate technique and simulate the same in HDL simulator 2. Realize a J-K Master / Slave Flip-Flop using NAND gates and verify its truth table. And implement the same in HDL.
Teaching-Learning Process 1. Demonstration using simulator 2. Case study: Arithmetic and Logic unit in VHDL 3. Chalk and Board for numerical
Module-5
Registers and Counters: Registers and Register Transfers, Parallel Adder with accumulator, shift registers, design of Binary counters, counters for other sequences, counter design using SR and J K Flip Flops. **Textbook 1: Part B: Chapter 12 (Sections 12.1 to 12.5)**

Laboratory Component:

1. Design and implement a mod-n (n<8) synchronous up counter using J-K Flip-Flop ICs and demonstrate its working.
2. Design and implement an asynchronous counter using decade counter IC to count up from 0 to n (n<=9) and demonstrate on 7-segment display (using IC-7447)

Teaching-Learning Process	1. Demonstration using simulator 2. Project Work: Designing any counter, use LED / Seven-segment display to display the output 3. Chalk and Board for numerical

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

CO 1. Design and analyze application of analog circuits using photo devices, timer IC, power supply and regulator IC and op-amp.

CO 2. Explain the basic principles of A/D and D/A conversion circuits and develop the same.

CO 3. Simplify digital circuits using Karnaugh Map, and Quine-McClusky Methods

CO 4. Explain Gates and flip flops and make us in designing different data processing circuits, registers and counters and compare the types.

CO 5. Develop simple HDL programs

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Practical Sessions need to be assessed by appropriate rubrics and viva-voce method. This will contribute to **20 marks**.

- Rubrics for each Experiment taken average for all Lab components – 15 Marks.
- Viva-Voce– 5 Marks (more emphasized on demonstration topics)

The sum of three tests, two assignments, and practical sessions will be out of 100 marks and will be **scaled down to 50 marks**

(to have a less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper has to be designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question

papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks. Marks scored shall be proportionally reduced to 50 marks
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module

Suggested Learning Resources:

Textbooks

1. Charles H Roth and Larry L Kinney, Raghunandan G H Analog and Digital Electronics, Cengage Learning,2019

Reference Books

1. Anil K Maini, Varsha Agarwal, Electronic Devices and Circuits, Wiley, 2012.
2. Donald P Leach, Albert Paul Malvino & Goutam Saha, Digital Principles and Applications, 8th Edition, Tata McGraw Hill, 2015.
3. M. Morris Mani, Digital Design, 4th Edition, Pearson Prentice Hall, 2008.
4. David A. Bell, Electronic Devices and Circuits, 5th Edition, Oxford University Press, 2008

Weblinks and Video Lectures (e-Resources):

1. Analog Electronic Circuits: https://nptel.ac.in/courses/108/102/108102112/
2. Digital Electronic Circuits: https://nptel.ac.in/courses/108/105/108105132/
3. Analog Electronics Lab: http://vlabs.iitkgp.ac.in/be/
4. Digital Electronics Lab: http://vlabs.iitkgp.ac.in/dec

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Real world problem solving - applying the design concepts of oscillator, amplifier, switch, Digital circuits using Opamps, 555 timer, transistor, Digital ICs and design a application like tone generator, temperature sensor, digital clock, dancing lights etc.

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SEMESTER - III [2022 - 23]

Course Code: 21CS33	Course Name: Analog and Digital Electronics

Course Teacher: Mr. SHARAN LIONAL PAIS

Course Outcomes: After studying this course, students will be able to,

CO Numbers	Course Outcomes	Blooms Level	Target Level
21CS33.1	**Explain** various analog circuits with their applications and **realize** them to understand the working.	L2, L3	2
21CS33.2	**Realize** different types of combinational logic circuits by using a bridge mapping techniques.	L2, L3	2
21CS33.3	**Realize** combinational logic circuits with limited Gate fan-in, Operation of Decoders, Encoders, Multiplexers and PLD's.	L2, L3	2
21CS33.4	**Illustrate** combinational logic circuits using HDL simulation and **implement** the working of Sequential Circuit.	L2, L3	2
21CS33.5	**Design** different data processing circuits using flip flops.	L2, L3	2

Program Outcomes (PO)

PO 1 Engineering knowledge	PO 7 Environment and sustainability
PO 2 Problem analysis	PO 8 Ethics
PO 3 Design/development of solutions	PO 9 Individual and team work
PO 4 Conduct investigations of complex problems	PO 10 Communication
PO 5 Modern tool usage	PO 11 Project management and finance
PO 6 The engineer and society	PO 12 Life-long learning

CO-PO/PSO Mapping Matrix

CO#	Program Outcomes/PSOs														
	1	2	3	4	5	6	7	8	9	10	11	12	PSO1	PSO2	PSO3
21CS33.1	2	1	1		2				2			1	2		
21CS33.2	2	2	2		2				2			1	1		
21CS33.3	2	2	2	1	2				2				1		
21CS33.4	2	2	1		2				2				1		1
21CS33.5	2	2	2	1	2				2				1		
SUM	10	9	8	2	10				10			1	6		
AVERAGE	2	1.8	1.6	1	2				2			1	1.2		1

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CO-PO/PSO Mapping Matrix Justification			
CO#	**POs/ PSOs**	**Level**	**Justification**
21CS33.1	PO1	2	Analog concepts and their application contribute to the enrichment of fundamental knowledge analog circuit design in moderately.
	PO2	1	Student will be able to analyze the principles of working of different digital and analog signals in a basic level.
	PO3	1	Students will be practicing the designs like timer circuits in lab by varying its parameters in basic level.
	PO5	2	Students will be simulating the designs using computers to practice various scenarios to the moderate level.
	PO9	2	Hands-on lab practice will be done in groups and assessed based on their demonstration to the moderate level.
	PO12	1	Student will be able to use the fundamentals studies in future for the new approaches in the field.
	PSO1	2	Analog concepts and their application contribute to the enrichment of fundamental knowledge analog circuit design in moderately.
21CS33.2	PO1	2	Basic concepts of logic design contribute to the enhancement of fundamental knowledge in understanding combinational circuits in moderately.
	PO2	2	Fundamental concepts of K-map, QM method etc. will contribute in analysing the problems in moderately.
	PO3	2	Students will learn to solve simplest circuit designs using various methods in a moderate level.
	PO5	2	Students will be simulating the designs using computers to practice various scenarios to the moderate level.
	PO9	2	Hands-on lab practice will be done in groups and assessed based on their demonstration to the moderate level.
	PO12	1	Basic concepts of digital problem solving techniques will contribute in lifelong learning slightly.
	PSO1	1	The study of logic design contributes to the enhancement of fundamental knowledge in understanding combinational circuits in basic level.
21CS33.3	PO1	2	Basic concepts of gate fan-in and gate fan-out will contribute in gaining basic engineering knowledge of digital logic in moderately.
	PO2	2	Solving the combinational circuits through various techniques will contribute in analysing the problems in a moderately.
	PO3	2	Concepts of multiplexer, encoder and PLD's will contribute in designing the solution to the problem in moderately.
	PO4	1	Knowledge of designing combinational circuits will contribute in investigating complex problem in slightly.
	PO5	2	Students will be simulating the designs using computers to practice various scenarios to the moderate level.
	PO9	2	Hands-on lab practice will be done in groups and assessed based on their demonstration to the moderate level.
	PSO1	1	Basic concepts of gate fan-in and gate fan-out will contribute in gaining basic computations of digital logic in low level.
21CS33.4	PO1	2	Basic concepts of VHDL, Flip flops will help to gain engineering knowledge in moderately.
	PO2	2	Concepts HDL implementation will contribute in enhancement of problem analysis in moderately.
	PO3	1	Flip flops and VHDL code for combinational circuits will contribute in designing the solution to the real world problems in slightly.
	PO5	2	Designing of combinational circuits using VHDL models will

			contribute in usage of modern tools in slightly.
	PO9	2	Hands-on lab practice will be done in groups and assessed based on their demonstration to the moderate level.
	PSO1	1	Basic knowledge of computations are needed for designing VHDL modules for Flip flops and other modules.
	PSO3	1	Simple VHDL programs will be designed and practiced by the student.
21CS33.5	PO1	2	Sequential circuits and data processing circuits will contribute in enhancement of computer engineering knowledge in moderately.
	PO2	2	Counter, registers concepts will contribute in enhancement of problem analysis skills in moderately.
	PO3	2	Creating Counters using flip flops will help to improve knowledge of designing the solution to real world problems in moderately.
	PO5	2	Students will be simulating the designs using computers to practice various scenarios to the moderate level.
	PO9	2	Hands-on lab practice will be done in groups and assessed based on their demonstration to the moderate level.
	PO4	1	Data processing circuit design will contribute in enhancement of investigating complex problem in slightly.
	PSO1	1	Basic knowledge of computations are needed for designing data processing circuits.

Course Teacher
Signature with Date

IQAC Member
Signature with Date

IQAC Chairman
Signature with Date

ALVA'S INSTITUTE OF ENGINEERING AND TECHNOLOGY
SHOBHAVANA CAMPUS, MIJAR, MOODBIDRI – 574 225
DEPARTMENT OF INFORMATION SCIENCE & ENGINEERING

Student List III Semester Academic Year 2022-23

SN	USN	NAME	Scheme	Student Contact No.	Parents' Contact No.
1	4AL21IS001	ADITHYA TEJASWI D	2021	8050506719	9008769011
2	4AL21IS002	AFIZA A	2021	9019264613	7338490077
3	4AL21IS003	AISHWARYA SALIMATH	2021	7899763690	9845563690
4	4AL21IS004	AKASH DEVADIGA	2021	6364173400	9845552005
5	4AL21IS005	AMAR B M	2021	7204729412	8762916638
6	4AL21IS006	ANAGHA UDUPA Y N	2021	9844312308	9844957355
7	4AL21IS007	ANANYA	2021	7975075298	9845949878
8	4AL21IS008	ANIRUDH KAMATH K	2021	8951051708	9663521781
9	4AL21IS009	ANKITHA B	2021	8660416756	9901627592
10	4AL21IS010	BHAGYASHREE R PUJARI	2021	7026102732	7090791998
11	4AL21IS011	BHARATH J	2021	8296798156	7022984622
12	4AL21IS012	BHUMIKA SUNIL KULKARNI	2021	8105454535	9663646169
13	4AL21IS013	CHAITRA S KODDADDI	2021	9148559228	9845955698
14	4AL21IS014	CHANDAN M N	2021	7019188873	9448566925
15	4AL21IS015	CHINDAN B V	2021	8123521923	9480775861
16	4AL21IS017	GOWRISH N	2021	9972231189	7019850845
17	4AL21IS018	HARSHITHA B	2021	8217422566	9972557393
18	4AL21IS019	JAHNAVI	2021	6366086852	8861497452
19	4AL21IS020	KARTHIK MADAKARI T P	2021	7676975951	7892714437
20	4AL21IS021	KELVIN DMELLO	2021	9482053631	9632662297
21	4AL21IS022	KOUSHIK ACHAR	2021	9019490821	9535391461
22	4AL21IS023	KRUPASHREE R	2021	8217795878	9448432409
23	4AL21IS024	LAYA R	2021	7338532513	9535590420
24	4AL21IS025	MANIKANTA	2021	8970971950	9980291920
25	4AL21IS026	MANISH K	2021	9916553511	9900595945
26	4AL21IS027	MANJUNATH R	2021	7795347656	9743346343
27	4AL21IS028	MANOJ LOKESH	2021	8197700565	7259604941
28	4AL21IS029	MANOJ M U	2021	7483252909	9008546320
29	4AL21IS030	MOHAMMED ADIL	2021	8197247822	9686590634
30	4AL21IS031	MOHAMMED RIHAN	2021	6366607931	8971644022
31	4AL21IS032	MUHAMMED YAMIN SHARFUDDIN	2021	7760476139	9663184013
32	4AL21IS033	NANDAN S	2021	9353521191	8618811846
33	4AL21IS034	NISHANT KUMAR	2021	8080514081	81781 20395
34	4AL21IS035	PRAGATHI G GOWDA	2021	7892823971	9964411922
35	4AL21IS036	PRAJNA	2021	8296108372	8762419459
36	4AL21IS037	PRAJWAL GOWDA H G	2021	8660385369	9686156512
37	4AL21IS038	PRASHANTH KUMAR B C	2021	9902597044	9980148218
38	4AL21IS039	PREETHAM BYADAGI	2021	9611331938	9618694342
39	4AL21IS040	R SREEJITH	2021	9567915304	9535075747
40	4AL21IS041	RANJITH	2021	9148526772	9148526772

41	4AL21IS042	SANJAY G K	2021	9353970998	8095696638
42	4AL21IS043	SANNIDHI K S	2021	6362062866	9480579237
43	4AL21IS044	SAPTHAMI	2021	9071350440	9880826839
44	4AL21IS045	SARTHAK K JAIN	2021	8088897133	9741814961
45	4AL21IS046	SATEESH DYAVAPPA SATYANNAVAR	2021	8088224753	9731453896
46	4AL21IS047	SATHWIK K D	2021	8088158503	9686328071
47	4AL21IS048	SHARAVI R RAI	2021	7349071195	9449471270
48	4AL21IS049	SHASHIDHAR MAHADEV PATGAR	2021	9148006853	9108355688
49	4AL21IS050	SHRAVAN R POOJARY	2021	9611583129	9480203366
50	4AL21IS051	SHRAVITHA	2021	7019053913	7899088173
51	4AL21IS052	SHREYA RAI	2021	9686271270	9945317010
52	4AL21IS053	SHRUJAN KUMAR H V	2021	9148547977	9902961379
53	4AL21IS054	SOORAJ	2021	9901417471	9535827550
54	4AL21IS055	SRIDEEKSHA G	2021	9110882772	9964183389
55	4AL21IS056	SRIKANTH RAJU SRINIVAS	2021	9902782222	9008621240
56	4AL21IS057	SRUJAN K M	2021	8147456955	9980205655
57	4AL21IS058	SRUSTI P S	2021	7483223006	8453510400
58	4AL21IS059	SUVAN P KEDILAYA	2021	7676513496	9448120375
59	4AL21IS060	SUVARNA ARVINKANTH HARISH	2021	9702721598	9702846240
60	4AL21IS061	SYED SALEHA	2021	8660512716	9945275071
61	4AL21IS062	VASAVI RAI C	2021	7975538949	9448152911
62	4AL21IS063	VITHIKA SHETTY	2021	7411249497	8722694676
63	4AL21IS064	CHANDANA N M	2021	8147837541	9448137541
64	4AL22IS400	ANKITH	2021	6361697620	9945924970
65	4AL22IS401	CHARAN S V	2021	6362236905	9880661614
66	4AL22IS402	CHETAN BYAHATTI	2021	8660688662	7619558244
67	4AL22IS403	LOHITH H	2021	7899328177	7019415431
68	4AL22IS404	NAMRATHA J SHETTY	2021	6366161922	9164563319
69	4AL22IS405	RAHUL P SHETTY	2021	7019842303	9481070199

HoD, Dept. of ISE
(Prof. Sudheer Shetty)

H. O. D.
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USN | | | | | | | | | | |

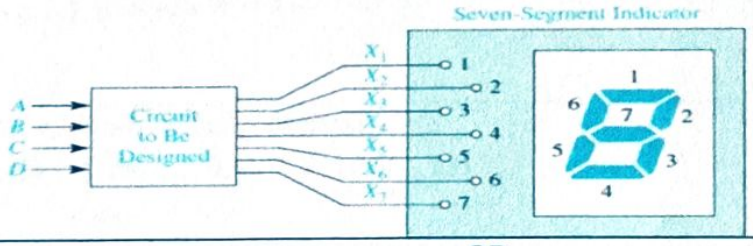
Alva's Institute of Engineering & Technology, Moodbidri

Department of Information Science & Engineering

Continuous Internal Evaluation Test-I ODD Semester 2022-23

Course Title : Analog and Digital Electronics		Course Code: 21CS33
Date: 08/12/2022	Time: 09.30 AM- 10.30 PM	Semester: III
Faculty: Mr. Sharan Lional Pais		Max. Marks: 20

Note: Answer one complete question (a & b) from each part.

Q. No.		Questions	Marks	COs	BTL
		Part - A			
1	a)	Get the simplified SOP and POS expression for the following expression: $F(A, B, C, D) = \sum m(2, 4, 5, 6, 7, 8, 9, 12) + d(0, 14, 15)$	5	CO2	L2
	b)	Simply using Quine-McClusky Method, $F(A, B, C, D) = \sum m(0, 2, 3, 6, 7, 8, 10, 12, 13)$.	5	CO2	L2
		OR			
2	a)	Simply Using Quine-McClusky Method, $F(A, B, C, D) = \sum m(2, 3, 7, 9, 11, 13) + d(1, 10, 15)$	5	CO2	L2
	b)	What is the use of Petrick's Method? Explain with an example.	5	CO2	L2
		Part - B			
3	a)	Explain the detection of Static-0 and Static-1 Hazards with an example.	5	CO3	L2
	b)	Design the missing out circuit, which is expected to drive a 7-segment display: where to display decimal "1": segments 2 and 3 must be high, to display "2": segments 1, 2, 7, 5, 4 are high, so on... 	5	CO3	L2
		OR			
4	a)	Explain Three state Buffers in detail.	5	CO3	L2
	b)	How the design of PLA differs from PAL? Design Full Adder using PAL.	5	CO3	L2

Course Outcomes (COs):

CO1	Explain various analog circuits with their applications and realize them to understand the working	L3
CO2	Realize different types of combinational logic circuits by using a bridge mapping techniques.	L3
CO3	Realize combinational logic circuits with limited Gate fan-in, Operation of Decoders, Encoders, Multiplexers and PLD's.	L3
CO4	Illustrate combinational logic circuits using HDL simulation and implement the working of Sequential Circuit.	L3
CO5	Design different data processing circuits using flip flops.	L3

Sharan 6/12/22.
Subject In-charge

IQAC Member

HOD

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Alva's Institute of Engineering & Technology, Moodbidri

Department of Information Science & Engineering

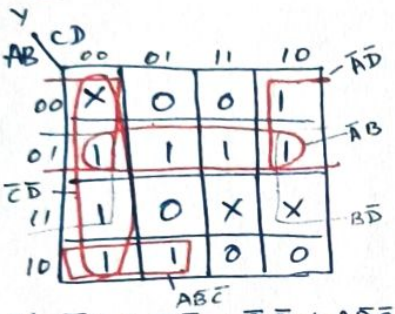
Scheme of Evaluation CIE Test-I ODD Semester 2022-23

Course Title : Analog and Digital Electronics		Course Code: 21CS33
Date: 08/12/2022	Time: 09.30 AM- 10.30 PM	Semester: III
Faculty: Mr. Sharan Lional Pais		Max. Marks: 20

Note: Answer one complete question (a & b) from each part.

Q. No.		Questions	M	CO	BT
		Part - A			
1	a)	Get the simplified SOP and POS expression for the following expression: $F(A, B, C, D) = \sum m(2, 4, 5, 6, 7, 8, 9, 12) + d(0, 14, 15)$	5	CO 2	L2
1	b)	Simply using Quine-McClusky Method, $F(A, B, C, D) = \sum m(0, 2, 3, 6, 7, 8, 10, 12, 13)$.	5	CO 2	L2

S.O.P:

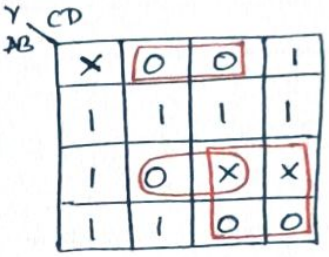


$Y = \bar{A}B + \bar{C}\bar{D} + \bar{A}\bar{D} + AB\bar{C}$

OR

$Y = \bar{A}B + \bar{A}\bar{D} + B\bar{D} + AB\bar{C}$

P.O.S:

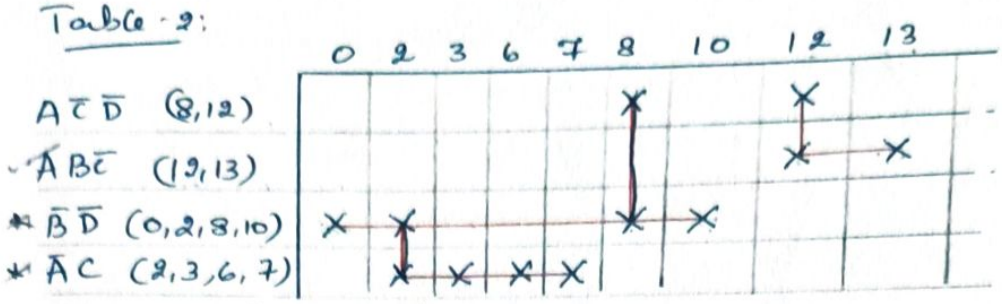


$Y = (\bar{A}+\bar{C}) \cdot (\bar{A}+\bar{B}+\bar{D}) \cdot (A+B+\bar{D})$

Stage 1	Stage 2	Stage 3
A B C D	A B C D	A B C D
0 0 0 0 (0) ✓	0 0 - 0 (0,2) ✓	- 0 - 0 (0,2,8,10) → (1)
0 0 1 0 (2) ✓	- 0 0 0 (0,8) ✓	~~- 0 - 0 (0,8,2,10)~~
1 0 0 0 (8) ✓	0 0 1 - (2,3) ✓	0 - 1 - (2,3,6,7) → (2)
0 0 1 1 (3) ✓	0 - 1 0 (2,6) ✓	~~0 - 1 - (2,6,3,7)~~
0 1 1 0 (6) ✓	- 0 1 0 (2,10) ✓	
1 0 1 0 (10) ✓	1 0 - 0 (8,10) ✓	
1 1 0 0 (12) ✓	1 - 0 0 (8,12) → (3)	
0 1 1 1 (7) ✓	0 - 1 1 (3,7) ✓	
1 1 0 1 (13) ✓	0 1 1 - (6,7) ✓	
	1 1 0 - (12,13) → (4)	

Prime implicants: $A\bar{C}\bar{D}$, $AB\bar{C}$, $\bar{B}\bar{D}$, $\bar{A}C$.

Table-2:



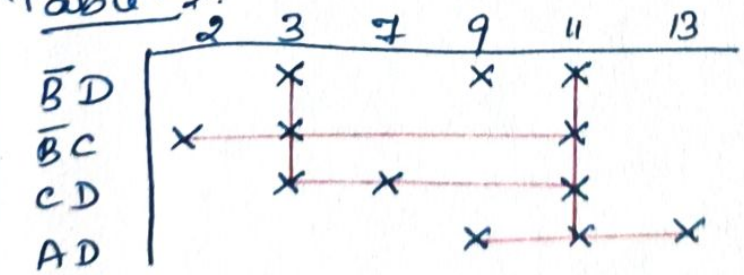
$Y = AB\bar{C} + \bar{B}\bar{D} + \bar{A}C$

2	a)	Simply Using Quine-McClusky Method, $F(A, B, C, D) = \sum m(2, 3, 7, 9, 11, 13) + d(1, 10, 15)$	5	CO 2	L2

Stage 1	Stage 2	Stage 3
A B C D	A B C D	A B C D
0 0 0 1 (1) ✓	0 0 − 1 (1,3) ✓	− 0 − 1 (1,3,9,11)
0 0 1 0 (2) ✓	− 0 0 1 (1,9) ✓	~~− 0 − 1 (1,9,3,11)~~
0 0 1 1 (3) ✓	0 0 1 − (2,3) ✓	− 0 1 − (2,3,10,11)
1 0 0 1 (9) ✓	− 0 1 0 (2,10) ✓	~~− 0 1 − (2,10,3,11)~~
1 0 1 0 (10) ✓	0 − 1 1 (3,7) ✓	− − 1 1 (3,11,7,15)
0 1 1 1 (7) ✓	− 0 1 1 (3,11) ✓	~~− − 1 1 (3,7,11,15)~~
1 0 1 1 (11) ✓	1 0 − 1 (9,11) ✓	1 − − 1 (9,11,13,15)
1 1 0 1 (13) ✓	1 − 0 1 (9,13) ✓	~~1 − − 1 (9,13,11,15)~~
1 1 1 1 (15) ✓	1 0 1 − (10,11) ✓	
	− 1 1 1 (7,15) ✓	
	1 − 1 1 (11,15) ✓	
	1 1 − 1 (13,15) ✓	

Prime implicants are:
$\bar{B}D$, $\bar{B}C$, CD & AD

Table-2:



$Y = \bar{B}C + CD + AD$

2	b)	What is the use of Petrick's Method? Explain with an example.	5	CO 2	L2

Petrick's Method:

① Reduce prime implicant chart by eliminating the essential prime implicants rows & columns.

② Label the rows of the reduced chart as P1, P2...

③ Form the logic function P, consists of P.O.S term

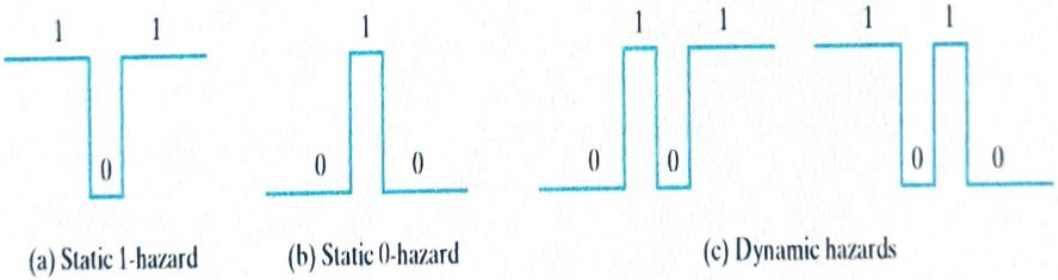
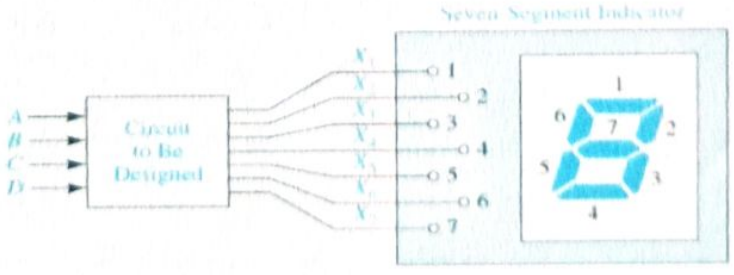
④ Reduce P to a minimum S.O.P by multiplying out & applying $X + XY = X$.

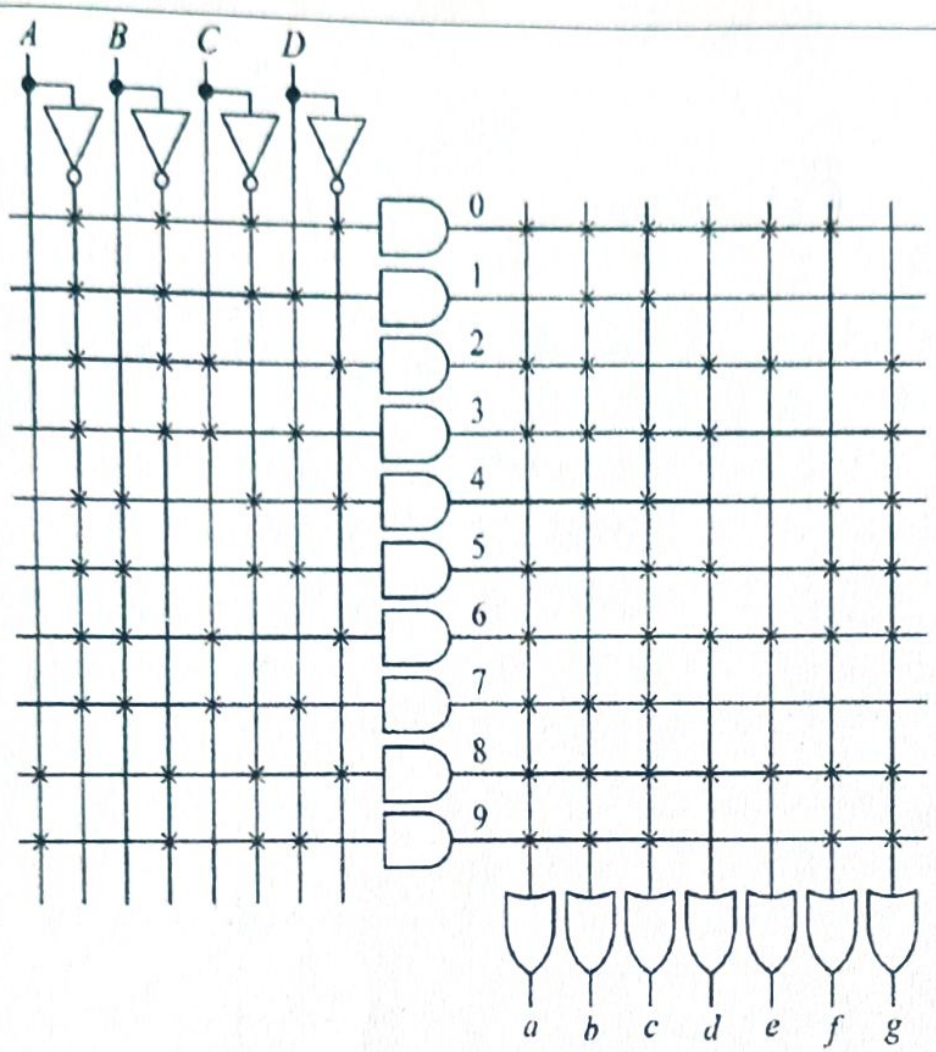
⑤ Determine the min solution by selecting the term which has minimum literals(variables).

⑥ Form the final expression by including essential prime implicants.

Example: Any example with steps followed as mentioned above.

Part - B

3	a)	Explain the detection of Static-0 and Static-1 Hazards with an example.  (a) Static 1-hazard (b) Static 0-hazard (c) Dynamic hazards Detection using adjacent zero or one not covered in same term must be explained using K-maps.	5	CO 3	L2
3	b)	Design the missing out circuit, which is expected to drive a 7-segment display: where to display decimal "1": segments 2 and 3 must be high, to display "2": segments 1, 2, 7, 5, 4 are high, so on...  	5	CO 3	L2

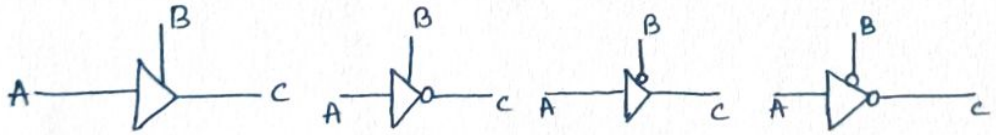


7-segment decoder using PLA

OR

4	**a)**	Explain Three state Buffers in detail.	5	CO 3	L2

Three-state Buffer:



B	A	C
0	0	Z
0	1	Z
1	0	0
1	1	1

B	A	C
0	0	Z
0	1	Z
1	0	0
1	1	1

B	A	C
0	0	0
0	1	1
1	0	Z
1	1	Z

B	A	C
0	0	1
0	1	0
1	0	Z
1	1	Z

explanation to each input & enable input

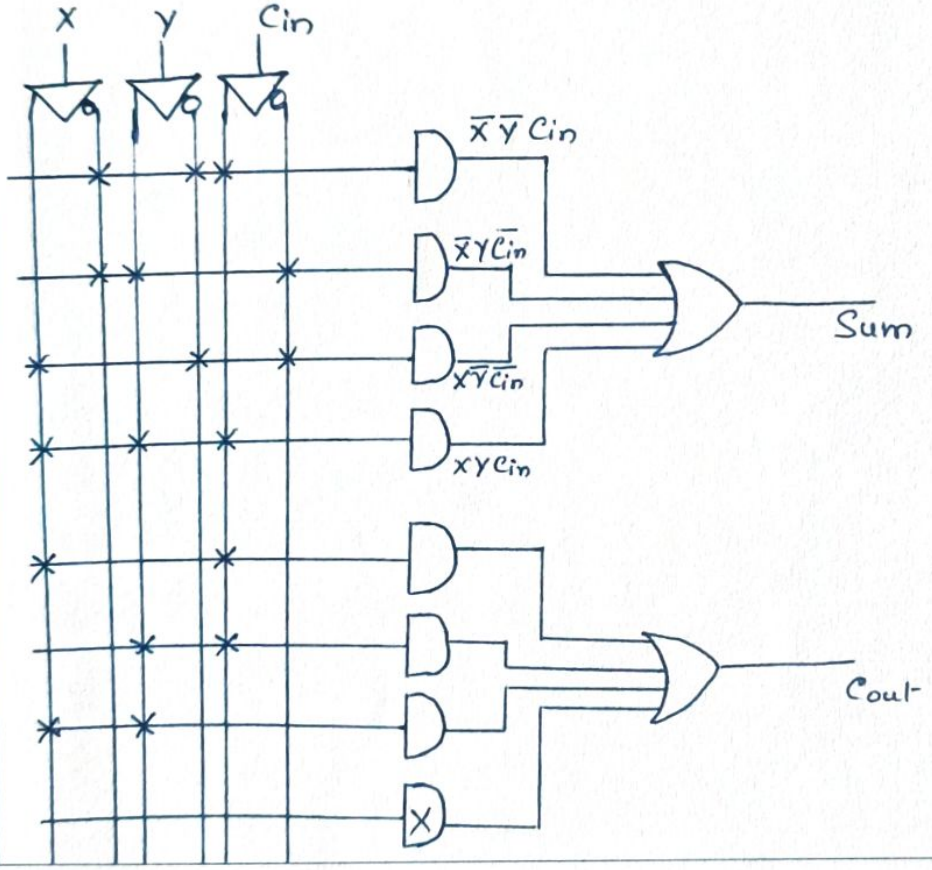
4	**b)**	How the design of PLA differs from PAL? Design Full Adder using PAL.	5	CO 3	L2

PLA:

→ programmable logic arrays
→ programmable array of AND and OR gates.
→ expensive.
→ slow operation.
→ large number of functions can be implemented.

PAL:

→ programmable array logic.
→ programmable array of AND gates & fixed array of OR gates
→ intermediate cost.
→ high speed.
→ provides the limited number of functions.



Subject In-charge

HOD

USN | | | | | | | | | | |

Alva's Institute of Engineering & Technology, Moodbidri

Department of Information Science & Engineering

Continuous Internal Evaluation Test-2 ODD Semester 2022-23

Course Title : Analog and Digital Electronics		Course Code: 21CS33
Date: 24/01/2023	Time: 09.30 AM- 11.00 AM	Semester: III
Faculty: Mr. Sharan Lional Pais		Max. Marks: 20

Note: Answer one complete question from each Module.

Q. No.		Questions	Marks	COs	BTL
		Module – 3			
1	a)	Write VHDL code for 8-to-1 Multiplexer operation.	5	CO4	L3
	b)	Write the block diagram, Output equation(Q+), State transition diagram and Excitation table of JK-ff, SR-ff.	5	CO5	L3
		$J\bar{Q}_n + \bar{K}Q_n$, $S + \bar{R}Q_n$ **OR**			
2	a)	Write VHDL code for 4-bit binary adder using full adder component.	5	CO4	L3
	b)	How J-K Flip-Flop is different from S-R Flip-Flop? Design Master-Slave J-K Flip-Flop, and explain its operation.	5	CO5	L3
		Module - 4			
3	a)	Design and Explain the operation of n-Bit Parallel Adder with Accumulator.	4	CO5	L2
	b)	Design the circuit for Modulo-6 synchronous Up Counter using J-K Flip-Flops.	6	CO5	L3
		OR $B\bar{C}$ $\bar{A}C$ C C			
4	a)	What are Shift Registers? Design and Explain the operation of Parallel-In, Parallel-Out Right Shift Register using Multiplexer.	4	CO5	L2
	b)	Design the synchronous counter for the following sequence using SR- Flip-Flops: → 0 → 3 → 6 → 4 → 2 → C $\bar{B}$ $\bar{B}$ $B\bar{C}$ $\bar{A}\bar{B}$ $B\vert C$	6	CO5	L3

Sharan 16/1/23

Subject In-charge

IQAC Member

HOD

Alva's Institute of Engineering & Technology, Moodbidri

Department of Information Science & Engineering

Scheme of Evaluation - CIE Test-2 ODD Semester 2022-23

Course Title : Analog and Digital Electronics		Course Code: 21CS33
Date: 24/01/2023	Time: 09.30 AM- 11.00 AM	Semester: III
Faculty: Mr. Sharan Lional Pais		Max. Marks: 20

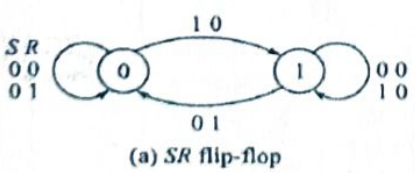
Note: Answer one complete question from each Module.

Q. No.		Questions	Marks	COs	BTL
		Module – 3			
1	a)	Write VHDL code for 8-to-1 Multiplexer operation.	5	CO4	L3
1	b)	Write the block diagram, Output equation(Q+), State transition diagram and Excitation table of JK-ff, SR-ff.	5	CO5	L3

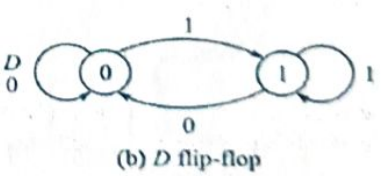
```
entity mux_8x1 is
port (d : in std_logic_vector (0 to 7);
      s : in std_logic_vector (0 to 2);
      o : out std_logic);
end mux_8x1;

architecture mux_arch of mux_8x1 is
  begin
   process (d,s)
    begin
      case s is
            when "000" => o<= d(0);
            when "001" => o<= d(1);
            when "010" => o<= d(2);
            when "011" => o<= d(3);
            when "100" => o<= d(4);
            when "101" => o<= d(5);
            when "110" => o<= d(6);
            when "111" => o<= d(7);
            when others => o<= '0';
       end case;
    end process;
end mux_arch;
```

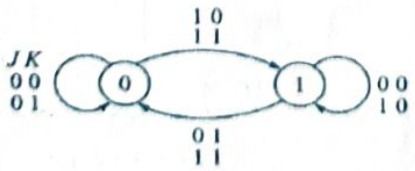
State Transition Diagrams:



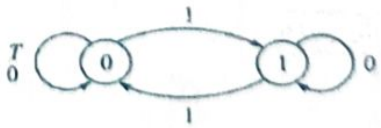
(a) *SR* flip-flop



(b) *D* flip-flop



(c) *JK* flip-flop

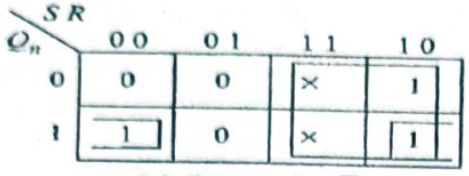


(d) *T* flip-flop

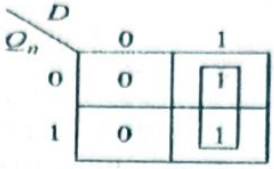
Excitation Table:

$Q_n \rightarrow Q_{n+1}$		S	R	J	K	D	T
0	0	0	×	0	×	0	0
0	1	1	0	1	×	1	1
1	0	0	1	×	1	0	1
1	1	×	0	×	0	1	0

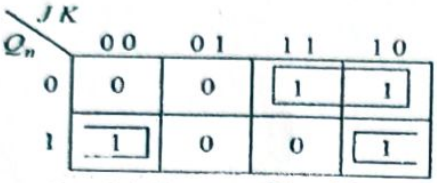
Characteristic equations:



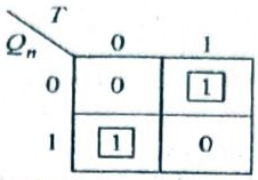
(a) $Q_{n+1} = S + \overline{R}\,Q_n$



(b) $Q_{n+1} = D$



(c) $Q_{n+1} = J\overline{Q}_n + \overline{K}\,Q_n$

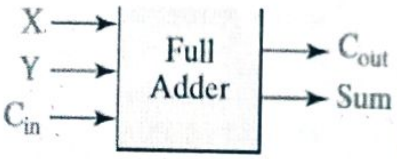


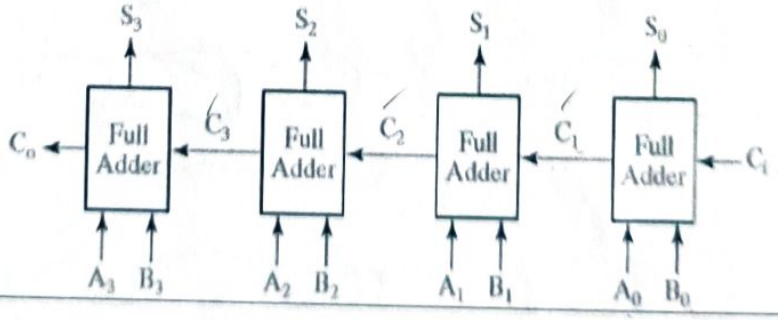
(d) $Q_{n+1} = T\overline{Q}_n + \overline{T}\,Q_n$

OR

2	a)	Write VHDL code for 4-bit binary adder using full adder component.	5	CO4	L3

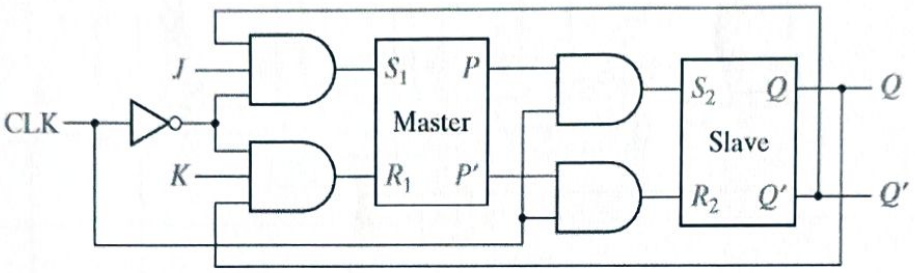
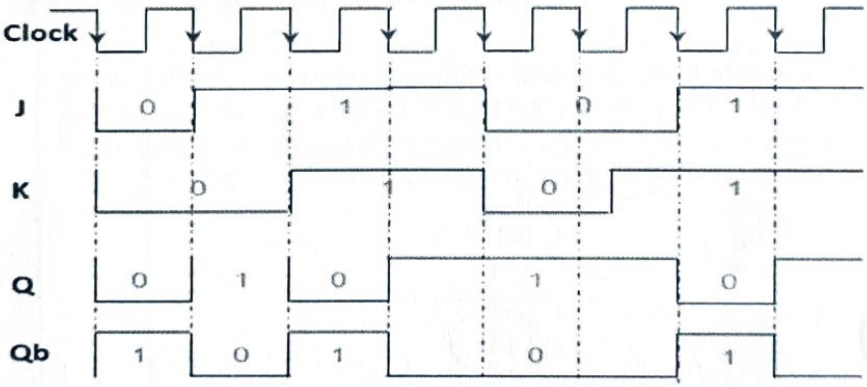
```
--Entity Declaration for a Full Adder Module
entity FullAdder is
    port (X,Y,Cin: in bit;  -- Inputs
          Cout, Sum: out bit); -- Outputs
end FullAdder;
--The operation of the full adder is specified by an architecture
--declaration:
architecture Equations of FullAdder is
begin
   -- concurrent assignment statements
   Sum <= X xor Y xor Cin after 10 ns;
   Cout <= (X and Y) or (X and Cin) or (Y and Cin) after 10 ns;
end Equations;
```



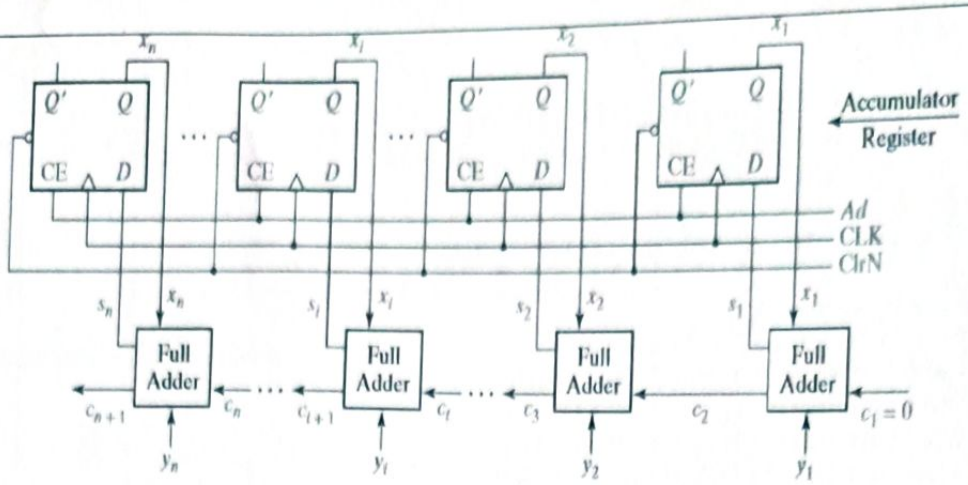


4-Bit Binary Adder

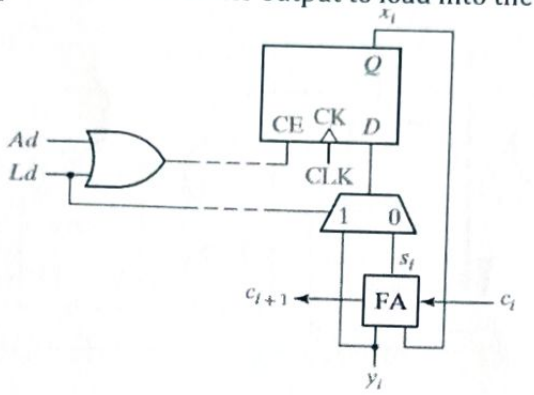
```
entityAdder4 is
    port (A,B:in bit_vector(3 downto 0);Ci:in bit; -- Inputs
    S:out bit_vector(3 downto 0);Co:out bit); -- Outputs endAdder4;
architecture Structure ofAdder4 is
component FullAdder
    port (X,Y,Cin:in bit; -- Inputs Cout,Sum:out bit); -- Outputs
end component;
signal C:bit_vector(3 downto 1);
begin -- instantiate four copies of the FullAdder
    FA0:FullAdder port map (A(0),B(0),Ci,C(1),S(0));
    FA1:FullAdder port map (A(1),B(1),C(1),C(2),S(1));
    FA2:FullAdder port map (A(2),B(2),C(2),C(3),S(2));
    FA3:FullAdder port map (A(3),B(3),C(3),Co,S(3));
end Structure;
```

2	b)	How J-K Flip-Flop is different from S-R Flip-Flop? Design Master-Slave J-K Flip-Flop, and explain its operation. Explain the behavior of JK=11(Toggle) and SR=11(Forbidden inputs). Master-Slave J-K Flip-Flop:   	5	CO5	L3
		Module - 4			

3	a)	Design and Explain the operation of n-Bit Parallel Adder with Accumulator.
		
		• Before addition can take place, the accumulator must be loaded with X.
		• This can be accomplished in two ways:
		  • Clear the accumulator
		  • Add multiplexers at the accumulator inputs
			4	CO5	L2

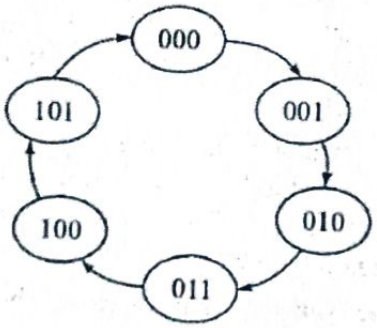


- **Clear the accumulator** using the asynchronous clear inputs on the flip-flops, and then put the X data on the Y inputs to the adder and add to the accumulator in the normal way.
- **Add multiplexers at the accumulator inputs:** So that we could select either the Y input data or the adder output to load into the accumulator.



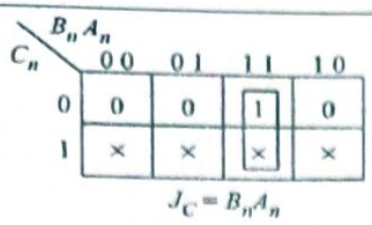
3	b)	Design the circuit for Modulo-6 synchronous Up Counter using J-K Flip-Flops.	6	CO5	L3

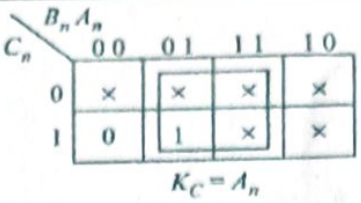
State Diagram:

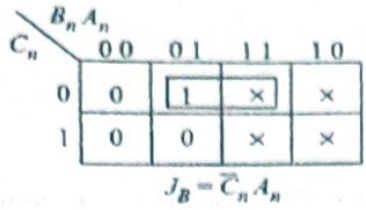


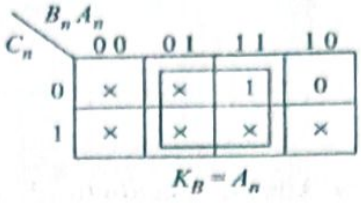
State Table:

C_n	B_n	A_n	C_{n+1}	B_{n+1}	A_{n+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	0	0	1	x	1	0	x	x	1

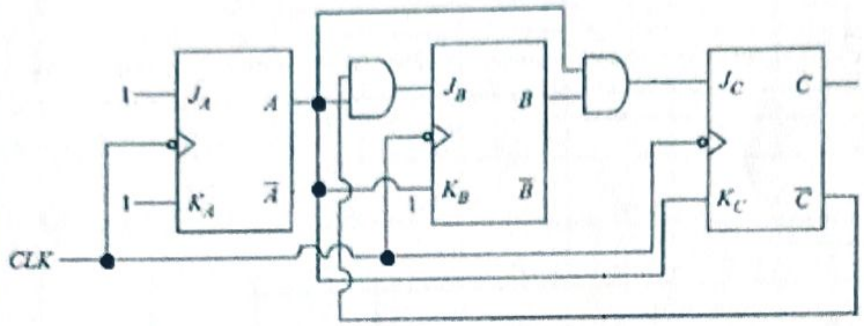








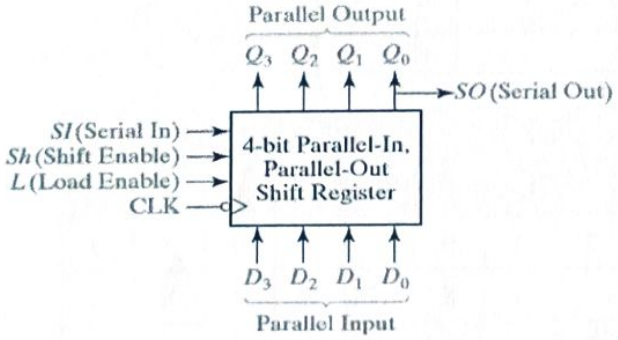
Circuit :



OR

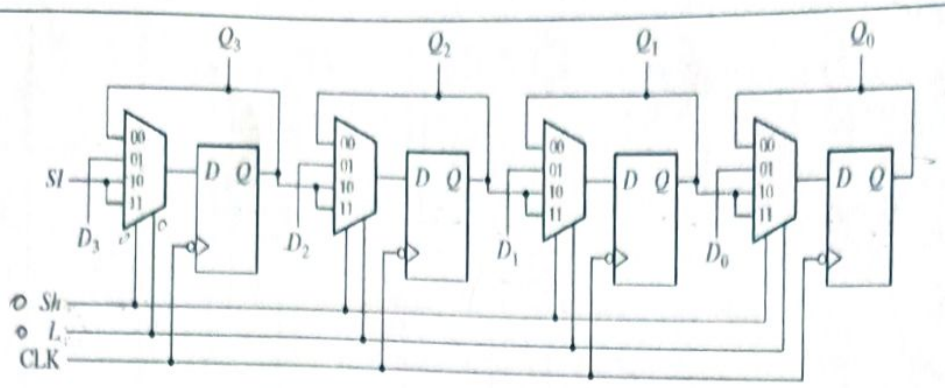
4	a)	What are Shift Registers? Design and Explain the operation of Parallel-In, Parallel-Out Right Shift Register using Multiplexer.	4	CO5	L2

- A shift register is a register in which binary data can be stored, and this data can be shifted to the left or right when a shift signal is applied.
- Bits shifted out one end of the register may be lost, or if the shift register is of cyclic type, bits shifted out one end are shifted back in the other end.



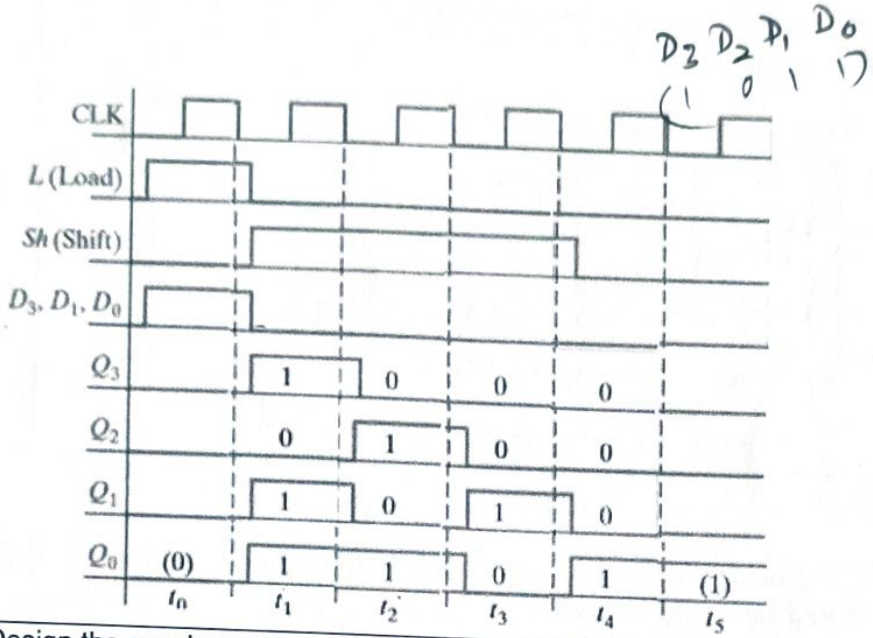
(a) Block diagram

Inputs		Next State				
Sh (Shift)	L (Load)	Q_3^+	Q_2^+	Q_1^+	Q_0^+	Action
0	0	Q_3	Q_2	Q_1	Q_0	No change
0	1	D_3	D_2	D_1	D_0	Load
1	X	SI	Q_3	Q_2	Q_1	Right shift



(b) Implementation using flip-flops and MUXes

Waveform:



4	b)	Design the synchronous counter for the following sequence using SR- Flip-Flops: 0 → 3 → 6 → 4 → 2	6	CO5	L3

$Q_n \rightarrow Q_{n+1}$		S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

Present State			Next State			Flip Flop Input					
A	B	C	A+	B+	C+	S_A	R_A	S_B	R_B	S_C	R_C
0	0	0	0	1	1	0	X	1	0	1	0
0	0	1	-	-	-	X	X	X	X	X	X
0	1	0	0	0	0	0	X	0	1	0	X
0	1	1	1	1	0	1	0	X	0	0	1
1	0	0	0	1	0	0	1	1	0	0	X
1	0	1	-	-	-	X	X	X	X	X	X
1	1	0	1	0	0	X	0	0	1	0	X
1	1	1	-	-	-	X	X	X	X	X	X

$S_A = C$

BC / A	00	01	11	10
0	0	X	1	0
1	0	X	X	X

$R_A = \bar{B}$

BC / A	00	01	11	10
0	X	X	0	X
1	1	X	X	0

$S_B = \bar{B}$

BC / A	00	01	11	10
0	1	X	X	0
1	1	X	X	0

$R_B = B\bar{C}$

BC / A	00	01	11	10
0	0	X	0	1
1	0	X	X	1

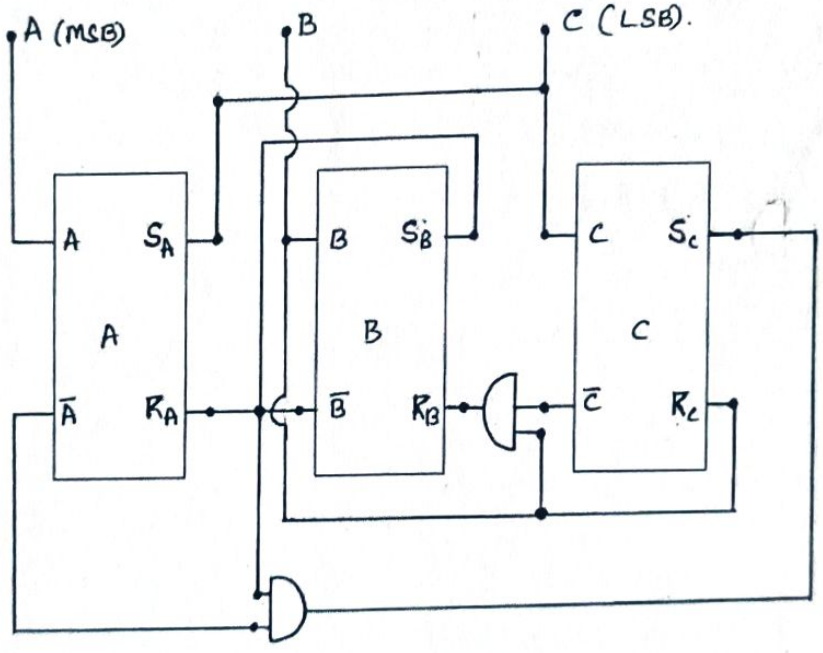
$S_C = \bar{A}\bar{B}$

BC / A	00	01	11	10
0	1	X	0	0
1	0	X	X	0

$R_C = B$ (or $R_C = C$)

BC / A	00	01	11	10
0	0	X	1	X
1	X	X	X	X

CIRCUIT DESIGN:



Subject In-charge 16/1/23

IQAC Member

HOD

USN: | | | | | | | | | | |

ALVA'S INSTITUTE OF ENGINEERING AND TECHNOLOGY, MIJAR

DEPARTMENT OF INFORMATION SCIENCE AND ENGINEERING

III - INTERNAL ASSESSMENT

SEMESTER: 3-CBCS(21-Scheme) DATE: 17-03-2023
SUBJECT : 21CS33- Analog and Digital Electronics TIME: 9.30am to 11.00am
FACULTY INCHARGE: Mr. Sharan Lional Pais MAX. MARKS: 20

INSTRUCTION: Answer ONE FULL questions from each Part.

PART - 1

Q. No:		Questions	Marks	CO	BT
1	A	Explain the working of Relaxation Oscillator.	5	1	L2
	B	Derive the expression for collector emitter voltage (V_{CE}) for fixed bias circuit.	5	1	L2
		OR			
2	A	Explain the working of Schmitt trigger.	5	1	L2
	B	Obtain the expression for collector to emitter voltage (V_{CE}) for voltage divider bias of BJT using accurate analysis.	5	1	L3

PART-2

3	A	What is multiplexer? Design 8-to-1 mux using 4-to-1 mux and 2-to-1 mux.	5	3	L2
	B	Explain how 4-bit register with data, load, clear and clock input is constructed using D Flip flops.	5	5	L3
		OR			
4	A	Design 7-segment decoder and realize using PLA.	5	3	L2
	B	Design 3-bit synchronous counter using T flip flop.	5	5	L3

Sharan 15/3/23
Subject Incharge

IQAC Member

IQAC Chairman

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ALVA'S INSTITUTE OF ENGINEERING AND TECHNOLOGY, MIJAR

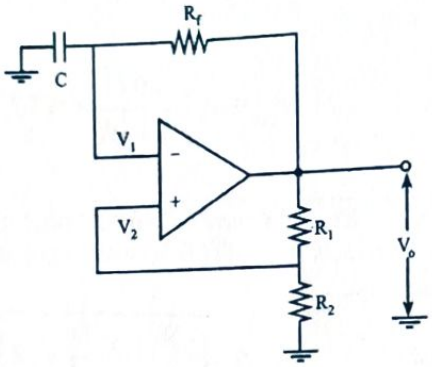
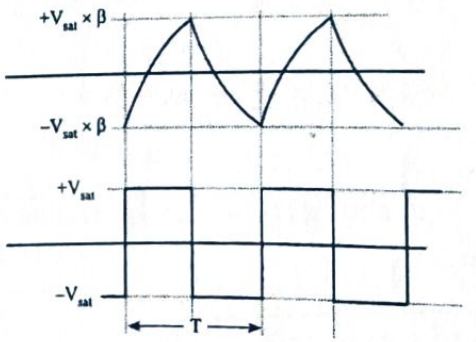
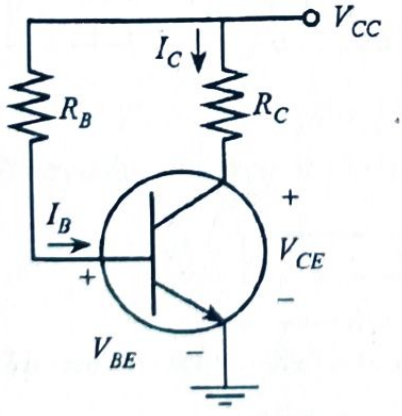
DEPARTMENT OF INFORMATION SCIENCE AND ENGINEERING

III - INTERNAL ASSESSMENT - ANSWER KEY/SCHEME

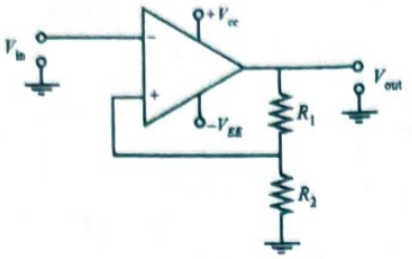
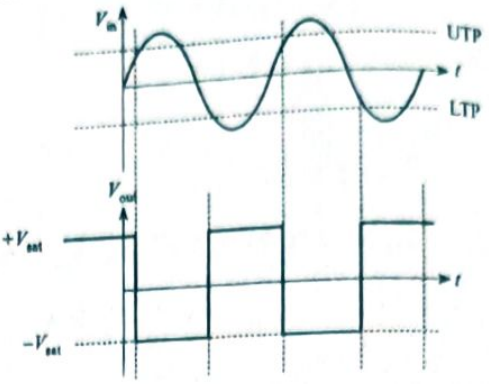
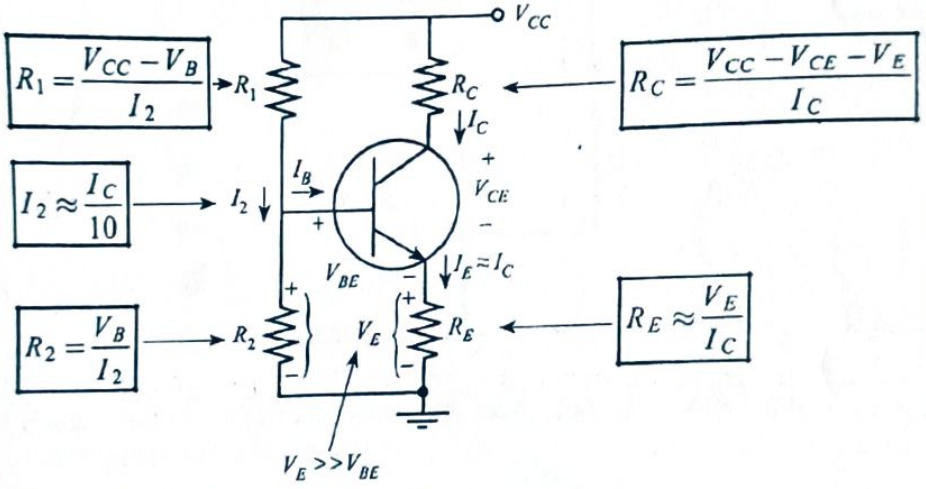
SEMESTER: 3-CBCS(21-Scheme) | DATE: 17-03-2023
SUBJECT : 21CS33- Analog and Digital Electronics | TIME: 9.30am to 11.00am
FACULTY INCHARGE: Mr. Sharan Lional Pais | MAX. MARKS: 20

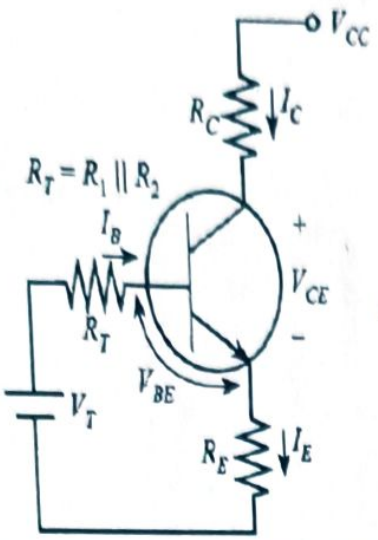
INSTRUCTION: Answer ONE FULL questions from each Part.

PART - 1

Q. No:		Questions	M	CO	BT
1	A	Explain the working of Relaxation Oscillator.   **Waveforms of Relaxation oscillator** $V_{UT} = \frac{R_1.(+V_{sat})}{R_1 + R_2}$ $V_{LT} = \frac{R_1(-V_{sat})}{R_1 + R_2}$ $T = 2R_fC\ln\left[\frac{2R_1 + R_2}{R_2}\right]$	5	1	L2
1	B	Derive the expression for collector emitter voltage (V_{CE}) for fixed bias circuit.  **Base bias circuit** $V_{CC} - I_BR_B - V_{BE} = 0$ $I_BR_B + V_{BE} = V_{CC}$ $\Rightarrow \quad I_B = \frac{V_{CC} - V_{BE}}{R_B}$ $I_C = \beta I_B.$ $V_{CC} = V_{CE} + I_CR_C$ $V_{CE} = V_{CC} - I_CR_C$	5	1	L2

OR

2	A	Explain the working of Schmitt trigger.  (a) Inverting Schmitt trigger circuit  (b) Waveform for Inverting Schmitt circuit. $V_{hys} = UTP - LTP$ $= \frac{R_2}{R_1+R_2}V_{sat} - \frac{R_2}{R_1+R_2}(-V_{sat})$ $= 2\left(\frac{R_2}{R_1+R_2}\right)V_{sat}$ $= 2\beta V_{sat}$ $UTP = \frac{R_2}{R_1+R_2}V_{sat}$ $LTP = \frac{R_2}{R_1+R_2}(-V_{sat})$	5	1	L2
2	B	Obtain the expression for collector to emitter voltage (V_{CE}) for voltage divider bias of BJT using accurate analysis.  $R_1 = \frac{V_{CC}-V_B}{I_2}$ → R_1 $R_C = \frac{V_{CC}-V_{CE}-V_E}{I_C}$ ← R_C $I_2 \approx \frac{I_C}{10}$ → I_2 $R_2 = \frac{V_B}{I_2}$ → R_2 $R_E \approx \frac{V_E}{I_C}$ ← R_E $V_E >> V_{BE}$ Thevenins voltage is given by, $V_T = \frac{V_{CC}R_2}{R_1+R_2}$ The equivalent resistance of parallel combination of resistors $R_T = \frac{R_1R_2}{R_1+R_2}$	5	1	L3



Applying KVL to the base circuit we get,

$$V_T = I_B R_T + V_{BE} + I_E R_E$$

$$= I_B R_T + V_{BE} + (1+\beta) I_B R_E$$

$$I_B = \frac{V_T - V_{BE}}{R_T + (1+\beta)R_E}$$

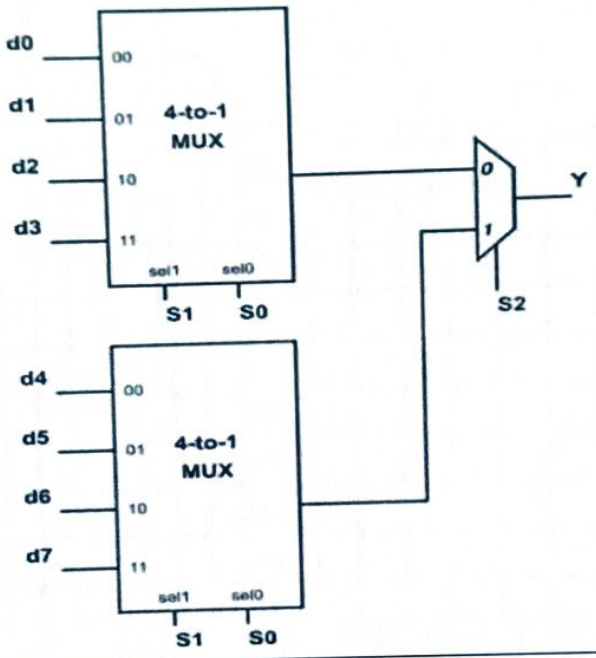
Applying KVL to the collector circuit we get,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

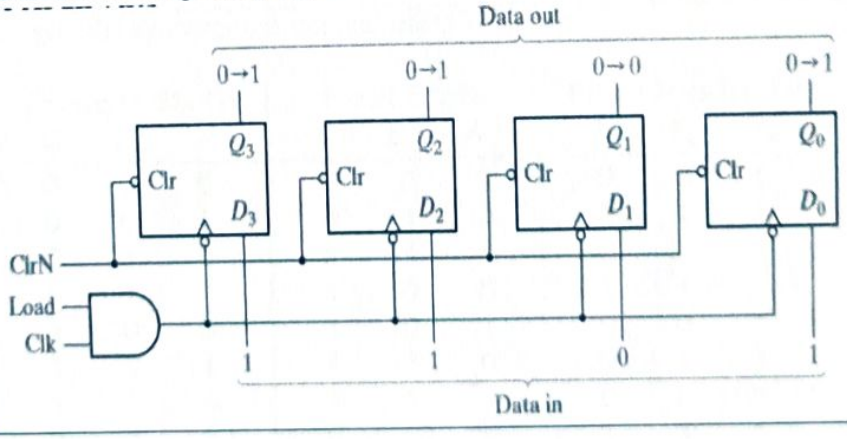
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

PART-2

3	A	What is multiplexer? Design 8-to-1 mux using 4-to-1 mux and 2-to-1 mux.	5	3	L2



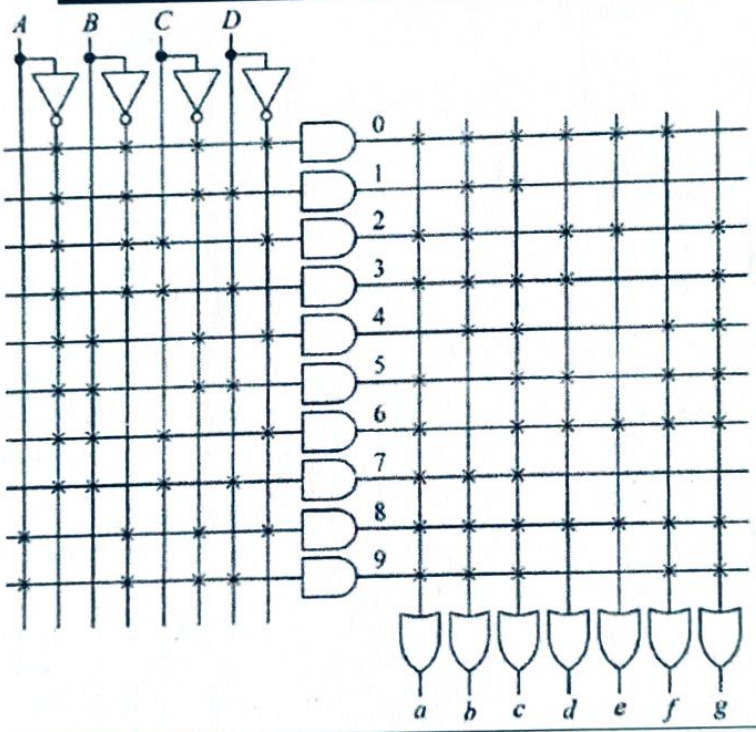
3	B	Explain how 4-bit register with data, load, clear and clock input is constructed using D Flip flops.	5	5	L3



OR

4	A	Design 7-segment decoder and realize using PLA.	5	3	L2

Segments Inputs							7 Segment Display Output
a	b	c	d	e	f	g	
1	1	1	1	1	1	0	0
0	1	1	0	0	0	0	1
1	1	0	1	1	0	1	2
1	1	1	1	0	0	1	3
0	1	1	0	0	1	1	4
1	0	1	1	0	1	1	5
1	0	1	1	1	1	1	6
1	1	1	0	0	0	0	7
1	1	1	1	1	1	1	8
1	1	1	1	0	0	1	9



4	B	Design 3-bit synchronous counter using T flip flop.						5	5	L3

Present State			Next State			Flip-Flop Inputs		
C	B	A	C^+	B^+	A^+	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

BA \ C	0	1
00	0	0
01	0	0
11	1	1
10	0	0

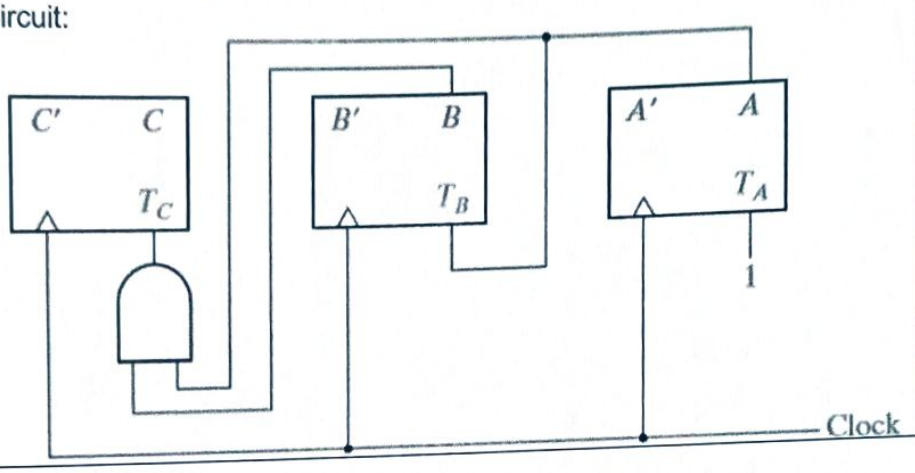
T_C

BA \ C	0	1
00	0	0
01	1	1
11	1	1
10	0	0

T_B

$T_C = BA$ $T_B = A.$ $T_A = 1$

Circuit:



Sharan 15/3/23.
Subject Incharge

HOD

RUBRICS TO BE FOLLOWED FOR ASSIGNMENT EVALUATION

Parameters	Not Submitted	Incomplete Assignment	Correctness of the Problem/Program	Timely submitted with correctness of the Problem/Program
Marks Allocation	0	1 - 4	5 - 9	10

Subject Teacher

HOD

Assignment -1 (21CS33 - Analog & Digital Electronics)
CO Mapped: CO2 BLT: L3
Announcement Date: 15-11-2022 (2022-23)

A) Get a simplified **Sum of Products** expression using K-Maps for the following:

1. f1(A,B,C,D) = Σm(1,3,4,5,7,10,12)
2. f2(A,B,C,D) = Σm(5,8,9,10,11,12,13,14,15)
3. f3(A,B,C,D) = Σm(0,2,3,5,6,7,8,9)+ d(10,11,12,13,14,15)
4. f4(A,B,C,D) = Σm(4,5,6)+d(10,12,13,14,15)
5. f5(A,B,C,D) = Σm(0,1,3,5,6,7,11,12,14)

B) Get a simplified **Product of Sum** expression using K-Maps for the following:

6. f6(A,B,C,D) = ΠM(1,9,11,12,14)
7. f7(A,B,C,D) = ΠM(5,7,13,15). D(1,2,3,9)
8. f8(A,B,C,D) = M1.M3.M5.M7
9. f9(A,B,C,D) = ΠM(2,3,4)
10. f10(A,B,C,D) = ΠM(5,7,8,9,12). D(0,6,10,15)

C) Get simplified **Sum of Product** and **Product of Sum** expressions using K-Maps for the following:

11. f11(W,X,Y,Z) = Σm(1,2,4,13,14)+ d(5,6,7,8,9,10)
12. f12(P,Q,R,S) = ΠM(0,2,6,7,9,12,13). ΠD(1,3,5)

D) Get a minimum SOP expression using **QM Method** for the following expression:

13. f13(a,b,c,d) = Σm(0,2,3,4,8,10,12,13,14)
14. f14(a,b,c,d) = Σm(7,9,12,13,14,15)+d(4,11)
15. f15(a,b,c,d) = Σm(1,3,6,7,10,12,13,14,15)

E) Determine minimal sum using MEV technique for the given functions:

16. f16(a,b,c,d) = Σm(3,4,5,7,8,11,12,13,15)
17. f17(A,B,C,D) =Σm(2,3,4,5,13,15)+d(1,10)

F) Explain Petrick's **Method**.

G) There are four adjacent parking slots in Mega Inc. executive parking area. Each Slot is equipped with sensor whose output is asserted high (1) when a

car is occupying the slot. Write a truth table so that the output is high (1) if two or more vacant parking is available.

i. write truth table
ii. find the expression of the system that will signal the existence of two or more vacant slots
iii. simplify the expression
iv. Draw the logic diagram for simplified expression

H) A digital system is to be designed in which the months of the year is given as input in 4 bit form. The month January is represented as 0000 February as 0001 and so on. The output of the system should be one (1) corresponding to the input of the month containing 31 days or otherwise it is zero (0). Consider excess number in the input beyond 1011 as don't care conditions. For this system of 4 variable ABCD find the following:

i. Boolean expression information Σm and ΠM form
ii. using k map simplify in a SOP form
iii. implement using NAND NAND Gates

Sharan
15/11/22.
Faculty In-charge.

Assignment-2 (21CS33 - Analog & Digital Electronics)
CO Mapped: CO3 BLT: L3
Announcement Date: 31-12-2022 (2022-23)
Submission On/Before: 07-01-2023

Question: (Practical Experiment)

- What do you mean by Parity?
- Describe types of parity.
- Conduct a Hardware experiment on Odd or Even Parity Checking.

Note: Conduct the lab experiment in ADE Lab and take signature after showing the output. Later same can be submitted as a assignment.

Sharan 31/12/22.
Subject In-charge

Assignment-3 (21CS33 - Analog & Digital Electronics)

CO Mapped: CO4, CO5 BLT: L3

Announcement Date: 09-01-2023 (2022-23)

Submission On/Before: 23-01-2023

Questions:

1. Write VHDL code for 4-to-1 Multiplexer.
2. Write the VHDL code for 4 bit parallel adder using full adder as component.
3. Derive characteristic equation for the following flip flops: SR, J, T and D flip flop.
4. Explain four bit parallel adder with accumulator
5. Differentiate between ring counter and Johnson counter.
6. Design 3 bit synchronous binary counter using T Flip Flop.

Sharan 9/01/23

Subject In-charge

Assignment-4 (21CS33 - Analog & Digital Electronics)

CO Mapped: CO1 BLT: L2,L3

Announcement Date: 02-03-2023 (2022-23)

Submission On/Before: 20-03-2023

Questions:

1. Design a monostable multivibrator circuit using 555 timer IC to generate an output pulse of 100ms. Choose C=0.47uF. Draw the circuit.
2. Design and draw astable multivibrator circuit using 555 timer IC to generate 1 kHz square wave (Duty Cycle=50%). Assume C=0.1uF.
3. Obtain the expression for collector to emitter voltage (V_{CE}) for voltage divider bias of BJT using accurate analysis.
4. Derive the expression for collector emitter voltage (V_{CE}) for fixed bias circuit.
5. Explain current to voltage converter.
6. Give the typical application of A/D and D/A converters with a block diagram.
7. Explain Adjustable Voltage regulator.
8. Explain the working of Schmitt trigger.
9. Explain the working of Relaxation Oscillator.
10. Explain with neat diagram R-2R ladder type DAC and derive the expression for V_0.

Sharan 2/3/23

Subject In-charge

Analog and Digital Electronics			Assignment Marks				
S. No.	USN	Full name	1	2	3	4	Final Marks (20)
1	4AL21IS001	Adithya Tejaswi D	4	5	5	5	19
2	4AL21IS002	Afiza A	5	5	5	5	20
3	4AL21IS003	Aishwarya Salimath	5	5	5	5	20
4	4AL21IS004	Akash Devadiga	4	5	5	5	19
5	4AL21IS005	Amar B M	4	5	5	5	19
6	4AL21IS006	Anagha Udupa Y N	5	5	5	5	20
7	4AL21IS007	Ananya	4	5	5	5	19
8	4AL21IS008	Anirudh Kamath K	4	5	5	4	18
9	4AL21IS009	Ankitha B	5	5	5	5	20
10	4AL21IS010	Bhagyashree R Pujari	4	5	5	5	19
11	4AL21IS011	Bharath J	4	5	5	5	19
12	4AL21IS012	Bhumika Sunil Kulkarni	5	5	5	5	20
13	4AL21IS013	Chaitra S Koddaddi	4	5	5	5	19
14	4AL21IS014	Chandan M N	4	5	5	5	19
15	4AL21IS015	Chindan B V	4	5	5	5	19
16	4AL21IS017	Gowrish N	5	5	5	5	20
17	4AL21IS018	Harshitha B	5	5	5	5	20
18	4AL21IS019	Jahnavi	4	5	5	5	19
19	4AL21IS020	Karthik Madakari T P	4	5	5	5	19
20	4AL21IS021	Kelvin Dmello	5	5	5	5	20
21	4AL21IS022	Koushik Achar	5	5	5	5	20
22	4AL21IS023	Krupashree R	4	5	5	5	19
23	4AL21IS024	Laya R	4	5	5	5	19
24	4AL21IS025	Manikanta	5	5	5	5	20
25	4AL21IS026	Manish K	4	5	5	5	19
26	4AL21IS027	Manjunath R	4	4	5	5	18
27	4AL21IS028	Manoj Lokesh	3	3	0	0	6
28	4AL21IS029	Manoj M U	5	5	5	5	20
29	4AL21IS030	Mohammed Adil	4	5	5	4	18
30	4AL21IS031	Mohammed Rihan	4	5	5	5	19
31	4AL21IS032	Muhammed Yamin Sharfuddin	5	5	5	5	20
32	4AL21IS033	NANDAN S	4	5	5	5	19
33	4AL21IS034	Nishant Kumar	4	5	5	5	19
34	4AL21IS035	Pragathi G Gowda	5	5	5	5	20
35	4AL21IS036	Prajna	5	5	5	5	20
36	4AL21IS037	Prajwal Gowda H G	5	5	5	5	20
37	4AL21IS038	Prashanth Kumar B C	3	5	5	5	18
38	4AL21IS039	Preetham Byadagi	4	5	5	4	18
39	4AL21IS040	R Sreejith	4	5	5	4	18
40	4AL21IS041	Ranjith	3	5	5	5	18
41	4AL21IS042	Sanjay G K	4	5	5	5	19
42	4AL21IS043	Sannidhi K S	5	5	5	5	20
43	4AL21IS044	Sapthami	5	5	5	5	20
44	4AL21IS045	Sarthak K Jain	5	5	5	5	20
45	4AL21IS046	Sateesh Dyavappa Satyannavar	4	5	5	5	19
46	4AL21IS047	Sathwik K D	5	5	5	5	20
47	4AL21IS048	Sharavi R Rai	4	5	5	5	19
48	4AL21IS049	Shashidhar Mahadev Patgar	4	5	5	5	19
49	4AL21IS050	Shravan R Poojary	4	5	5	5	19
50	4AL21IS051	Shravitha	5	5	5	5	20
51	4AL21IS052	Shreya Rai	5	5	5	5	20
52	4AL21IS053	Shrujan Kumar H V	4	5	5	4	18
53	4AL21IS054	Sooraj	5	5	5	5	20
54	4AL21IS055	SriDeeksha G	5	5	5	5	20
55	4AL21IS056	Srikanth Raju Srinivas	4	5	5	5	19
56	4AL21IS057	Srujan K M	4	5	5	5	19
57	4AL21IS058	Srusti P S	5	5	5	5	20
58	4AL21IS059	Suvan P Kedilaya	4	5	5	5	19
59	4AL21IS060	Suvarna Arvinkanth Harish	4	5	5	5	19
60	4AL21IS061	Syed Saleha	5	5	5	5	20
61	4AL21IS062	Vasavi Rai C	4	5	5	5	19
62	4AL21IS063	Vithika Shetty	5	5	5	5	20
63	4AL21IS064	Chandana	5	5	5	5	20
64	4AL22IS400	Ankith	5	5	5	5	20
65	4AL22IS401	Charan S V	5	5	5	5	20
66	4AL22IS402	Chetan Byaleatti	5	5	5	5	20
67	4AL22IS405	Rahul P Shetty	5	5	5	5	20
68	4AL22IS404	Namratha J Shetty	5	5	5	5	20
69	4AL22IS403	Lohith H	5	5	5	5	20

S. No.	USN	Full name	Procedure (15)	Conduction (25)	Viva (10)	Total (50)	Out of 5
1	4AL21IS001	Adithya Tejaswi D	15	24	6	45	5
2	4AL21IS002	Afiza A	14	24	10	48	5
3	4AL21IS003	Aishwarya Salimath	2	5	8	15	2
4	4AL21IS004	Akash Devadiga	15	24	6	45	5
5	4AL21IS005	Amar B M	4	8	6	18	2
6	4AL21IS006	Anagha Udupa Y N	7	13	8	28	3
7	4AL21IS007	Ananya	7	12	6	25	3
8	4AL21IS008	Anirudh Kamath K	4	7	6	17	2
9	4AL21IS009	Ankitha B	12	20	6	38	4
10	4AL21IS010	Bhagyashree R Pujari	5	9	4	18	2
11	4AL21IS011	Bharath J	15	25	8	48	5
12	4AL21IS012	Bhumika Sunil Kulkarni	12	21	10	43	5
13	4AL21IS013	Chaitra S Koddaddi	4	8	6	18	2
14	4AL21IS014	Chandan M N	5	9	4	18	2
15	4AL21IS015	Chindan B V	15	24	6	45	5
16	4AL21IS017	Gowrish N	7	13	8	28	3
17	4AL21IS018	Harshitha B	15	25	8	48	5
18	4AL21IS019	Jahnavi	8	14	6	28	3
19	4AL21IS020	Karthik Madakari T P	15	25	8	48	5
20	4AL21IS021	Kelvin Dmello	15	25	8	48	5
21	4AL21IS022	Koushik Achar	15	25	8	48	5
22	4AL21IS023	Krupashree R	4	7	4	15	2
23	4AL21IS024	Laya R	14	23	8	45	5
24	4AL21IS025	Manikanta	15	25	8	48	5
25	4AL21IS026	Manish K	4	7	4	15	2
26	4AL21IS027	Manjunath R	5	8	6	19	2
27	4AL21IS028	Manoj Lokesh	0	0	0	0	0
28	4AL21IS029	Manoj M U	15	25	10	50	5
29	4AL21IS030	Mohammed Adil	6	11	6	23	3
30	4AL21IS031	Mohammed Rihan	15	25	8	48	5
31	4AL21IS032	Muhammed Yamin Sharfuddin	14	24	8	46	5
32	4AL21IS033	NANDAN S	1	2	6	9	1
33	4AL21IS034	Nishant Kumar	12	21	8	41	5
34	4AL21IS035	Pragathi G Gowda	15	23	10	48	5
35	4AL21IS036	Prajna	15	25	8	48	5
36	4AL21IS037	Prajwal Gowda H G	15	25	8	48	5
37	4AL21IS038	Prashanth Kumar B C	4	7	6	17	2
38	4AL21IS039	Preetham Byadagi	1	2	4	7	1
39	4AL21IS040	R Sreejith	5	9	6	20	2
40	4AL21IS041	Ranjith	6	11	6	23	3
41	4AL21IS042	Sanjay G K	8	14	6	28	3
42	4AL21IS043	Sannidhi K S	8	14	8	30	3
43	4AL21IS044	Sapthami	15	24	6	45	5
44	4AL21IS045	Sarthak K Jain	15	24	6	45	5
45	4AL21IS046	Sateesh Dyavappa Satyannavar	15	24	6	45	5
46	4AL21IS047	Sathwik K D	13	22	10	45	5
47	4AL21IS048	Sharavi R Rai	8	14	6	28	3
48	4AL21IS049	Shashidhar Mahadev Patgar	15	24	10	49	5
49	4AL21IS050	Shravan R Poojary	6	11	6	23	3
50	4AL21IS051	Shravitha	4	8	6	18	2
51	4AL21IS052	Shreya Rai	15	24	6	45	5
52	4AL21IS053	Shrujan Kumar H V	6	11	6	23	3
53	4AL21IS054	Sooraj	15	25	10	50	5
54	4AL21IS055	SriDeeksha G	4	8	6	18	2
55	4AL21IS056	Srikanth Raju Srinivas	4	8	6	18	2
56	4AL21IS057	Srujan K M	7	12	6	25	3
57	4AL21IS058	Srusti P S	15	25	8	48	5
58	4AL21IS059	Suvan P Kedilaya	10	17	6	33	4
59	4AL21IS060	Suvarna Arvinkanth Harish	15	24	4	43	5
60	4AL21IS061	Syed Saleha	15	25	8	48	5
61	4AL21IS062	Vasavi Rai C	7	12	6	25	3
62	4AL21IS063	Vithika Shetty	10	17	10	37	4
63	4AL21IS064	Chandana	7	12	6	25	3
64	4AL22IS400	Ankith	11	19	6	36	4
65	4AL22IS401	Charan S V	10	17	6	33	4
66	4AL22IS402	Chetan Byaleatti	10	17	6	33	4
67	4AL22IS405	Rahul P Shetty	11	19	6	36	4
68	4AL22IS404	Namratha J Shetty	11	19	6	36	4
69	4AL22IS403	Lohith H	11	19	6	36	4

Analog and Digital Electronics			Module-wise Lab experiment Marks												
S. No.	USN	Full name	Exp-1	Exp-2	Exp-3	Exp-4	Exp-5	Exp-6	Exp-7	Exp-8	Exp-9	Exp-10	AVG (Exp) (15)	LAB IA (5)	Final Lab Marks (20)
1	4AL21IS001	Adithya Tejaswi D	15	10	10	10	10	15	15	15	15	15	13	5	18
2	4AL21IS002	Afiza A	10	15	15	15	15	15	15	15	15	15	15	5	20
3	4AL21IS003	Aishwarya Salimath	10	10	15	10	10	15	15	15	15	15	13	2	15
4	4AL21IS004	Akash Devadiga	15	15	15	15	15	15	15	15	15	15	15	5	20
5	4AL21IS005	Amar B M	10	10	10	10	15	10	15	15	15	15	13	2	15
6	4AL21IS006	Anagha Udupa Y N	15	15	15	15	10	15	15	15	15	15	15	3	18
7	4AL21IS007	Ananya	15	15	15	15	10	15	15	15	15	15	15	3	18
8	4AL21IS008	Anirudh Kamath K	10	10	10	15	10	15	15	15	15	15	13	2	15
9	4AL21IS009	Ankitha B	15	10	10	15	10	10	15	15	15	15	13	4	17
10	4AL21IS010	Bhagyashree R Pujari	15	15	10	15	10	15	15	15	15	15	14	2	16
11	4AL21IS011	Bharath J	15	10	10	15	10	15	15	15	15	15	14	5	19
12	4AL21IS012	Bhumika Sunil Kulkarni	15	15	10	15	15	15	15	15	15	15	15	5	20
13	4AL21IS013	Chaitra S Koddaddi	10	10	10	0	10	15	15	15	15	15	12	2	14
14	4AL21IS014	Chandan M N	10	10	10	10	10	10	15	15	15	15	12	2	14
15	4AL21IS015	Chindan B V	10	10	10	10	15	15	15	15	15	15	13	5	18
16	4AL21IS017	Gowrish N	15	10	10	10	10	15	15	15	15	15	13	3	16
17	4AL21IS018	Harshitha B	15	15	15	15	10	15	15	15	15	15	15	5	20
18	4AL21IS019	Jahnavi	15	15	15	15	10	15	15	15	15	15	15	3	18
19	4AL21IS020	Karthik Madakari T P	10	10	10	10	10	15	15	15	15	15	13	5	18
20	4AL21IS021	Kelvin Dmello	15	15	15	15	15	15	15	15	15	15	15	5	20
21	4AL21IS022	Koushik Achar	15	15	15	15	15	15	15	15	15	15	15	5	20
22	4AL21IS023	Krupashree R	10	10	15	10	10	15	15	15	15	15	13	2	15
23	4AL21IS024	Laya R	10	10	15	10	10	15	10	15	10	10	12	5	17
24	4AL21IS025	Manikanta	10	15	15	15	15	15	15	15	15	15	15	5	20
25	4AL21IS026	Manish K	10	15	10	10	10	10	15	15	15	15	13	2	15
26	4AL21IS027	Manjunath R	10	10	15	10	10	10	15	15	15	15	13	2	15
27	4AL21IS028	Manoj Lokesh	15	15	15	15	10	10	0	0	0	0	8	0	8
28	4AL21IS029	Manoj M U	15	15	10	15	15	15	15	15	15	15	15	5	20
29	4AL21IS030	Mohammed Adil	10	10	10	10	10	15	15	15	15	15	13	3	16
30	4AL21IS031	Mohammed Rihan	15	10	15	10	10	15	15	15	15	15	14	5	19
31	4AL21IS032	Muhammed Yamin Sharfuddin	15	15	15	15	10	15	15	15	15	15	15	5	20
32	4AL21IS033	NANDAN S	15	10	15	10	10	10	15	15	15	15	13	1	14
33	4AL21IS034	Nishant Kumar	10	15	15	15	15	15	15	15	15	15	15	5	20
34	4AL21IS035	Pragathi G Gowda	15	15	15	15	10	15	15	15	15	15	15	5	20
35	4AL21IS036	Prajna	15	15	15	15	15	15	15	15	15	15	15	5	20
36	4AL21IS037	Prajwal Gowda H G	15	15	15	15	15	10	15	15	15	15	15	5	20
37	4AL21IS038	Prashanth Kumar B C	10	10	10	10	8	8	8	8	10	10	10	2	12
38	4AL21IS039	Preetham Byadagi	15	15	15	15	15	10	15	15	15	15	15	1	16
39	4AL21IS040	R Sreejith	15	15	10	10	15	15	15	15	15	15	14	2	16
40	4AL21IS041	Ranjith	15	15	15	0	15	15	15	15	15	15	14	3	17
41	4AL21IS042	Sanjay G K	15	10	15	15	10	15	15	15	15	15	14	3	17
42	4AL21IS043	Sannidhi K S	15	15	10	15	10	15	15	15	15	15	14	3	17
43	4AL21IS044	Sapthami	15	15	15	15	10	15	15	15	15	15	15	5	20
44	4AL21IS045	Sarthak K Jain	10	15	15	15	15	15	15	15	15	15	15	5	20
45	4AL21IS046	Sateesh Dyavappa Satyannavar	15	15	15	10	10	15	15	15	15	15	14	5	19
46	4AL21IS047	Sathwik K D	15	15	15	15	15	15	15	15	15	15	15	5	20
47	4AL21IS048	Sharavi R Rai	15	15	15	10	10	15	10	15	15	15	14	3	17
48	4AL21IS049	Shashidhar Mahadev Patgar	15	15	15	10	15	15	15	15	15	15	15	5	20
49	4AL21IS050	Shravan R Poojary	10	15	15	15	15	15	15	15	15	15	15	3	18
50	4AL21IS051	Shravitha	15	15	15	15	15	15	10	10	10	10	13	2	15
51	4AL21IS052	Shreya Rai	15	15	15	15	15	15	15	15	15	10	15	5	20
52	4AL21IS053	Shrujan Kumar H V	10	15	10	15	15	10	15	15	15	15	14	3	17
53	4AL21IS054	Sooraj	15	15	15	15	15	15	15	15	15	15	15	5	20
54	4AL21IS055	SriDeeksha G	15	15	15	15	15	15	15	15	15	15	15	2	17
55	4AL21IS056	Srikanth Raju Srinivas	15	10	15	15	10	10	15	15	15	15	14	2	16
56	4AL21IS057	Srujan K M	15	15	15	15	15	10	15	15	15	15	15	3	18
57	4AL21IS058	Srusti P S	15	15	15	15	15	15	15	15	15	15	15	5	20
58	4AL21IS059	Suvan P Kedilaya	15	15	10	10	10	10	15	15	15	15	13	4	17
59	4AL21IS060	Suvarna Arvinkanth Harish	15	15	10	10	15	15	15	15	15	15	14	5	19
60	4AL21IS061	Syed Saleha	15	15	15	15	15	15	15	15	15	15	15	5	20
10	4AL21IS062	Vasavi Rai C	15	15	15	15	10	10	10	10	15	15	13	3	16
62	4AL21IS063	Vithika Shetty	15	15	15	15	15	15	15	15	15	15	15	4	19
63	4AL21IS064	Chandana	10	10	10	15	15	15	15	15	15	15	14	3	17
64	4AL22IS400	Ankith	15	15	15	15	15	15	15	15	15	15	15	4	19
65	4AL22IS401	Charan S V	15	15	15	15	15	15	15	15	15	15	15	4	19
66	4AL22IS402	Chetan Byaleatti	15	15	15	15	15	10	10	10	10	10	13	4	17
67	4AL22IS405	Rahul P Shetty	15	15	15	15	15	15	15	15	15	15	15	4	19
68	4AL22IS404	Namratha J Shetty	15	15	15	15	15	15	15	15	15	15	15	4	19
69	4AL22IS403	Lohith H	15	15	15	15	15	15	15	15	15	15	15	4	19

Analog and Digital Electronics CIE Marks 2022-23													
S. No.	USN	Full name	IA1	IA2	IA3	MIN	IA TOTAL (Best Two IA) (40)	ASSIGNMENT (20)	IA + ASMT (60)	Final IA (30)	LAB (20)	TOTAL (50)	Attd
1	4AL21IS001	Adithya Tejaswi D	16	13	18	13	34	19	53	27	18	**45**	88
2	4AL21IS002	Afiza A	12	15	20	12	35	20	55	28	20	**48**	99
3	4AL21IS003	Aishwarya Salimath	14	13	16	13	30	20	50	25	15	**40**	89
4	4AL21IS004	Akash Devadiga	12	17	20	12	37	19	56	28	20	**48**	96
5	4AL21IS005	Amar B M	9	12	14	9	26	19	45	23	15	**38**	85
6	4AL21IS006	Anagha Udupa Y N	19	19	20	19	39	20	59	30	18	**48**	91
7	4AL21IS007	Ananya	10	14	17	10	31	19	50	25	18	**43**	90
8	4AL21IS008	Anirudh Kamath K	7	12	18	7	30	18	48	24	15	**39**	85
9	4AL21IS009	Ankitha B	11	13	20	11	33	20	53	27	17	**44**	91
10	4AL21IS010	Bhagyashree R Pujari	11	11	19	11	30	19	49	25	16	**41**	88
11	4AL21IS011	Bharath J	17	12	20	12	37	19	56	28	19	**47**	99
12	4AL21IS012	Bhumika Sunil Kulkarni	14	19	20	14	39	20	59	30	20	**50**	94
13	4AL21IS013	Chaitra S Koddaddi	9	13	17	9	30	19	49	25	14	**39**	87
14	4AL21IS014	Chandan M N	6	9	19	6	28	19	47	24	14	**38**	87
15	4AL21IS015	Chindan B V	12	13	15	12	28	19	47	24	18	**42**	87
16	4AL21IS017	Gowrish N	14	16	16	14	32	20	52	26	16	**42**	96
17	4AL21IS018	Harshitha B	14	7	12	7	26	20	46	23	20	**43**	85
18	4AL21IS019	Jahnavi	12	15	20	12	35	19	54	27	18	**45**	88
19	4AL21IS020	Karthik Madakari T P	13	16	20	13	36	19	55	28	18	**46**	100
20	4AL21IS021	Kelvin Dmello	20	18	20	18	40	20	60	30	20	**50**	99
21	4AL21IS022	Koushik Achar	18	19	17	17	37	20	57	29	20	**49**	94
22	4AL21IS023	Krupashree R	9	10	17	9	27	19	46	23	15	**38**	85
23	4AL21IS024	Laya R	10	14	15	10	29	19	48	24	17	**41**	87
24	4AL21IS025	Manikanta	19	15	20	15	39	20	59	30	20	**50**	88
25	4AL21IS026	Manish K	7	13	18	7	31	19	50	25	15	**40**	85
26	4AL21IS027	Manjunath R	17	12	14	12	31	18	49	25	15	**40**	86
27	4AL21IS028	Manoj Lokesh	11	12	0	0	23	6	29	15	8	**23**	78
28	4AL21IS029	Manoj M U	18	19	20	18	39	20	59	30	20	**50**	99
29	4AL21IS030	Mohammed Adil	10	10	15	10	25	18	43	22	16	**38**	90
30	4AL21IS031	Mohammed Rihan	13	11	18	11	31	19	50	25	19	**44**	85
31	4AL21IS032	Muhammed Yamin Sharfuddin	15	18	20	15	38	20	58	29	20	**49**	88

Analog and Digital Electronics CIE Marks 2022-23													
S. No.	USN	Full name	IA1	IA2	IA3	MIN	IA TOTAL (Best Two IA) (40)	ASSIGNMENT (20)	IA + ASMT (60)	Final IA (30)	LAB (20)	TOTAL (50)	Attd
32	4AL21IS033	NANDAN S	10	9	18	9	28	19	47	24	14	38	85
33	4AL21IS034	Nishant Kumar	15	18	20	15	38	19	57	29	20	49	87
34	4AL21IS035	Pragathi G Gowda	12	17	20	12	37	20	57	29	20	49	96
35	4AL21IS036	Prajna	19	15	20	15	39	20	59	30	20	50	96
36	4AL21IS037	Prajwal Gowda H G	16	14	17	14	33	20	53	27	20	47	93
37	4AL21IS038	Prashanth Kumar B C	11	6	15	6	26	18	44	22	12	34	85
38	4AL21IS039	Preetham Byadagi	7	9	10	7	19	18	37	19	16	35	88
39	4AL21IS040	R Sreejith	7	13	15	7	28	18	46	23	16	39	85
40	4AL21IS041	Ranjith	14	9	15	9	29	18	47	24	17	41	90
41	4AL21IS042	Sanjay G K	11	12	19	11	31	19	50	25	17	42	93
42	4AL21IS043	Sannidhi K S	8	15	19	8	34	20	54	27	17	44	93
43	4AL21IS044	Sapthami	14	13	19	13	33	20	53	27	20	47	93
44	4AL21IS045	Sarthak K Jain	8	11	17	8	28	20	48	24	20	44	97
45	4AL21IS046	Sateesh Dyavappa Satyannavar	7	6	18	6	25	19	44	22	19	41	88
46	4AL21IS047	Sathwik K D	12	16	20	12	36	20	56	28	20	48	85
47	4AL21IS048	Sharavi R Rai	12	10	19	10	31	19	50	25	17	42	96
48	4AL21IS049	Shashidhar Mahadev Patgar	19	16	20	16	39	19	58	29	20	49	91
49	4AL21IS050	Shravan R Poojary	13	10	10	10	23	19	42	21	18	39	88
50	4AL21IS051	Shravitha	9	11	16	9	27	20	47	24	15	39	91
51	4AL21IS052	Shreya Rai	12	12	19	12	31	20	51	26	20	46	91
52	4AL21IS053	Shrujan Kumar H V	6	6	14	6	20	18	38	19	17	36	86
53	4AL21IS054	Sooraj	14	15	17	14	32	20	52	26	20	46	91
54	4AL21IS055	SriDeeksha G	13	8	18	8	31	20	51	26	17	43	90
55	4AL21IS056	Srikanth Raju Srinivas	12	9	12	9	24	19	43	22	16	38	86
56	4AL21IS057	Srujan K M	12	10	20	10	32	19	51	26	18	44	85
57	4AL21IS058	Srusti P S	17	17	20	17	37	20	57	29	20	49	95
58	4AL21IS059	Suvan P Kedilaya	13	10	19	10	32	19	51	26	17	43	85
59	4AL21IS060	Suvarna Arvinkanth Harish	8	15	11	8	26	19	45	23	19	42	85
60	4AL21IS061	Syed Saleha	14	14	13	13	28	20	48	24	20	44	88
61	4AL21IS062	Vasavi Rai C	4	7	17	4	24	19	43	22	16	38	90
62	4AL21IS063	Vithika Shetty	17	15	20	15	37	20	57	29	19	48	96

Analog and Digital Electronics CIE Marks 2022-23													
S. No.	USN	Full name	IA1	IA2	IA3	MIN	IA TOTAL (Best Two IA) (40)	ASSIGNMENT (20)	IA + ASMT (60)	Final IA (30)	LAB (20)	TOTAL (50)	Attd
63	4AL21IS064	Chandana N M	12	11	19	11	31	20	51	26	17	**43**	88
64	4AL22IS400	Ankith	7	13	9	7	22	20	42	21	19	**40**	86
65	4AL22IS401	Charan S V	11	17	10	10	28	20	48	24	19	**43**	90
66	4AL22IS402	Chetan Byaleatti	8	17	9	8	26	20	46	23	17	**40**	85
67	4AL22IS405	Rahul P Shetty	4	17	10	4	27	20	47	24	19	**43**	86
68	4AL22IS404	Namratha J Shetty	12	18	16	12	34	20	54	27	19	**46**	92
69	4AL22IS403	Lohith H	12	19	11	11	31	20	51	26	19	**45**	95

ALVA S INSTITUTE OF ENGINEERING AND TECHNOLOGY, MOODBIDRI

Branch : IS Semester : 3

Sl NO.	USN	21CS33
1	4AL21IS001	27 (**TH**) , 18 (**PR**)
2	4AL21IS002	28 (**TH**) , 20 (**PR**)
3	4AL21IS003	25 (**TH**) , 15 (**PR**)
4	4AL21IS004	28 (**TH**) , 20 (**PR**)
5	4AL21IS005	23 (**TH**) , 15 (**PR**)
6	4AL21IS006	30 (**TH**) , 18 (**PR**)
7	4AL21IS007	25 (**TH**) , 18 (**PR**)
8	4AL21IS008	24 (**TH**) , 15 (**PR**)
9	4AL21IS009	27 (**TH**) , 17 (**PR**)
10	4AL21IS010	25 (**TH**) , 16 (**PR**)
11	4AL21IS011	28 (**TH**) , 19 (**PR**)
12	4AL21IS012	30 (**TH**) , 20 (**PR**)
13	4AL21IS013	25 (**TH**) , 14 (**PR**)
14	4AL21IS014	24 (**TH**) , 14 (**PR**)
15	4AL21IS015	24 (**TH**) , 18 (**PR**)
16	4AL21IS017	26 (**TH**) , 16 (**PR**)
17	4AL21IS018	23 (**TH**) , 20 (**PR**)
18	4AL21IS019	27 (**TH**) , 18 (**PR**)
19	4AL21IS020	28 (**TH**) , 18 (**PR**)
20	4AL21IS021	30 (**TH**) , 20 (**PR**)
21	4AL21IS022	29 (**TH**) , 20 (**PR**)
22	4AL21IS023	23 (**TH**) , 15 (**PR**)
23	4AL21IS024	24 (**TH**) , 17 (**PR**)
24	4AL21IS025	30 (**TH**) , 20 (**PR**)
25	4AL21IS026	25 (**TH**) , 15 (**PR**)
26	4AL21IS027	25 (**TH**) , 15 (**PR**)
27	4AL21IS028	15 (**TH**) , 8 (**PR**)
28	4AL21IS029	30 (**TH**) , 20 (**PR**)
29	4AL21IS030	22 (**TH**) , 16 (**PR**)
30	4AL21IS031	25 (**TH**) , 19 (**PR**)
31	4AL21IS032	29 (**TH**) , 20 (**PR**)
32	4AL21IS033	24 (**TH**) , 14 (**PR**)
33	4AL21IS034	29 (**TH**) , 20 (**PR**)
34	4AL21IS035	29 (**TH**) , 20 (**PR**)
35	4AL21IS036	30 (**TH**) , 20 (**PR**)
36	4AL21IS037	27 (**TH**) , 20 (**PR**)

CBCS SCHEME

USN | | | | | | | | | | |

21CS33

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Derive an expression for collector current and collector emitter voltage of voltage divider bias circuit (accurate analysis). **(08 Marks)**

b. Explain relaxation oscillator. **(06 Marks)**

c. Sketch and explain the working of Peak detector. **(06 Marks)**

OR

2 a. Explain R-2R ladder type DAC with a neat diagram. **(06 Marks)**

b. List the advantages of active filters over passive filters. **(06 Marks)**

c. For the circuit shown in Fig. Q2 (c) below find the value of R_1 and R_2 if supply voltages are +12 and −12 V. Assume hysteresis with ±6 V.

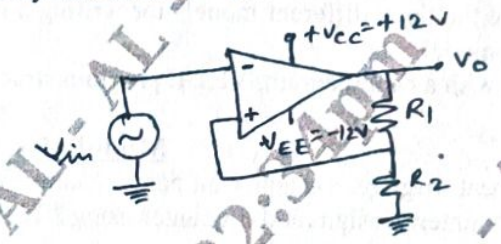


Fig. Q2 (c) **(08 Marks)**

Module-2

3 a. Find all the prime implicates of the function,
$f(a,b,c,d) = \Pi(0,2,3,4,5,12,13) + \Pi d(8,10)$
using the Quine-McCluskey method. **(10 Marks)**

b. Plot the Karnaugh maps and find all the minimal sums and minimal products of the following Boolean functions.
(i) $f(a,b,c) = \sum(2,4,5,6,7)$
(i) $f(a,b,c) = \Pi(1,4,5,6)$ **(10 Marks)**

OR

4 a. With an example, explain Petrik's method. **(06 Marks)**

b. For the given Boolean function, determine a minimal sum and a minimal product using MEV techniques using a, b and c as the map variables.
$f = \sum(3,4,5,7,8,11,12,13,15)$ **(08 Marks)**

c. Explain Entered variable map method. **(06 Marks)**

Module-3

5 a. Explain the importance of three-state buffer. (06 Marks)
b. With a neat diagram, explain 3 to 8 line decoder. (06 Marks)
c. What is a multiplexer? Write the logic diagram for 8 : 1 multiplexer using 4 input AND and OR gates. (08 Marks)

OR

6 a. Discuss different types of hazards in combinational circuits. (08 Marks)
b. Distinguish between combinational and sequential circuit. (06 Marks)
c. Write a note on PLA and PAL. (06 Marks)

Module-4

7 a. Explain the working of JK master slave flip-flop with a sketch, truth table and symbol. (06 Marks)
b. What is D flip flop? Illustrate the operation of the clear and preset inputs in D-flip-flop with timing diagram. (08 Marks)
c. What is VHDL? Show how to model the 4 to 1 multiplexer using a VHDL conditional assignment statement. (06 Marks)

OR

8 a. What is T-flip-flop? Show how to convert D-flip flop into T-flip-flop. (08 Marks)
b. What are the three different models for writing a module body in VHDL? Give example for any one model. (06 Marks)
c. Explain with a neat diagram, VHDL program structure. (06 Marks)

Module-5

9 a. With a neat diagram, explain 4-bit parallel adder with accumulator. (10 Marks)
b. Define counter. Design mod-5 counter using J-K flip flop. (10 Marks)

OR

10 a. With neat diagram, explain 4 bit SISO register. (08 Marks)
b. Mention the Application of shift registers. (05 Marks)
c. Explain the working of a 3 bit shift register. (07 Marks)

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CBCS SCHEME

USN | | | | | | | | | | | | 18CS33

Third Semester B.E. Degree Examination, July/August 2022
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the working principal of photodiode and discuss its applications. **(08 Marks)**

b. Design a monostable multivibrator circuit using 555 Timer IC to generate an output pulse of 100 ms. Choose C = 0.47 μF. Draw the circuit. **(06 Marks)**

c. Give the typical application of A/D and D/A converters with a block diagram. **(06 Marks)**

OR

2 a. Obtain the expression for collector to emitter voltage for voltage divider bias of BJT using accurate analysis. **(08 Marks)**

b. Design and draw astable multivibrator circuit using 555 Timer IC to generate 1 kHz square wave (Duty cycle = 50 %). Assume C = 0.1 μF. **(06 Marks)**

c. Explain R-2R ladder type DAC with a neat diagram. **(06 Marks)**

Module-2

3 a. Define prime implicant and essential prime implicant. Give an example. **(04 Marks)**

b. Use a Karnaugh map to find the minimum sum-of-products form for,

$F(A,B,C,D) = \sum m(0,2,4,10,11,14,15) + \sum d(6,7)$ **(06 Marks)**

c. Find a minimum sum-of-products solution using the Quine-McClusky method for given function,

$f(w,x,y,z) = \sum m(1,3,6,7,8,9,10,12,13,14)$ **(10 Marks)**

OR

4 a. Obtain the minimum product of sums for $f(w,x,y,z) = \bar{x}\bar{z} + wyz + \bar{w}\bar{y}\bar{z} + \bar{x}y$ using Karnaugh map. **(08 Marks)**

b. Find all prime implicants of the given function $F = \sum m(0,1,2,5,6,7)$, and find all minimal solutions using Petrick's method. **(08 Marks)**

c. Explain simplification of logic functions using map-entered variables. **(04 Marks)**

Module-3

5 a. Realize the given function $f = \bar{b}\bar{c} + a\bar{b} + \bar{a}b$ using only two-input NAND gates. **(06 Marks)**

b. Discuss different types of hazards in combinational logic circuits. **(06 Marks)**

c. What is Programmable Array Logic (PAL)? Show the implementation of a full adder using a PAL. **(08 Marks)**

OR

6 a. What is a multiplexer? Write the logic diagram for 8 : 1 multiplexer using 4 input AND and OR gates. **(08 Marks)**

b. Discuss the four kinds of three state buffers. **(08 Marks)**

c. Explain programmable logic array structure. **(04 Marks)**

Module-4

7 a. What is VHDL? Show how to model the 4-to-1 multiplexer using a VHDL conditional assignment statement. **(06 Marks)**

b. Derive the characteristic equation for S-R flip-flop and J-K flip-flop in product-of-sums form. **(06 Marks)**

c. What is D flip-flop? Illustrate the operation of the clear and preset inputs in D-flip-flop with timing diagram. **(08 Marks)**

OR

8 a. Show how to construct a VHDL module using an entity architecture pair. **(06 Marks)**

b. Explain switch debouncing with an S-R latch. **(06 Marks)**

c. What is T flip-flop? Show how to convert D-flip-flop into T-flip-flop. **(08 Marks)**

Module-5

9 a. What is a register? Build a parallel adder with an accumulator using registers. **(06 Marks)**

b. Design 3-bit synchronous counter using T-flip-flops. **(08 Marks)**

c. Design a sequential parity checker for serial data. **(06 Marks)**

OR

10 a. Explain the working of a 3 bit shift register. **(06 Marks)**

b. Distinguish ring counter and Johnson counter. Also give the general form of a shift register counter. **(06 Marks)**

c. Design 3-bit binary synchronous down counter using J-K flip-flops. **(08 Marks)**

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ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

SHOBHAVANA CAMPUS, MIJAR, MOODBIDRI – 574 225

DEPARTMENT OF INFORMATION SCIENCE & ENGINEERING

Jan-Feb 2023 Semester End Examinations (SEE) Results III Semester (2021 Scheme) AY 2022-23 (GRADE)

SN	USN	NAME	21MAT31				21CS32				21CS33				21CS34				21CSL35				21SCR36				21CIP37				21CSL381				21MATDIP31				SGPA	RES
			CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP		
1	4AL21IS001	ADITHYA TEJASWI D	3	B	6	18	4	A	8	32	4	A	8	32	3	A	8	24	1	B+	7	7	1	A+	9	9	1	A	8	8	1	A+	9	9					7.72	PCD
2	4AL21IS002	AFIZA A	3	A	8	24	4	A	8	32	4	A	8	32	3	A	8	24	1	O	10	10	1	O	10	10	1	A	8	8	1	O	10	10					8.33	PCD
3	4AL21IS003	AISHWARYA SALIMATH	0	F	0	0	4	A	8	32	4	A	8	32	3	B+	7	21	1	A	8	8	1	A+	9	9	1	B+	7	7	1	O	10	10					6.61	FAIL
4	4AL21IS004	AKASH DEVADIGA	3	B+	7	21	4	A	8	32	4	A+	9	36	3	A	8	24	1	O	10	10	1	A+	9	9	1	B+	7	7	1	O	10	10					8.28	PCD
5	4AL21IS005	AMAR B M	3	B+	7	21	4	B+	7	28	4	B+	7	28	3	B+	7	21	1	B+	7	7	1	A+	9	9	1	B+	7	7	1	A+	9	9					7.22	PCD
6	4AL21IS006	ANAGHA UDUPA Y N	3	B+	7	21	4	A	8	32	4	A+	9	36	3	A	8	24	1	A+	9	9	1	O	10	10	1	A+	9	9	1	O	10	10					8.39	PCD
7	4AL21IS007	ANANYA	3	B+	7	21	4	A	8	32	4	B+	7	28	3	A	8	24	1	A+	9	9	1	A+	9	9	1	B+	7	7	1	O	10	10					7.78	PCD
8	4AL21IS008	ANIRUDH KAMATH K	3	P	4	12	4	A	8	32	4	B+	7	28	3	A+	9	27	1	A	8	8	1	A+	9	9	1	A	8	8	1	A+	9	9					7.39	PCD
9	4AL21IS009	ANKITHA B	3	B	6	18	4	A	8	32	4	A+	9	36	3	A	8	24	1	A	8	8	1	O	10	10	1	A	8	8	1	O	10	10					8.11	PCD
10	4AL21IS010	BHAGYASHREE R PUJARI	3	B+	7	21	4	A	8	32	4	A	8	32	3	B+	7	21	1	A+	9	9	1	A+	9	9	1	A	8	8	1	O	10	10					7.89	PCD
11	4AL21IS011	BHARATH J	3	B+	7	21	4	B+	7	28	4	A	8	32	3	B+	7	21	1	B+	7	7	1	A	8	8	1	A	8	8	1	A+	9	9					7.44	PCD
12	4AL21IS012	BHUMIKA SUNIL KULKARNI	3	O	10	30	4	A+	9	36	4	A+	9	36	3	A+	9	27	1	O	10	10	1	O	10	10	1	A+	9	9	1	O	10	10					9.33	PCD
13	4AL21IS013	CHAITRA S KODDADDI	3	B	6	18	4	B+	7	28	4	B	6	24	3	A	8	24	0	F	0	0	1	A+	9	9	1	B+	7	7	1	A+	9	9					6.61	FAIL
14	4AL21IS014	CHANDAN M N	3	B	6	18	4	B+	7	28	4	B+	7	28	3	B+	7	21	1	B+	7	7	1	A+	9	9	1	A	8	8	1	A+	9	9					7.11	PCD
15	4AL21IS015	CHINDAN B V	3	B+	7	21	4	A	8	32	4	B+	7	28	3	A	8	24	1	A+	9	9	1	A+	9	9	1	A	8	8	1	O	10	10					7.83	PCD
16	4AL21IS017	GOWRISH N	3	C	5	15	4	A	8	32	4	A	8	32	3	A	8	24	1	O	10	10	1	A+	9	9	1	A	8	8	1	O	10	10					7.78	PCD
17	4AL21IS018	HARSHITHA B	3	A	8	24	4	A+	9	36	4	A	8	32	3	A+	9	27	1	A+	9	9	1	A+	9	9	1	B+	7	7	1	O	10	10					8.56	PCD
18	4AL21IS019	JAHNAVI	3	B+	7	21	4	A	8	32	4	A	8	32	3	A	8	24	1	A+	9	9	1	A+	9	9	1	B+	7	7	1	A+	9	9					7.94	PCD
19	4AL21IS020	KARTHIK MADAKARI T P	3	A+	9	27	4	A+	9	36	4	A+	9	36	3	A	8	24	1	A	8	8	1	A+	9	9	1	A+	9	9	1	A+	9	9					8.78	PCD
20	4AL21IS021	KELVIN DMELLO	3	O	10	30	4	A	8	32	4	O	10	40	3	A	8	24	1	O	10	10	1	O	10	10	1	A+	9	9	1	O	10	10					9.17	PCD
21	4AL21IS022	KOUSHIK ACHAR	3	B+	7	21	4	A+	9	36	4	A+	9	36	3	A+	9	27	1	A+	9	9	1	O	10	10	1	B+	7	7	1	O	10	10					8.67	PCD
22	4AL21IS023	KRUPASHREE R	0	F	0	0	4	B+	7	28	4	B	6	24	3	B	6	18	1	B+	7	7	1	A+	9	9	1	B	6	6	1	A+	9	9					5.61	FAIL
23	4AL21IS024	LAYA R	3	B	6	18	4	A+	9	36	4	B+	7	28	3	B+	7	21	1	A+	9	9	1	O	10	10	1	B+	7	7	1	O	10	10					7.72	PCD
24	4AL21IS025	MANIKANTA	3	B+	7	21	4	A	8	32	4	A+	9	36	3	A	8	24	1	O	10	10	1	A+	9	9	1	B+	7	7	1	O	10	10					8.28	PCD
25	4AL21IS026	MANISH K	3	B	6	18	4	B+	7	28	4	B+	7	28	3	B	6	18	1	A	8	8	1	A+	9	9	1	B+	7	7	1	A+	9	9					6.94	PC
26	4AL21IS027	MANJUNATH R	3	B	6	18	4	B	6	24	4	B+	7	28	3	B	6	18	1	B+	7	7	1	O	10	10	1	B	6	6	1	O	10	10					6.72	PC
27	4AL21IS028	MANOJ LOKESH	0	AB	0	0	0	AB	0	0	0	AB	0	0	0	AB	0	0	0	AB	0	0	0	AB	0	0	0	AB	0	0	0	AB	0	0					0.00	ABS
28	4AL21IS029	MANOJ M U	3	A	8	24	4	A+	9	36	4	A+	9	36	3	A	8	24	1	O	10	10	1	O	10	10	1	A	8	8	1	O	10	10					8.78	PCD
29	4AL21IS030	MOHAMMED ADIL	0	F	0	0	0	F	0	0	4	B	6	24	3	B+	7	21	1	A	8	8	1	A+	9	9	1	B+	7	7	1	A+	9	9					4.33	FAIL
30	4AL21IS031	MOHAMMED RIHAN	3	B+	7	21	4	A	8	32	4	A	8	32	3	A+	9	27	1	A+	9	9	1	A	8	8	1	A	8	8	1	A+	9	9					8.11	PCD
31	4AL21IS032	MUHAMMED YAMIN SHARFUDDIN	3	A	8	24	4	A	8	32	4	A+	9	36	3	B+	7	21	1	A+	9	9	1	O	10	10	1	A	8	8	1	O	10	10					8.33	PCD
32	4AL21IS033	NANDAN S	3	B+	7	21	4	B+	7	28	4	B+	7	28	3	B	6	18	1	B	6	6	1	A+	9	9	1	B+	7	7	1	O	10	10					7.06	PCD

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

SHOBHAVANA CAMPUS, MIJAR, MOODBIDRI – 574 225

DEPARTMENT OF INFORMATION SCIENCE & ENGINEERING

Jan-Feb 2023 Semester End Examinations (SEE) Results III Semester (2021 Scheme) AY 2022-23 (GRADE)

SN	USN	NAME	21MAT31				21CS32				21CS33				21CS34				21CSL35				21SCR36				21CIP37				21CSL381				21MATDIP31				SGPA	RES
			CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP		
33	4AL21IS034	NISHANT KUMAR	3	A	8	24	4	A	8	32	4	B+	7	28	3	B+	7	21	1	O	10	10	1	O	10	10	1	B+	7	7	1	O	10	10					7.89	PCD
34	4AL21IS035	PRAGATHI G GOWDA	3	B+	7	21	4	O	10	40	4	A+	9	36	3	A+	9	27	1	A+	9	9	1	O	10	10	1	A+	9	9	1	O	10	10					9.00	PCD
35	4AL21IS036	PRAJNA	3	A+	9	27	4	A	8	32	4	A	8	32	3	A+	9	27	1	O	10	10	1	O	10	10	1	A+	9	9	1	O	10	10					8.72	PCD
36	4AL21IS037	PRAJWAL GOWDA H G	3	A	8	24	4	A	8	32	4	A	8	32	3	A+	9	27	1	B+	7	7	1	A+	9	9	1	A	8	8	1	O	10	10					8.28	PCD
37	4AL21IS038	PRASHANTH KUMAR B C	3	C	5	15	4	B+	7	28	4	C	5	20	3	B	6	18	1	C	5	5	1	A+	9	9	1	A	8	8	1	A+	9	9					6.22	PC
38	4AL21IS039	PREETHAM BYADAGI	0	F	0	0	4	A	8	32	4	C	5	20	3	B+	7	21	1	B+	7	7	1	A	8	8	1	B+	7	7	1	A	8	8					5.72	FAIL
39	4AL21IS040	R SREEJITH	3	B	6	18	4	B+	7	28	4	B	6	24	3	B+	7	21	1	A+	9	9	1	A+	9	9	1	A	8	8	1	A+	9	9					7.00	PCD
40	4AL21IS041	RANJITH	3	C	5	15	4	A+	9	36	4	A	8	32	3	A+	9	27	1	A+	9	9	1	A+	9	9	1	A	8	8	1	A+	9	9					8.06	PCD
41	4AL21IS042	SANJAY G K	3	B+	7	21	4	B+	7	28	4	A	8	32	3	B+	7	21	1	B+	7	7	1	A+	9	9	1	A	8	8	1	A+	9	9					7.50	PCD
42	4AL21IS043	SANNIDHI K S	3	B+	7	21	4	A+	9	36	4	A	8	32	3	A	8	24	1	B+	7	7	1	A+	9	9	1	A	8	8	1	A+	9	9					8.11	PCD
43	4AL21IS044	SAPTHAMI	3	A+	9	27	4	A+	9	36	4	A	8	32	3	A	8	24	1	A+	9	9	1	O	10	10	1	A+	9	9	1	O	10	10					8.72	PCD
44	4AL21IS045	SARTHAK K JAIN	3	B	6	18	4	B	6	24	4	B+	7	28	3	B+	7	21	1	A	8	8	1	O	10	10	1	B+	7	7	1	O	10	10					7.00	PCD
45	4AL21IS046	SATEESH DYAVAPPA SATYANNAVA	3	B+	7	21	0	F	0	0	4	B+	7	28	3	B	6	18	1	O	10	10	1	A+	9	9	1	A	8	8	1	O	10	10					5.78	FAIL
46	4AL21IS047	SATHWIK K D	3	B+	7	21	4	O	10	40	4	A	8	32	3	A+	9	27	1	O	10	10	1	O	10	10	1	A	8	8	1	O	10	10					8.78	PCD
47	4AL21IS048	SHARAVI R RAI	3	B+	7	21	4	B+	7	28	4	B+	7	28	3	B+	7	21	1	B+	7	7	1	O	10	10	1	A	8	8	1	O	10	10					7.39	PCD
48	4AL21IS049	SHASHIDHAR MAHADEV PATGAR	3	A+	9	27	4	A	8	32	4	A+	9	36	3	B+	7	21	1	O	10	10	1	A+	9	9	1	A	8	8	1	O	10	10					8.50	PCD
49	4AL21IS050	SHRAVAN R POOJARY	3	B	6	18	4	B+	7	28	4	B+	7	28	3	B+	7	21	1	B+	7	7	1	O	10	10	1	A	8	8	1	A+	9	9					7.17	PCD
50	4AL21IS051	SHRAVITHA	3	B	6	18	4	A	8	32	4	A	8	32	3	A	8	24	1	A	8	8	1	A+	9	9	1	B+	7	7	1	A+	9	9					7.72	PCD
51	4AL21IS052	SHREYA RAI	3	B	6	18	4	A	8	32	4	A+	9	36	3	A	8	24	1	A+	9	9	1	O	10	10	1	A+	9	9	1	O	10	10					8.22	PCD
52	4AL21IS053	SHRUJAN KUMAR H V	3	P	4	12	4	B+	7	28	4	B	6	24	0	F	0	0	1	B	6	6	1	A+	9	9	1	B+	7	7	1	A+	9	9					5.28	FAIL
53	4AL21IS054	SOORAJ	3	B+	7	21	4	A	8	32	4	A+	9	36	3	A	8	24	1	A	8	8	1	A+	9	9	1	B+	7	7	1	O	10	10					8.17	PCD
54	4AL21IS055	SRIDEEKSHA G	3	B	6	18	4	B+	7	28	4	A	8	32	3	B+	7	21	1	A	8	8	1	O	10	10	1	A	8	8	1	O	10	10					7.50	PCD
55	4AL21IS056	SRIKANTH RAJU SRINIVAS	0	F	0	0	4	B+	7	28	4	B+	7	28	3	A	8	24	1	B	6	6	1	A	8	8	1	B	6	6	1	A+	9	9					6.06	FAIL
56	4AL21IS057	SRUJAN K M	3	A	8	24	4	A	8	32	4	A	8	32	3	B+	7	21	1	O	10	10	1	O	10	10	1	A	8	8	1	A+	9	9					8.11	PCD
57	4AL21IS058	SRUSTI P S	3	A+	9	27	4	A	8	32	4	A	8	32	3	A	8	24	1	A+	9	9	1	O	10	10	1	A+	9	9	1	O	10	10					8.50	PCD
58	4AL21IS059	SUVAN P KEDILAYA	3	A+	9	27	4	A+	9	36	4	A+	9	36	3	A	8	24	1	B+	7	7	1	O	10	10	1	A	8	8	1	A+	9	9					8.72	PCD
59	4AL21IS060	SUVARNA ARVINKANTH HARISH	3	C	5	15	4	B+	7	28	4	A	8	32	3	A	8	24	1	A	8	8	1	A+	9	9	1	B+	7	7	1	A+	9	9					7.33	PCD
60	4AL21IS061	SYED SALEHA	3	B+	7	21	4	A	8	32	4	A+	9	36	3	B+	7	21	1	O	10	10	1	A+	9	9	1	B+	7	7	1	O	10	10					8.11	PCD
61	4AL21IS062	VASAVI RAI C	0	F	0	0	4	A	8	32	4	A+	9	36	3	B+	7	21	1	B+	7	7	1	O	10	10	1	B+	7	7	1	A+	9	9					6.78	FAIL
62	4AL21IS063	VITHIKA SHETTY	3	A	8	24	4	A	8	32	4	A	8	32	3	A+	9	27	1	A+	9	9	1	O	10	10	1	A	8	8	1	O	10	10					8.44	PCD
63	4AL21IS064	CHANDANA N M	3	B+	7	21	4	A+	9	36	4	A	8	32	3	A+	9	27	1	A	8	8	1	O	10	10	1	A+	9	9	1	O	10	10					8.50	PCD

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY

SHOBHAVANA CAMPUS, MIJAR, MOODBIDRI – 574 225

DEPARTMENT OF INFORMATION SCIENCE & ENGINEERING

Jan-Feb 2023 Semester End Examinations (SEE) Results III Semester (2021 Scheme) AY 2022-23 (GRADE)

SN	USN	NAME	21MAT31				21CS32				21CS33				21CS34				21CSL35				21SCR36				21CIP37				21CSL381				21MATDIP31				SGPA	RES
			CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP	CE	GL	GP	CP		
64	4AL22IS400	ANKITH	0	F	0	0	4	B+	7	28	4	B	6	24	3	B	6	18	1	A+	9	9	1	A+	9	9	1	B+	7	7	1	A+	9	9	0	A+	9	0	5.78	FAIL
65	4AL22IS401	CHARAN S V	3	C	5	15	0	F	0	0	4	B+	7	28	3	B+	7	21	1	B+	7	7	1	A+	9	9	1	B	6	6	1	O	10	10	0	A	8	0	5.33	FAIL
66	4AL22IS402	CHETAN BYAHATTI	0	F	0	0	0	F	0	0	4	A	8	32	3	B+	7	21	1	B+	7	7	1	A+	9	9	1	C	5	5	1	A+	9	9	0	A	8	0	4.61	FAIL
67	4AL22IS403	LOHITH H	3	B+	7	21	4	B+	7	28	4	A	8	32	3	A	8	24	1	O	10	10	1	A+	9	9	1	B+	7	7	1	O	10	10	0	A+	9	0	7.83	FCD
68	4AL22IS404	NAMRATHA J SHETTY	0	F	0	0	4	B+	7	28	4	A	8	32	3	A	8	24	1	O	10	10	1	A+	9	9	1	B+	7	7	1	O	10	10	0	O	10	0	6.67	FAIL
69	4AL22IS405	RAHUL P SHETTY	0	F	0	0	4	B+	7	28	4	B+	7	28	3	B+	7	21	1	A	8	8	1	A+	9	9	1	B	6	6	1	O	10	10	0	O	10	0	6.11	FAIL

Result Analysis - Subjectwise - III Semester 2022-23 (2021 Scheme)

SN	Subject	Sub Code	Total	O	A+	A	B+	B	C	P	F	AB	Percentage	>= A (70)%
1	TRANSFORM CALCULUS, FOURIER SERIES AND NUMERICAL	21MAT31	69	2	6	8	22	13	5	2	10	1	85.29	23.53
2	DATA STRUCTURES AND APPLICATIONS	21CS32	69	2	11	29	20	2	0	0	4	1	94.12	61.76
3	ANALOG AND DIGITAL ELECTRONICS	21CS33	69	1	16	26	17	6	2	0	0	1	100.00	63.24
4	COMPUTER ORGANIZATION AND ARCHITECTURE	21CS34	69	0	12	25	23	7	0	0	1	1	98.53	54.41
5	OBJECT ORIENTED PROGRAMMING WITH JAVA LABORATORY	21CSL35	69	16	18	13	16	3	1	0	1	1	98.53	69.12
6	SOCIAL CONNECT AND RESPONSIBILITY	21SCR36	69	26	38	4	0	0	0	0	0	1	100.00	100.00
7	CONSTITUTION OF INDIA AND PROFESSIONAL ETHICS	21CIP37	69	0	10	27	25	5	1	0	0	1	100.00	54.41
8	MASTERING OFFICE	21CSL381	69	40	27	1	0	0	0	0	0	1	100.00	100.00
9	ADDITIONAL MATHEMATICS - I	21MATDIP31	6	2	2	2	0	0	0	0	0	0	100.00	100.00

Overall	Total	FCD	FC	SC	FL	AB	>= 9	>= 8	>= 7	>= 6	Percentage
III Sem IS	69	51	3	0	14	1	3	29	51	60	79.41

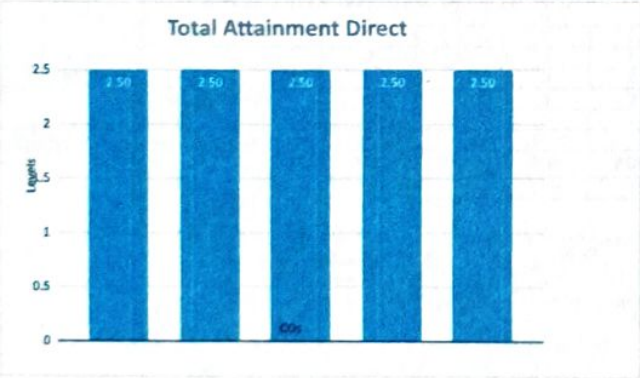
PRINCIPAL
Alva's Institute of Engg. & Technology
Mijar, MOODBIDRI - 574 225, D.K

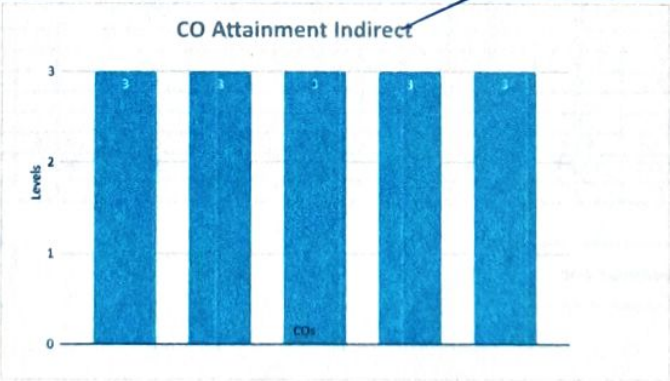
COURSE OUTCOMES (COs) ASSESSMENT MATRIX					
Alva's Institute of Engineering and Technology, Moodbidri					
Department of Information Science and Engineering					
Academic Year:	2022-2023			CO Attainment Indirect	CO Attainment
Course Name & Course Code:	Analog and Digital Electronics/18CS33				
Faculty Name:	Mr.SHARAN LIONAL PAIS				
CO Attainment - Direct					
Cos	**Formative Assessment**	**Summative Assessment**	**Total Attainment**		
18CS33.1	**3**	**2**	**2.50**	**3**	**2.55**
18CS33.2	**3**	**2**	**2.50**	**3**	**2.55**
18CS33.3	**3**	**2**	**2.50**	**3**	**2.55**
18CS33.4	**3**	**2**	**2.50**	**3**	**2.55**
18CS33.5	**3**	**2**	**2.50**	**3**	**2.55**
18CS33.6					
Average			**2.50**	**3**	**2.55**

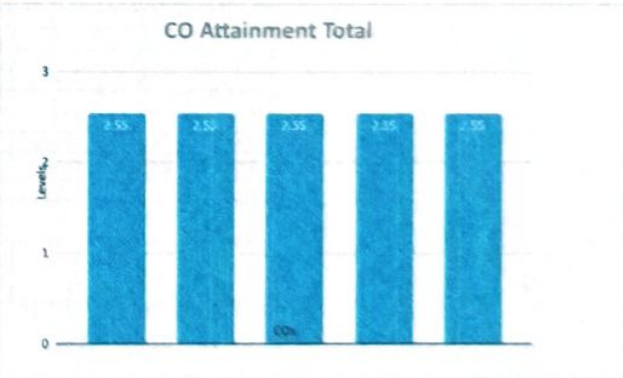
Note:
Total Attainment Direct = (Weightage*Formative Assessment)+(Weightage*Summative Assessment)
Weightage for Formative Assessment = 50%;
Weightage for Summative Assessment = 50%

CO Attainment = (Weightage*Total Attainment Direct)+(Weightage*CO Attainment Indirect)
Weightage for Total Attainment Direct = 90%;
Weightage for CO Attainment Indirect = 10%

Faculty Name & Signature:	Sharan	**HOD Signature:**	







PROGRAMME OUTCOME & PROGRAMME SPECIFIC OUTCOME ASSESSMENT MATRIX

Alva's Institute of Engineering and Technology, Moodbidri

Department of Information Science and Engineering

Academic Year:	2022-2023
Course Name:	Analog and Digital Electronics
Course Code:	18CS33
Faculty Name:	Mr. SHARAN UJONAL PAIS

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
18CS33.1	2	1										1	2		
18CS33.2	2	2											1		
18CS33.3	2	2	2	1									1		
18CS33.4	2	2	1		1								1		1
18CS33.5	2	2	2	1									1		
18CS33.6															
AVG	2	1.8	1.67	1	1							1	1.2		1

Key Words (POs)	Apply Knowledge	Solve Problems	Design/ Development of Solution	Conduct Investigations	Use Modern Tools	Engineer and Society	Environment and Sustainability	Professional Ethics	Individual and Team Work	Communicate Effectively	Project Management and Finance	Life-long Learning	PSO 1	PSO 2	PSO 3
18CS33 Direct (X)	1.67	1.51	1.4	0.84	0.84	0	0	0	0	0	0	0.84	1.01	0	0.84
18CS33 Indirect (Y)	2	1.8	1.67	1	1	0	0	0	0	0	0	1	1.2	0	1
Attainment Level	1.71	1.54	1.43	0.86	0.86	0	0	0	0	0	0	0.86	1.03	0	0.86

PO Attainment Calculation Direct

COs	CO Attainment Grade	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
18CS33.1	2.50	1.67	0.84	0	0	0	0	0	0	0	0	0	0.84	1.67	0	0
18CS33.2	2.50	1.67	1.67	0	0	0	0	0	0	0	0	0	0	0.84	0	0
18CS33.3	2.50	1.67	1.67	1.67	0.84	0	0	0	0	0	0	0	0	0.84	0	0
18CS33.4	2.50	1.67	1.67	0.84	0	0.84	0	0	0	0	0	0	0	0.84	0	0.84
18CS33.5	2.50	1.67	1.67	1.67	0.84	0	0	0	0	0	0	0	0	0.84	0	0
18CS33.6		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Weighted Sum --->	8.35	7.52	4.18	1.68	0.84	0	0	0	0	0	0	0.84	5.03	0	0.84
	Max Weight --------->	10	9	5	2	1	0	0	0	0	0	0	1	6	0	1
PO Attainment in percentage	:--------->	83.50	83.56	83.60	84.00	84.00	0.00	0.00	0.00	0.00	0.00	0.00	84.00	83.83	0.00	84.00
	PO Attained Grade	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
		1.67	1.51	1.4	0.84	0.84	0	0	0	0	0	0	0.84	1.01	0	0.84

PO Attainment Calculation Indirect

COs	CO Attainment Grade	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
18CS33.1	3	2	1	0	0	0	0	0	0	0	0	0	1	2	0	0
18CS33.2	3	2	2	0	0	0	0	0	0	0	0	0	0	1	0	0
18CS33.3	3	2	2	2	1	0	0	0	0	0	0	0	0	1	0	0
18CS33.4	3	2	2	1	0	1	0	0	0	0	0	0	0	1	0	1
18CS33.5	3	2	2	2	1	0	0	0	0	0	0	0	0	1	0	0
18CS33.6		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Weighted Sum --->	10	9	5	2	1	0	0	0	0	0	0	1	6	0	1
	Max Weight --------->	10	9	5	2	1	0	0	0	0	0	0	1	6	0	1
PO Attainment in percentage	:--------->	100.00	100.00	100.00	100.00	100.00	0.00	0.00	0.00	0.00	0.00	0.00	100.00	100.00	0.00	100.00
	PO Attained Grade	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
		2	1.8	1.67	1	1	0	0	0	0	0	0	1	1.2	0	1

Faculty Name & Signature:	Sharan
HOD Signature:	

Academic Year:	2022-2023
Course Name:	Analog and Digital Electronics
Course Code:	18CS33
Faculty Name:	Mr.SHARAN LIONAL PAIS

Observations and Action Plan (Direct)

Course	Target	Attainment	Gap	Observation	Action Proposed to bridge the Gap
18CS33	2	2.50	0.00	Target Achieved	NIL

Outcomes on Actions for CAYm1 Observations/Suggestions

Sl. No.	Action Taken	Change Observed
1	Target achieved. Planned to continue the same teaching methodology.	Students were facing diffculty in solving apply level concepts, now it has been resolved by giving more number of excercise problems

Faculty Name & Signature:	Sharan

HOD Signature:	

ALVA'S INSTITUTE OF ENGINEERING & TECHNOLOGY
(Unit of Alva's Education Foundation (R), Moodbidri)
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Department of Information Science and Engineering

List of Fast Learners - Second Year 2022-23

SL NO	USN	NAME	CGPA
1.	4AL21IS036	Prajna	9.33
2.	4AL21IS032	M. Yamin Sharfudd	8.98
3.	4AL21IS021	Kelviin D'Mello	8.93
4.	4AL21IS012	Bhumika Sunil K	8.88
5.	4AL21IS063	Vithika Shetty	8.85
6.	4AL21IS029	Manoj M U	8.83

List of Slow Learners - Second Year 2022-23

SL NO	USN	NAME	CGPA
1.	4AL21IS062	VASAVI RAI C	6.5
2.	4AL21IS013	CHAITRA S KODDADDI	7.5
3.	4AL21IS014	CHANDAN M N	6.2
4.	4AL21IS023	KRUPASHREE R	6.3
5.	4AL21IS030	MOHAMMED ADIL	7.1
6.	4AL21IS039	PREETHAM BYADAGI	6.1

HOD