ANALOG AND DIGITAL ELECTRONICS LABORATORY
[As per Choice Based Credit System (CBCS) scheme]
(Effective from the academic year 2017 -2018)
SEMESTER - III

Laboratory Code	**17CSL37**	**IA Marks**	**40**
Number of Lecture Hours/Week	**01I + 02P**	**Exam Marks**	**60**
Total Number of Lecture Hours	**40**	**Exam Hours**	**03**

CREDITS – 02

Descriptions (if any)

Any simulation package like MultiSim / P-spice /Equivalent software may be used.
Faculty-in-charge should demonstrate and explain the required hardware components and their functional Block diagrams, timing diagrams etc. Students have to prepare a write-up on the same and include it in the Lab record and to be evaluated.

Laboratory Session-1: Write-upon analog components; functional block diagram, Pin diagram (if any), waveforms and description. The same information is also taught in theory class; this helps the students to understand better.

Laboratory Session-2: Write-upon Logic design components, pin diagram (if any), Timing diagrams, etc. The same information is also taught in theory class; this helps the students to understand better.

Note: These **TWO Laboratory sessions** are used to fill the gap between theory classes and practical sessions. Both sessions are to be evaluated for 40 marks as lab experiments.

Laboratory Experiments:

1. a) Design and construct a Schmitt trigger using Op-Amp for given UTP and LTP values and demonstrate its working.
   b) Design and implement a Schmitt trigger using Op-Amp using a simulation package for two sets of UTP and LTP values and demonstrate its working.

2. a) Design and construct a rectangular waveform generator (Op-Amp relaxation oscillator) for given frequency and demonstrate its working.
   b) Design and implement a rectangular waveform generator (Op-Amp relaxation oscillator) using a simulation package and demonstrate the change in frequency when all resistor values are doubled.

3. Design and implement an Astable multivibrator circuit using 555 timer for a given frequency and duty cycle.

NOTE: hardware and software results need to be compared

4. Design and implement Half adder, Full Adder, Half Subtractor, Full Subtractor using basic gates.

5. a) Given a 4-variable logic expression, simplify it using Entered Variable Map and realize the simplified logic expression using 8:1 multiplexer IC.
   b) Design and develop the Verilog /VHDL code for an 8:1 multiplexer. Simulate and verify its working.

6. a) Design and implement code converter I)Binary to Gray (II) Gray to Binary Code using basic gates.

7. Design and verify the Truth Table of 3-bit Parity Generator and 4-bit Parity Checker using basic Logic Gates with an even parity bit.

8. a) Realize a J-K Master / Slave Flip-Flop using NAND gates and verify its truth table.

b) Design and develop the Verilog / VHDL code for D Flip-Flop with positive-edge triggering. Simulate and verify it's working.

9. a) Design and implement a mod-n (n<8) synchronous up counter using J-K Flip-Flop ICs and demonstrate its working.

b) Design and develop the Verilog / VHDL code for mod-8 up counter. Simulate and verify it's working.

10. Design and implement an asynchronous counter using decade counter IC to count up from 0 to n (n<=9) and demonstrate on 7-segment display (using IC- 7447).

11. Generate a Ramp output waveform using DAC0800 (Inputs are given to DAC through IC74393 dual 4-bit binary counter).

Study experiment

12. To study 4-bitALU using IC-74181.

Course outcomes:

On the completion of this laboratory course, the students will be able to:

- Demonstrate various Electronic Devices like Cathode ray Oscilloscope, Signal generators, Digital Trainer Kit, Multimeters and components like Resistors, Capacitors, Op amp and Integrated Circuit.
- Design and demonstrate various combinational logic circuits.
- Design and demonstrate various types of counters and Registers using Flip-flops
- Make use of simulation package to design circuits.
- Infer the working and implementation of ALU.

Conduction of Practical Examination:

1. All laboratory experiments (1 to 11 nos) are to be included for practical examination.
2. Students are allowed to pick one experiment from the lot.
3. Strictly follow the instructions as printed on the cover page of answer script.
4. Marks distribution:
   a) For questions having part a only- Procedure + Conduction + Viva:**15 + 70 +15 =100 Marks**
   b) For questions having part a and b
   Part a- Procedure + Conduction + Viva:**09 + 42 +09= 60 Marks**
   Part b- Procedure + Conduction + Viva:**06 + 28 +06= 40 Marks**
5. **Change of experiment is allowed only once and marks allotted to the procedure part to be made zero.**

DATA STRUCTURES LABORATORY
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